PEEL™ 20CG10

AMI SEMICONDUCTORS

CMOS Programmable Electrically Erasable Logic Device

February 1993

Features

Advanced CMOS EEPROM™ Technology

High Performance with Low Power Consumption

- tPD = 25ns Max, tCO = 15ns Max
- 65mA + 0.5mA/MHz Max

EE Reprogrammability

- Superior programming and functional yield
- Low-cost, "windowless" package
- Erases and programs in seconds

Development/Programmer Support

- Third-party software and programmers
- AMI PEEL Development Software with APEEL Logic Assembler
- Software controlled write protection

Architectural Flexibility

- 92 product term X 44 input AND array
- Up to 22 Inputs and 10 Outputs
- Independently programmable 12-configuration I/O macrocells
- Synchronous preset, asynchronous clear
- Independent programmable output enables

Application Versatility

- Replaces random SSI/MSI logic
- Emulates 24-pin bipolar PAL®, GAL®, and EPLD devices
- Convert 24-pin PAL®and EPLD designs with AMI software
- Superset-compatible with the CMOS PALC20G10

General Description

The AMI PEEL20CG10 is a CMOS Programmable Electrically Erasable Logic device that provides a high-performance, low-power, reprogrammable, and architecturally enhanced alternative to conventional programmable logic devices (PLDs). Designed in advanced CMOS EEPROM technology, the PEEL20CG10 rivals speed parameters of comparable bipolar PLDs while dramatically improving power consumption. EE reprogrammability simplifies inventory management, reduces development and field retrofit costs, and enhances testability to ensure 100% field programmability and function, while allowing for low-cost, "windowless" packaging in a 24-pin, 300-mil DIP.

The PEEL20CG10's flexible architecture and AMI's JEDEC file translator allows the PEEL20CG10 to replace bipolar 24-pin PAL® devices without the need to rework the existing design. Applications for the PEEL20CG10 include replacement of random SSI/MSI logic circuitry, emulation of 24-pin bipolar PAL® devices, and user customized sequential and combinational functions such as counters, shift registers, state machines, address decoders, multiplexers, etc. Development support for the PEEL20CG10 is provided by AMI and third-party manufacturers. Programming support is provided by third-party manufacturers.

Figure 13: PEEL20CG10 Pin and Block Diagram

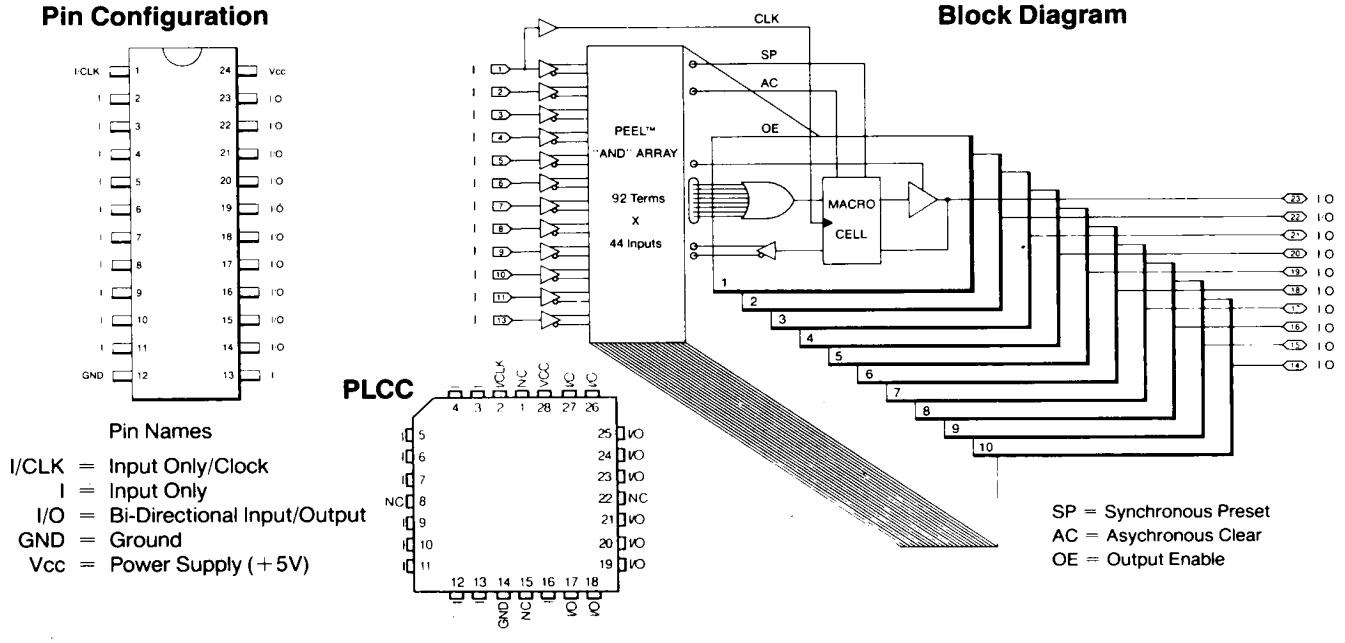
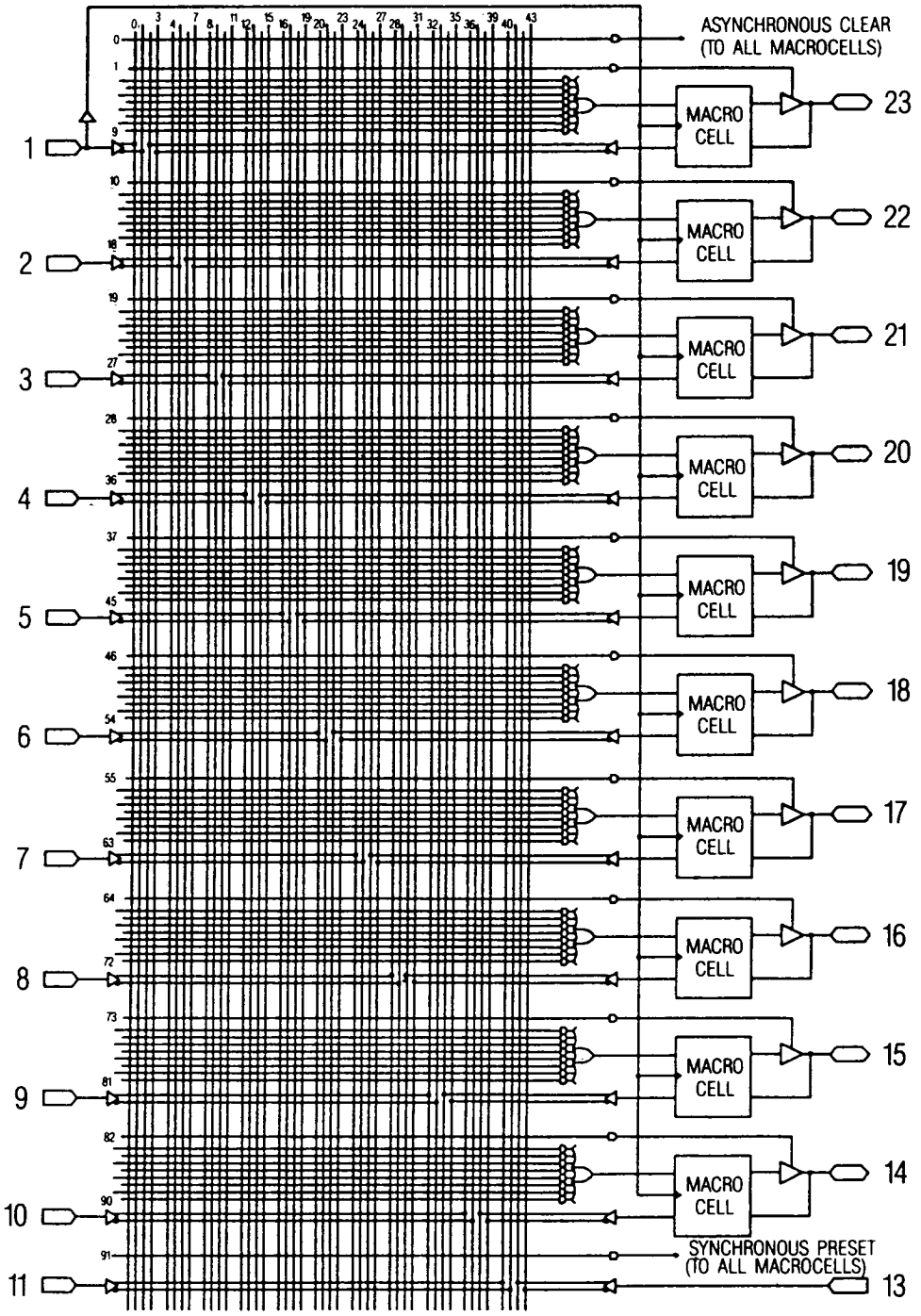


Figure 14: PEEL20CG10 Logic Array Diagram



Function Description

The PEEL20CG10 implements logic functions as sum-of-products expressions in a programmable-AND/fixed-OR logic array. User-defined functions are created by programming the connections of input signals into the array. User-configurable output structures in the form of I/O macrocells further increase logic flexibility.

Architectural Overview

The PEEL20CG10 architecture is illustrated in the block diagram of figure 13. Twelve dedicated inputs and 10 I/Os provide up to 22 inputs and 10 outputs for creation of logic functions. At the core of the device is a programmable electrically-erasable AND array which drives a fixed-OR array. With this structure, the PEEL20CG10 can implement up to 10 sum-of-products logic expressions.

Associated with each of the 10 OR functions is an I/O macrocell that can be independently programmed to one of 12 different configurations. The programmable macrocells allow each I/O to create sequential or combinational logic functions of active-high or active-low polarity, while providing three different feedback paths into the AND array.

AND/OR Logic Array

The programmable-AND array of the PEEL20CG10 (shown in figure 14) is formed by input lines intersecting product terms. The input lines and product terms are used as follows:

44 Input Lines:

24 input lines carry the true and complement of the signals applied to the 12 input pins

20 additional lines carry the true and complement values of feedback or input signals from the 10 I/Os

92 product terms:

80 product terms (8 per I/O) used to form logical sums

10 output enable terms (one for each I/O)

1 global synchronous preset term

1 global asynchronous clear term

At each input-line/product-term intersection is an EEPROM memory cell which determines whether or not a logical connection exists at that intersection. Each product term is essentially a 44-input AND gate. A product term that is connected to both the true and complement of an input signal will always be FALSE and thus will not affect the OR function that it drives. When all the connections on a product term are opened, a don't care state exists and that term will always be TRUE.

When programming the PEEL20CG10, the device programmer first performs a bulk erase to instantly remove the previous pattern. The erase cycle opens every logical connection in the array. The device is configured to perform the user-defined function by programming selected connections in the AND array. (Note that PEEL device programmers automatically program all of the connections on unused product terms so that they will have no effect on the output function.)

Programmable I/O Macrocell

The unique 12-configuration output macrocell provides complete control over the architecture of each output. The ability to configure each output independently permits users to tailor the configuration of the PEEL20CG10 to the precise requirements of their designs.

Macrocell Architecture

Each I/O macrocell, as shown in figure 15, consists of a D-type flip-flop and two signal-select multiplexers. The configurations of each macrocell are determined by the four EEPROM bits controlling these multiplexers. These bits determine output polarity, output type (registered or non-registered), and input/feedback path (bi-directional I/O, combinational feedback, or register feedback). Refer to page 29 for details.

Equivalent circuits for the 12 macrocell configurations are illustrated in figure 16. In addition to emulating the four PAL- type output structures (configurations 3, 4, 9, and 10), the macrocell provides eight configurations that are unavailable in any PAL® device. When creating a PEEL device design, the desired macrocell configuration generally is specified explicitly in the design file. When the design is assembled or compiled, the macrocell configuration bits are defined in the last lines of the JEDEC programming file.

Output Type

The signal from the OR array can be fed directly to the output pin or latched in the D-type flip-flop (registered function). The D-type flip-flop latches data on the rising edge of the clock and is controlled by the global preset and clear terms. When the synchronous preset term is satisfied, the Q output of the register will be set HIGH at the next rising edge of the clock input. Satisfying the asynchronous clear term will set Q LOW, regardless of the clock state. If both terms are satisfied simultaneously, the clear will override the preset.

Output Polarity

Each macrocell can be configured to implement active-high or active-low logic. Programmable polarity eliminates the need for external inverters.

Output Enable

The output of each I/O macrocell can be enabled or disabled under the control of its associated programmable output enable product term. When the logical conditions programmed on the output enable term are satisfied, the output signal is propagated to the I/O pin. Otherwise, the output buffer is driven into the high-impedance state.

Under the control of the output enable term, the I/O pin can function as a dedicated input, a dedicated output, or a bi-directional I/O. Opening every connection on the output enable term will permanently enable the output buffer and yield a dedicated output. Conversely, if every connection is intact, the enable term will always be logically false and the I/O will function as a dedicated input.

Input/Feedback Select

The PEEL20CG10 macrocell also provides control over the feedback path. The input/feedback signal associated with each I/O macrocell may be obtained from three different locations: from the I/O pin (bi-directional I/O), directly from the $\overline{Q}$ output of the flip-flop (registered feedback), or directly from the OR gate (combinational feedback).

Bi-Direction I/O

The input/feedback signal is taken from the I/O pin when using the pin as a dedicated input or as a bi-directional I/O. (Note that it is possible to create a registered output function with bi-directional I/O.)

Combinatorial Feedback

The signal-select multiplexer gives the macrocell the ability to feedback the output of either the OR gates, bypassing the output buffer, regardless of whether the output function is registered or combinational. This feature allows the creation of asynchronous latches, even when the output must be disabled. (Refer to configurations 5, 6, 7, and 8 in figure 16.)

Figure 15: PEEL20CG10 Macrocell Diagram

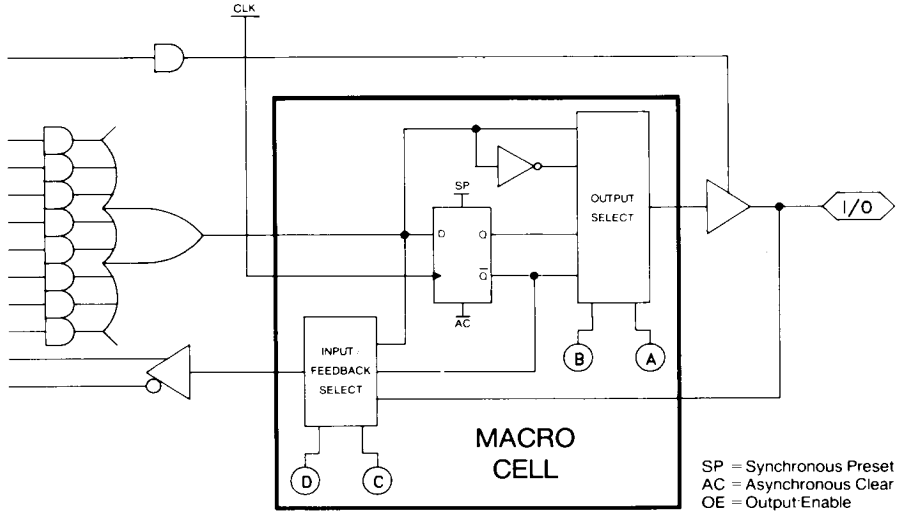


Figure 16: PEEL20CG10 Macrocell Configuration Equivalent Circuits

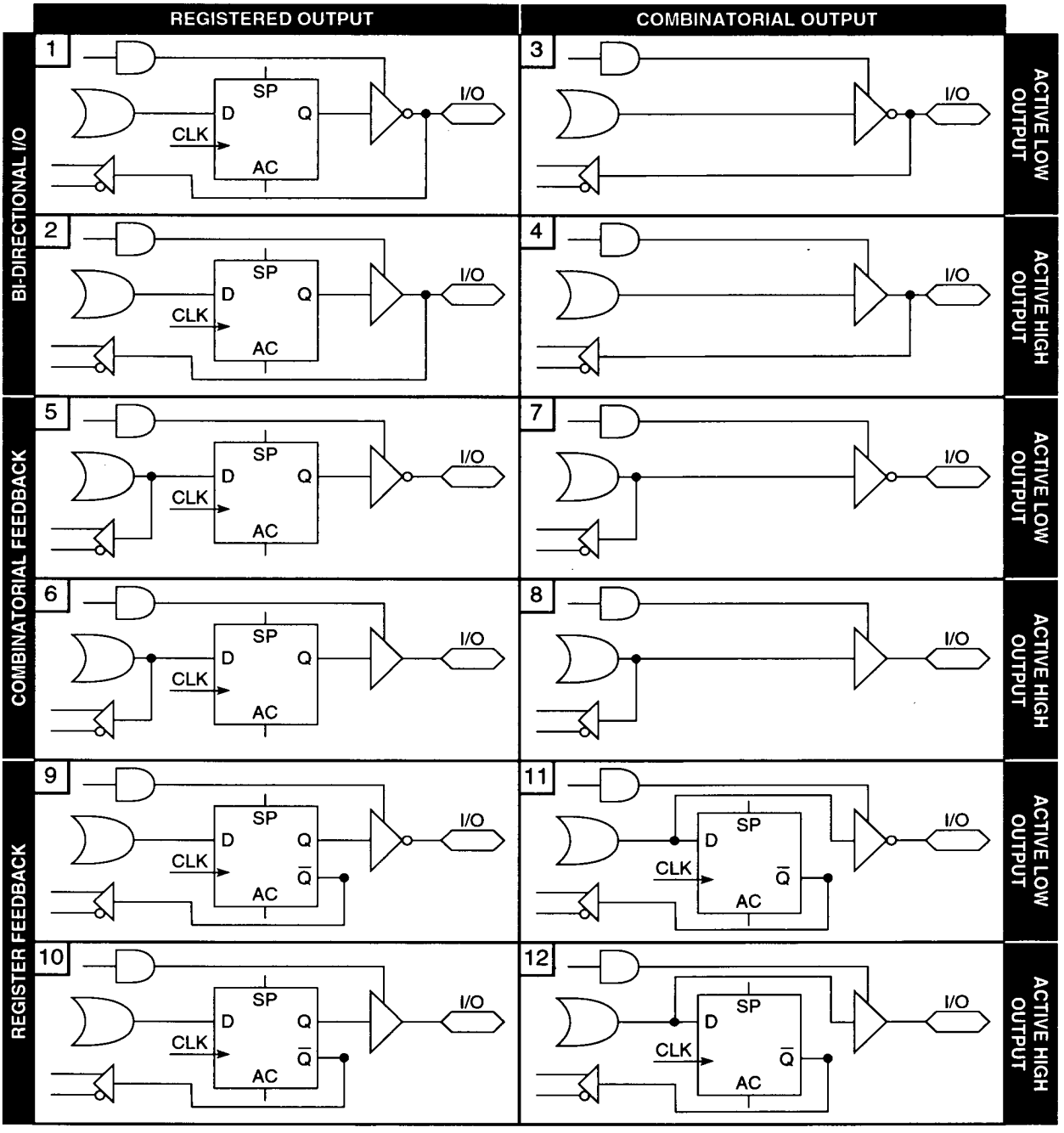


Figure 17: PEEL20CG10 Macrocell Configuration Bits

Configuration					Input/Feedback Select	Output Select	
#	A	B	C	D			
1	0	0	1	0	Bi-Directional I/O	Register	Active Low
2	1	0	1	0	Bi-Directional I/O	Register	Active High
3	0	1	0	0	Bi-Directional I/O	Combinational	
4	1	1	0	0	Bi-Directional I/O	Combinational	Active High
5	0	0	1	1	Combinational Feedback	Register	Active Low
6	1	0	1	1	Combinational Feedback	Register	Active High
7	0	1	1	1	Combinational Feedback	Combinational	Active Low
8	1	1	1	1	Combinational Feedback	Combinational	Active High
9	0	0	0	0	Register Feedback	Register	Active Low
10	1	0	0	0	Register Feedback	Register	Active High
11	0	1	1	0	Register Feedback	Combinational	Active Low
12	1	1	1	0	Register Feedback	Combinational	Active High

Registered Feedback

Feedback also can be taken from the register, regardless of whether the output function is to be combinational or registered. When implementing the combinational output function, registered feedback allows for the internal latching of states without giving up the use of the external output.

Design Security

The PEEL20CG10 provides a special EEPROM security bit that prevents unauthorized reading or copying of designs programmed into the device. The security bit is set by the PLD programmer, either at the conclusion of the programming cycle or as a separate step after the device has been programmed. Once the security bit is set, it is impossible to verify (read) or program the PEEL until the entire device has first been erased with the bulk-erase function.

Signature Word

The signature word feature allows a 24-bit code to be programmed into the PEEL20CG10. This code then can be read back even after the security bit has been set. The signature word can be used to identify the pattern that has been programmed into the device or to record the date of programming, design revision, etc.

Absolute Values

Absolute Maximum Ratings[8]

SYMBOL	PARAMETER	CONDITIONS	MIN	MAX	UNIT
Vcc	Supply Voltage	Relative to GND	-0.5	7.0	V
Vi	Voltage applied to Input[2,4]	Relative to GND[1]	-0.5	Vcc +0.6	V
Vo	Voltage applied to Output[2]	Relative to GND[1]	-0.5	Vcc +0.6	V
Io	Output Current	Per pin (Iol, Ioh)		+25	mA
Tst	Storage Temperature		-65	+150	C
Tlt	Lead Temperature	(soldering 10 seconds)		+300	C

Operating Ranges

SYMBOL	PARAMETER	CONDITIONS	MIN	MAX	UNIT
Vcc	Supply Voltage	Commercial	4.75	5.25	V
		Industrial	4.5	5.5	V
Ta	Operating Temperature	Commerical	0	+70	C
		Industrial	-40	+85	C
Tr	Clock Rise Time[5]	Test points at 10% and 90% levels		250	ns
Tf	Clock Fall Time[5]	Test points at 10% and 90% levels		250	ns
Trvcc	Vcc Rise Time[5]	Test points at 10% and 90% levels		250	ms

DC Characteristics (Over Operating Range Specifications)

SYMBOL	PARAMETER	CONDITIONS	MIN	TYP	MAX	UNIT
Iil	Input Leakage	Vin = GND to Vcc			±10	µA
Ioz	Output Leakage	I/O = High Impedance Vo = GND to Vcc			±10	µA
Vil	Input Low Voltage		-0.3		0.8	V
Vih	Input High Voltage		2.0		Vcc+0.3	V
Vol	Output Low Voltage TTL	Iol = +8.0mA[12]			0.45	V
Volc	Output Low Voltage CMOS	Iol = 10µA[12]			0.1	V
Voh	Output High Voltage TTL	Ioh = -4.0mA[12]	2.4			V
Vohc	Output High Voltage CMOS	Ioh = -10µA[12]	Vcc -0.1			v

Capacitance

SYMBOL	PARAMETER	CONDITIONS	MIN	TYP	MAX	UNIT
Cin[3,7]	Input Capacitance	Frequency = 1MHz		4	6	pF
Cout[3,7]	Output Capacitance	Frequency = 1MHz		8	12	pF
Cclk[3,7]	Clk Pin Capacitance	Frequency = 1MHz		8	13	pF

Electrical Characteristics (Over Operating Range Specifications)

			PEEL 20CG10-25	
SYMBOL	PARAMETER	UNITS	MIN	MAX
Iccs	Vcc Current Standby[9]	mA		65
Icca	Vcc Current Active[9]	mA		Iccs + 0.5 mA/MHz
tPD	Input[4] to combinatorial output	ns		25
tOD	Input[4] to output disable[6]	ns		25
tOE	Input[4] to output enable[6]	ns		25
tSC	Input[4] set-up to clock	ns	15	
tHC	Input[4] hold after clock	ns	0	
tCH	Clock high time[5]	ns	13	
tCL	Clock low time[5]	ns	13	
tCO1	Clock to output	ns		15
tCO2	Clock to combinatorial output delay via registered feedback	ns		30
tCP	Minimum clock period tSC+tCO1	ns	30	
fmax1	Max clock freq(1/tSC+tCL)	MHz	35.7	
fmax2	Max clock freq (1/tCP)	MHz	33.3	
fmax3	Max clock freq (1/tCL+tCH)	MHz	38.5	
tAW	Async clear pulse width	ns	25	
tAP	Input[4] to asynchronous clear[11]	ns		25
tAR	Asynchronous reset recovery	ns		25
tRESET	Register power-on-reset[5]	µs		5

NOTES:

1. Minimum DC input is -0.5V; however, inputs may undershoot to -2.0V for periods less than 20 ns.
2. Voltage applied to input or output must not exceed Vcc + 1.0V.
3. These measurements are periodically sample tested.
4. "Input" refers to an Input signal.
5. Test points for Clock and Vcc in Tr, Tf, Trvcc, tCH, tCL, and tRESET are referenced at 10% and 90% levels.
6. See AC test point/load circuit table for tOE and tOD testing.
7. Typical values and capacitance are measured at Vcc=5.0V and Ta=25°C.
8. Exposure to absolute maximum ratings over extended periods of time may affect device reliability. Exceeding absolute maximum ratings may cause permanent damage.
9. I/O pins are open (no load).
10. Vin specified is not for program/verify operation. Contact AMI for information regarding PEEL program/verify specifications.
11. Minimum width required to ensure proper asynchronous clear operation and does not imply rejection of signal less than this value.
12. Contact factory for increased Iol requirements.

Figure 18: PEEL20CG10 AC Switching Waveforms

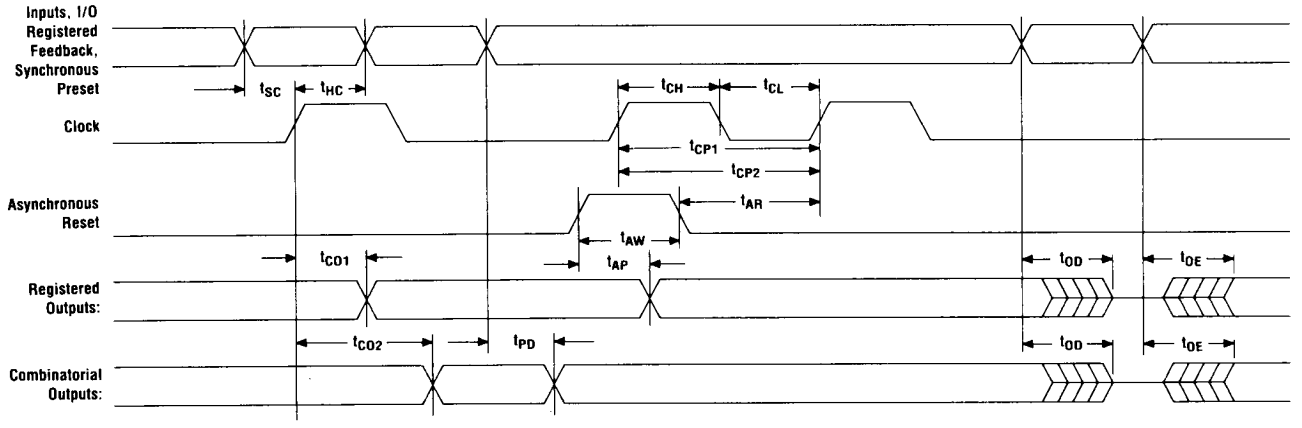
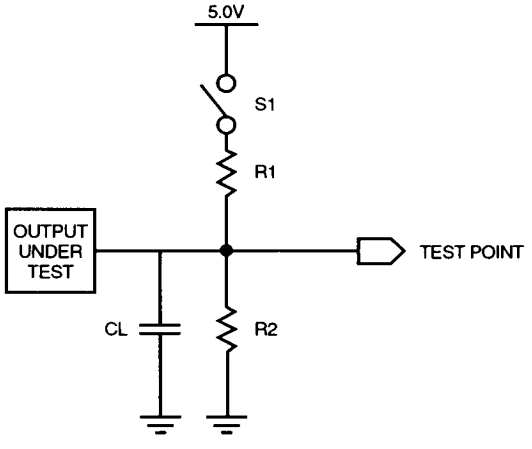


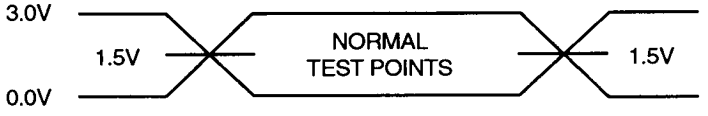
Figure 19: PEEL20CG10 AC Test Loads/Waveforms

AC Equivalent Load Circuit



TTL Levels	CMOS Levels
R1 = 448Ω	R1 = 480KΩ
R2 = 245Ω	R2 = 480KΩ

AC Testing Input/Output Waveform



AC Test Point/Load Circuit Table

AC Test	Test Point	CL	S1
NORMAL	1.5V	50pF	closed
tOE(Z→0)	VOH	50pF	open
tOE(Z→0)	VOL	50pF	closed
tOD(1→Z)	VOH–.5V	5pF	open
tOD(0→Z)	VOL+.5V	5pF	closed

Z=High Impedance