Military
Programmable
Array
Logic

PAL32VX10
PAL32VX10A

T-46-13-47

High Speed Programmable Array Logic
Conforms to MIL-STD-883, Class B*

DISTINCTIVE CHARACTERISTICS

- Increased logic power
  –Up to 32 inputs and 10 outputs
- Dual independent feedback paths allow buried state registers or input registers
- Programmable flip-flops allow J-K, S-R, T or D types for the most efficient use of product terms
- 10 input/output macrocells for flexibility
- Programmable registered or combinatorial outputs
- Individual user-programmable output polarity
- Global register asynchronous preset/synchronous reset or synchronous preset/asynchronous reset
- Total dose $1x10^6$ rads (Si)
- Dose rate $1x10^{10}$ rads/sec
- Automatic register reset on power up
- Preloadable output registers for testability
- Varied product term distribution
  –Up to 16 product terms per output
- High-speed
  –30 ns "A" version
  –35 ns standard version
- 300-mil SKINNYDIP® or surface-mount packaging available
- Programmed security fuse makes readout of logic pattern difficult to copy
- Pin-compatible functional superset of PAL22V10
- Instant prototyping/zero NRE charge
- Neutron fluence $1x10^{14}$ N/cm²

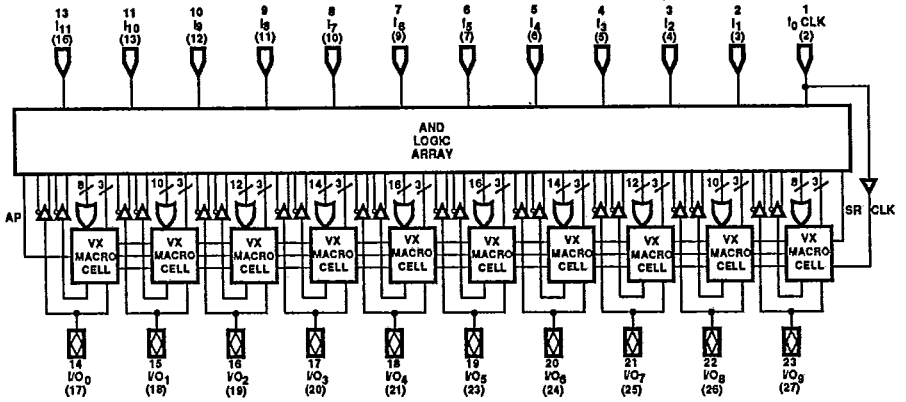
GENERAL DESCRIPTION

The PAL32VX10/A is a high-density Programmable Array Logic (PAL®) device which implements a sum-of-products transfer function via a user-programmable AND logic array and a fixed OR logic array. Featured are ten highly flexible input/output macrocells which are user-configurable for combinatorial or registered operation. Each flip-flop can be programmed to be either a J-K, S-R, T, or D-type for optimal design of state machines and other synchronous logic. In addition, a unique dual feedback architecture allows I/O capability for each macrocell in both combinatorial and registered configurations. This can be achieved even when register feedback is present, and allows implementation of buried flip-flops while preserving the external macrocell input. The PAL32VX10/A is supplied in a space-saving 300-mil-wide dual in-line package offering a powerful, space-saving alternative to SSI/MSI logic devices, while providing the advantage of instant prototyping. Security fuses defeat readout after programming and make proprietary designs difficult to copy.

The PAL32VX10/A is fabricated using Advanced Micro Devices' advanced oxide-isolated bipolar process for high speed and low power. TiW fuse links provide high reliability and programming yields. Preloadable output registers facilitate functional testing.

The PAL32VX10/A can be programmed on standard PAL device programmers, fitted with appropriate programming modules and configuration software. Design development is supported by AMD's PALASM® software as well as by other programmable logic CAD tools available from third-party vendors.

BLOCK DIAGRAM



Note: LCC pin numbers are indicated in parentheses. LCC pins 1, 8, 15, and 22 are not connected.

Monolithic Memories
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* Latest revision effect
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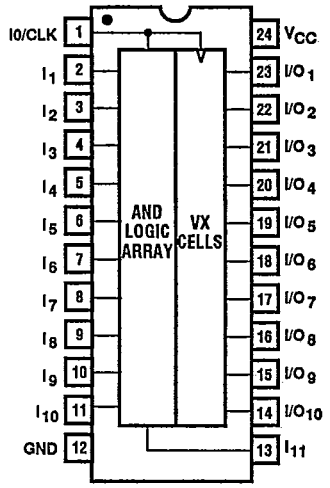
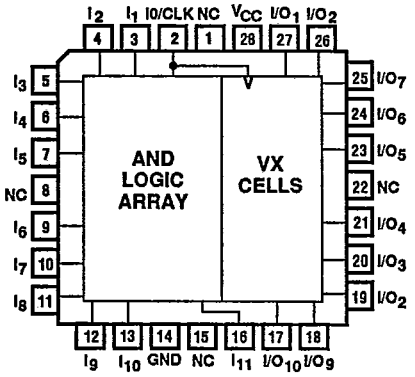
CONNECTION DIAGRAMS
(Top View)

Ceramic SKINNYDIP



LCC



Note: Pin 1 is marked for orientation.

Pin Designations: I = Input; I/O = Input/Output; OE = Output Enable; CLK = Clock; V_{CC} = Supply Voltage; GND = Ground

ORDERING INFORMATION

Standard Products

AMD/MMI standard products are available in several packages. The order number (Valid Combination) is formed by a combination of:

a. Device Number
b. Speed/Power Option
c. Operating Conditions
d. Package Type

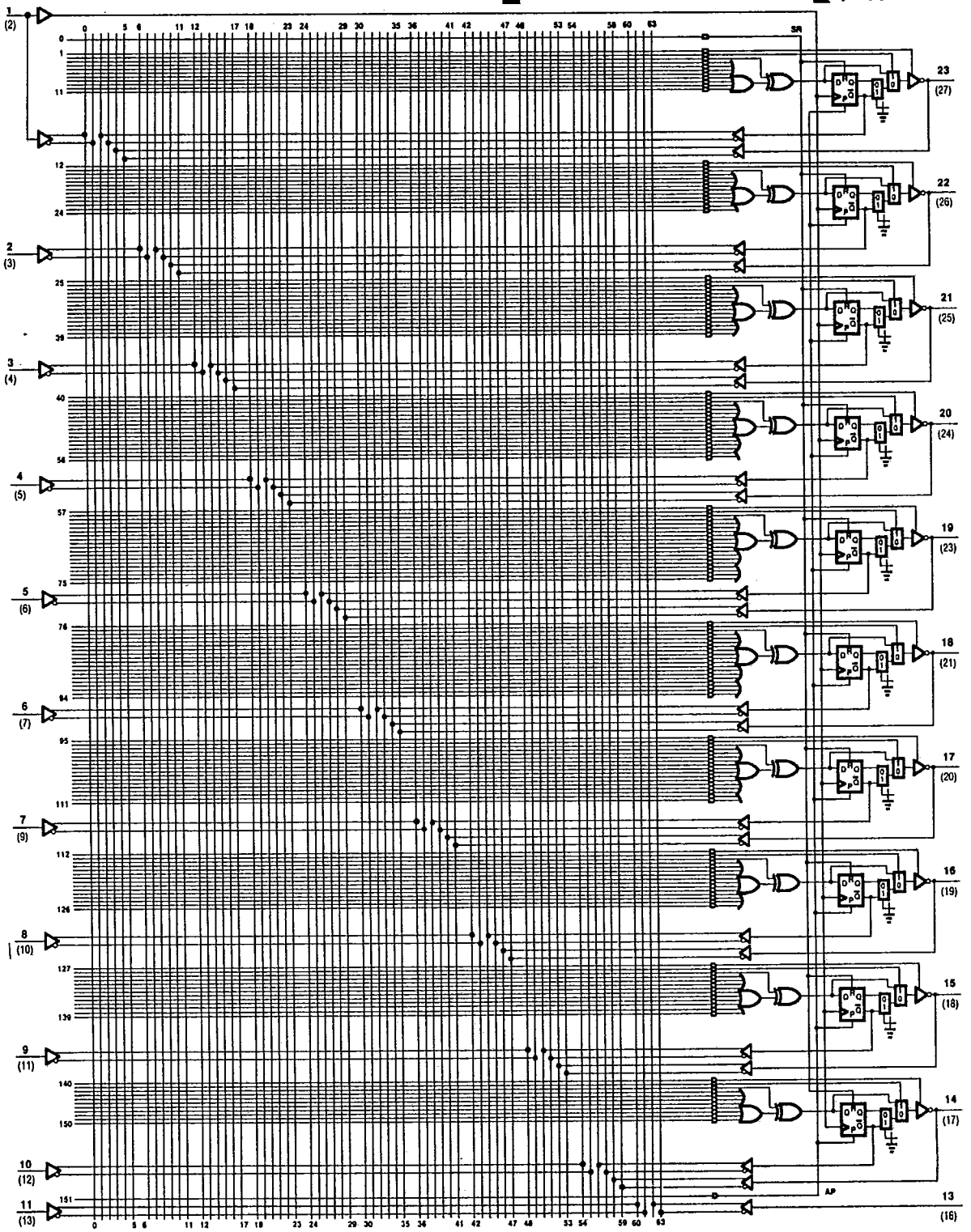
PAL 32 VX 10 A M JS /883B

- **a. PROGRAMMABLE ARRAY LOGIC**
- **NUMBER OF ARRAY INPUTS**
- **OUTPUT TYPE**
  VX = Varied terms with XOR
- **NUMBER OF OUTPUTS**
- **b. SPEED**
  Blank = Standard
  A = High Speed
- **c. TEMPERATURE RANGE**
  M = -55°C to +125°C
- **d. PACKAGE TYPE**
  JS = Ceramic SKINNYDIP
  L = Leadless Chip Carrier
  W = Cerpack
- **e. OPTIONAL PROCESSING**
  /883B = MIL-STD-Class B

MILITARY CASE OUTLINES (See Note)

Package Outline Letter	Conforms to MIL-M-38510 Appendix C Case Outline
JS	D-9
W	F-6
L	C-4

Note: Refer to MIL-M-38510 Appendix C for the appropriate package drawing.



PAL32VX10/A Logic Diagram

FUNCTIONAL DESCRIPTION

The PAL32VX10/A has twelve dedicated input lines and ten programmable I/O macrocells. Pin 1 serves either as an array input or as a clock for all flip-flops. Buffers for device inputs have complementary outputs to provide user-programmable input signal polarity. The fuse matrix implements a programmable AND logic array, which drives a fixed OR logic array.

The high level of flexibility built into each macrocell, shown in Figure 1, allows the PAL32VX10/A to implement over thirty different architecture options. Each macrocell can be individually programmed to implement a variety of combinatorial or registered logic functions.

DUAL OUTPUT FEEDBACK

Dual feedback paths associated with each macrocell provide independent feedback paths directly into the array from both the flip-flop output and the output pin. Unlike other devices which have a single feedback path, the PAL32VX10/A allows each output to have full I/O capability when configured as either a combinatorial output or a registered output, even if register feedback to the array is used. Thus registers can be loaded from their outputs.

If a macrocell is configured as a dedicated input, by disabling the three-state output buffer, the dual feedback architecture allows use of the associated register as an input register or as a "buried" state register, avoiding waste of the flip-flop, as shown in Figure 2.

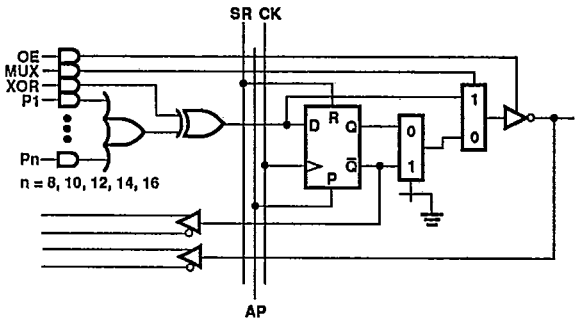


Figure 1. PAL32VX10/A Macrocell

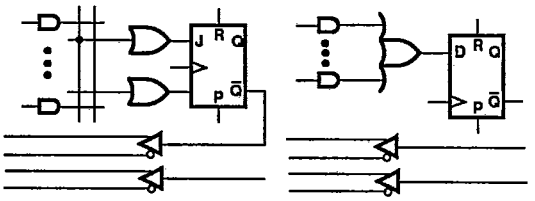


Figure 2. Buried Flip-Flops With Dedicated Inputs

PROGRAMMABLE FLIP-FLOPS

Each output macrocell contains a unique programmable flip-flop consisting of a basic D-type flip-flop driven by an XOR gate. This allows the user to choose the optimal flip-flop for the design, since either J-K, S-R, or T-type flip-flops can be synthesized from such a structure without wasting product terms.

As indicated in the macrocell logic diagram, one input of the XOR gate is connected to a single product term, while the second input is connected to the output of the OR logic array. The XOR gate output feeds the input of the D flip-flop. The way in which the XOR gate is used to synthesize the different flip-flop types is described in detail below.

D Flip-Flop. The D flip-flop option is implemented directly. In this configuration, the XOR gate on the input of the flip-flop can be used to program the logic polarity of the transfer function.

J-K Flip-Flop. The J-K flip-flop option can be easily synthesized with a more sophisticated manipulation of the XOR gate inputs and the D flip-flop output.

The transfer function of a J-K flip-flop can be mapped in the Karnaugh map of Figure 3, where Q+ represents the next state of the flip-flop:

J K \ Q	0	1	Q+
0 0	0	(1)	(HOLD)
0 1	0	0	(RESET)
1 1	(1)	0	(TOGGLE)
1 0	(1)	(1)	(SET)

Figure 3. J-K Flip-Flop Transfer Function

Dropping the (+) for simplicity, the equivalent Boolean expression for Q+ is:

$$Q := \overline{K}*Q + J*\overline{Q}$$

In general, J and K can be sum-of-product expressions which are provided in the PAL architecture only in active-high form. Thus, a direct implementation of $\overline{K}$ expressions must invoke a DeMorgan transformation, which can use excessive product terms. This can be avoided by rewriting the equation for Q without inversion on the J or K inputs.

The XOR gate can be used to construct a logically equivalent expression without any inversions on the J or K inputs. The rewritten Boolean expression is:

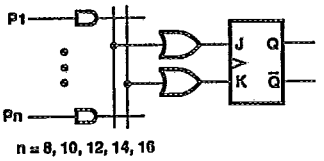
$$Q := Q :+: (J*\overline{Q} + K*Q)$$

To check that these expressions are logically equivalent, change the XOR to its equivalent sum-of-products form (remember $A :+: B = A*\overline{B} + \overline{A}*B$) and reduce (using DeMorgan's theorem):

$$Q := Q*\overline{(J*\overline{Q} + K*Q)} + \overline{Q}*(J*\overline{Q} + K*Q)$$
$$Q := Q*(\overline{J} + Q)*(\overline{K} + \overline{Q}) + \overline{Q}*J*\overline{Q} + \overline{Q}*K*Q$$
$$Q := Q*(\overline{J}*\overline{K} + \overline{J}*\overline{Q} + Q*\overline{K} + Q*\overline{Q}) + J*\overline{Q}$$
$$Q := \overline{J}*\overline{K}*Q + \overline{K}*Q + J*\overline{Q}$$

which simplifies to $Q := \overline{K}*Q + J*\overline{Q}$

Since J and K are, in general, sums of products, J and K in either expression can be substituted with (J1 + J2 + ... + Jm) and (K1 + K2 + ... + Kn-m), where n is the total number of product terms associated with a given output macrocell. Thus, the total n-product term resource is shared between the J and K control inputs (Figure 4). Note that all J terms will contain $\overline{Q}$ and all K terms will contain Q.



n = 8, 10, 12, 14, 16

Figure 4. J-K Flip-Flop Logic Equivalent; J and K Can Also Be Active-Low

The above discussions have assumed that it was most convenient to "group ones" in the Karnaugh map. Sometimes it takes fewer product terms to "group zeros", i.e., implement the inversion of the desired function. The equations shown in Table 1 are equivalent and can be interchanged to optimize product term utilization. This can be readily proved through logic reductions similar to that above.

J and K active high	$Q := Q :+: (J*\overline{Q} + K*Q)$
J active high, K active low	$Q := J*\overline{Q} + \overline{K}*Q$
J active low, K active high	$\overline{Q} := \overline{J}*\overline{Q} + K*Q$
J and K active low	$Q := \overline{Q} :+: (\overline{J}*\overline{Q} + \overline{K}*Q)$

Note: J = sum of products J1 + J2 + ... + Jm
K = sum of products K1 + K2 + ... + Kn-m
n = total number of available product terms for a given macrocell (8 to 16)

Table 1. J-K Flip-Flop Transfer Functions

S-R Flip-Flop. The S-R flip-flop has a truth table identical to that of the J-K flip-flop, with the exception that the J=K=1 (toggle) condition is not allowed. The S-R flip-flop implementation is identical to that of the J-K flip-flop, with J-K replaced by S-R, and the S=R=1 condition avoided.

T Flip-Flop. A T (toggle) flip-flop either holds its state or toggles, depending on the logic state of the T input. The T flip-flop is a subset of the J-K flip-flop and can be considered equivalent to a J-K type with J=K. The general transfer function and its active-low T equivalent are both given in Table 2.

$Q := Q :+: T$
$Q := \overline{Q} :+: \overline{T}$

Note: T = sum of products T1 + T2 + T3 + ... + Tn

Table 2. T Flip-Flop Transfer Functions

SUMMARY

The PAL32VX10/A can synthesize J-K, S-R, T, and D flip-flops, whichever is most convenient for the application, without sacrificing products terms. Additionally, the synthesized equations can use the active-high or active-low forms of the inputs, allowing the designer to minimize product term requirements.

FLIP-FLOP BYPASS

Any output in the PAL32VX10/A can be configured to be combinatorial by bypassing the output flip-flop. This is done by setting the output multiplexer to the appropriate state. The multiplexer is controlled by a product term which can be set unconditionally for a permanent combinatorial (all fuses opened, product term high) or registered (all fuses intact, product term low) output configuration, or can be programmed to bypass the output flip-flop "on the fly" allowing signals to be routed directly to output pins under user-specified conditions.

VARIED PRODUCT TERM DISTRIBUTION

An increased number of product terms has been provided in the PAL32VX10/A over previous generation PAL devices. These terms are distributed among the ten macrocells in a varied manner, ranging from eight to sixteen terms per output. The five output pairs have 8, 10, 12, 14, or 16 product terms available for the OR gate within each macrocell. In addition, each macrocell has one XOR product term and two architecture control product terms.

PROGRAMMABLE I/O

Each macrocell has a three-state output buffer with programmable three-state control. Control is implemented by a single product term, allowing specification of enable/disable functions controlled by any device input or output. Each macrocell can be configured as a dedicated input by disabling the buffer drive capability. When this is done, the associated register can still be used as an input register or buried state register, due to the independent register feedback path.

PROGRAMMABLE PRESET AND RESET

The ten macrocell flip-flops share common programmable preset and reset control for easy system initialization. The Q outputs of the register will go to the logic low state following a low-to-high transition on pin 1 (I0/CLK) when the synchronous reset (SR) product term is asserted. The register will be forced to the logic high state independent of the clock when the asynchronous preset (AP) product term is asserted.

PROGRAMMABLE POLARITY

The polarity of each macrocell output can be set active high or active low.

Combinatorial Outputs. The XOR gate provides polarity control for combinatorial outputs, with the single product term to the XOR gate controlling the invert/not invert function. With all fuses intact, there is no inversion through the XOR gate, creating an active low output. Opening all fuses forces the product term high, inverting data and creating an active high output.

Registered Outputs. Output polarity for registered outputs can be determined in two ways. For D-type registered outputs, polarity can be set by the XOR gate, as is the case with combinatorial outputs. Using this method to set polarity, preset and reset will not be affected.

Polarity, as observed from the output pin, can also be determined by the flip-flop output multiplexer. Note that this does not affect the polarity of the register feedback signal, but does affect preset and reset. By changing the flip-flop output multiplexer, the preset and reset functions are exchanged relative to the controlling product terms.

With the multiplexer fuse intact, the Q output is routed to the output pin, configuring an active low output. With the multiplexer fuse opened, $\overline{Q}$ is routed to the output pin and synchronous reset becomes synchronous preset. Similarly, asynchronous reset becomes asynchronous preset.

Polarity options for J-K, S-R, and T flip-flops have been discussed in the section on programmable flip-flops.

POWER-UP PRESET

All flip-flops power up to a logic high for predictable system initialization. Outputs of the PAL32VX10/A will be high or low depending on the state of the register output multiplexers.

REGISTER PRELOAD

The register on the PAL32VX10/A can be preloaded to facilitate functional testing of complex state machine designs. This feature allows direct loading of arbitrary states, thereby making it unnecessary to cycle through long test vector sequences to reach a desired state. In addition, transitions from illegal states can be verified by loading in illegal states and observing proper recovery.

SECURITY FUSE

After programming and verification, a PAL32VX10/A design can be secured by programming the security fuses. Once programmed, these fuses defeat readback of the internal fuse pattern by a device programmer, making proprietary designs very difficult to copy.

QUALITY AND TESTABILITY

The PAL32VX10/A offers a very high level of built-in quality. Special on-chip test circuitry provides a means of verifying performance of all AC and DC parameters prior to programming. In addition, these built-in test paths verify complete functionality of each device to provide the highest post-programming functional yields in the industry.

ABSOLUTE MAXIMUM RATINGS

	Operating	Programming
Supply voltage V_{CC}	-0.5 V to 7.0 V	-0.5 V to 12 V
Input voltage	-1.5 V to 5.5 V	-1.0 V to 12 V
Off-state output voltage	5.5 V	12 V
Storage temperature	-65°C to +150°C	

Stresses above those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent device failure. Functionality at or above these limits is not implied. Exposure to absolute maximum ratings for extended periods may affect device reliability.

Operating ranges define those limits between which the functionality of the device is guaranteed.

OPERATING CONDITIONS

Parameter Symbol	Parameter Description		Military (Note 3) STD Min.	STD Max.	A Min.	A Max.	Unit
V_{CC}	Supply voltage		4.5	5.5	4.5	5.5	V
V_{IL}	Static D.C. low-level input voltage (Note 2)			≤0.8		≤0.8	V
V_{IH}	Static D.C. high-level input voltage (Note 2)		≥2.0		≥2.0		V
t_w	Width of clock (Note 1)	Low	25		23		ns
		High	25		23		
t_{su}	Setup time from input or feedback to clock	Product terms P_1-P_n, SR	35		30		ns
		Product term XOR	40		35		
t_h	Hold time (Note 1)		0		0		ns
t_{aw}	Asynchronous preset width (Note 1)		35		30		ns
t_{ar}	Asynchronous preset recovery time (Note 1)		35		30		ns
t_{sr}	Synchronous reset recovery time (Note 1)		35		30		ns
T_A	Operating free-air temperature		-55		-55		°C
T_C	Operating case temperature			125		125	°C

Notes: Virgin array verify of an unprogrammed PAL device is performed at 25°C only.
1. These are device set-up conditions which are measured during initial qualification and are not directly tested.
2. These are absolute voltage levels with respect to the ground pins on the device and include all overshoots due to system or tester noise. Do not attempt to test these values without suitable equipment.
3. For commercial specifications, contact Advanced Micro Devices.

DC CHARACTERISTICS Over operating conditions. (Note 1)

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Parameter Symbol	Parameter Description	Test Conditions		Min.	Typ.	Max.	Unit
V_{IC}	Input Clamp Voltage	V_{CC} = Min.	I_I = -18 mA			-1.5	V
I_{IL}	Low-Level Input Current (Note 1)	V_{CC} = Max.	V_I = 0.4 V			-0.25	mA
I_{IH}	High-Level Input Current (Note 1)	V_{CC} = Max.	V_I = 2.4 V			25	µA
I_I	Maximum Input Current	V_{CC} = Max.	V_I = 5.5 V			200	µA
V_{OL}	Low-Level Output Voltage	V_{CC} = Min.	I_{OL} = 12 mA			0.5	V
V_{OH}	High-Level Output Voltage	V_{CC} = Min.	I_{OH} = -2 mA	2.4			V
I_{OZL}	Off-State Output Current (Note 1)	V_{CC} = Max.	V_O = 0.4 V			-100	µA
I_{OZH}			V_O = 2.4 V			100	µA
I_{OS}	Output Short-Circuit Current (Note 2)	V_{CC} = 5 V	V_O = 0.5 V	-30		-130	mA
I_{CC}	Supply Current	V_{CC} = Max.				180	mA
C_{IN}	Input Capacitance	V_{IN} = 2.0 V at f = 1 MHz			11		pF
C_{OUT}	Output Capacitance	V_{OUT} = 2.0 V at f = 1 MHz			15		pF

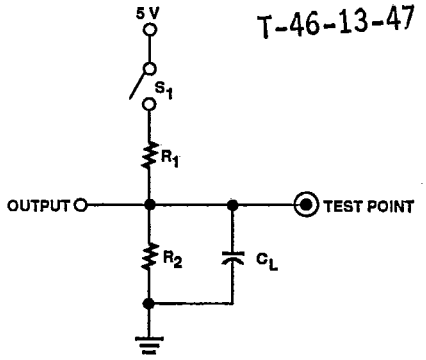
Notes: 1. Programmed devices conform to Mil-Std-883, Method 5005, Group A, Subgroups 1, 2, 3, 7, 8, 9, 10, and 11.
2. I/O pin leakage is the worst case of I_{IL} and I_{OZL} (or I_{IH} and I_{OZH}).
3. No more than one output should be tested at a time. Duration of the short circuit should not exceed one second.

SWITCHING CHARACTERISTICS Over operating conditions. (Note 1)

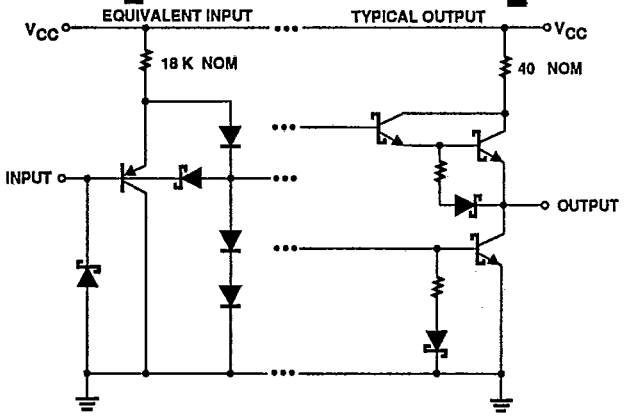
Parameter Symbol	Parameter Description			Test Conditions	STD Min.	STD Max.	A Min.	A Max.	Unit
t_{PD}	Input or Feedback to Output		Product Terms P_1-P_n	R_1 = 390 Ω, R_2 = 750 Ω		35		30	ns
			Product Term XOR			40		35	
t_{CLK}	Clock to Output or Feedback					20		20	ns
t_{PZX}	Input to Output Enable					35		30	ns
t_{PXZ}	Input to Output Disable					35		30	ns
t_{AP}	Asynchronous Preset to Output					35		30	ns
t_{CR}	Input or Feedback to Registered Output from Combinatorial Configuration					95		95	ns
t_{RC}	Input or Feedback to Combinatorial Output from Registered Configuration					95		95	ns
f_{MAX}	Maximum Frequency (Note 2)	Feedback ($1/t_{P1}$)	Product Terms P_1-P_n		18		20		MHz
			Product Term XOR		16.7		18		
		No Feedback ($1/t_{P2}$)			20		21.7		

Notes: 1. Programmed devices conform to Mil-Std-883, Method 5005, Group A, Subgroups 1, 2, 3, 7, 8, 9, 10, and 11.
2. f_{MAX} is calculated and measured on initial qualifications only.
f_{MAX} (state machine) = $1/[t_{SU} + t_{CLK}]$.
f_{MAX} (data path register) = $1/[t_{WL} + t_{WH}]$ or $1/[t_{SU} + t_H]$, whichever is smaller.

SWITCHING TEST CIRCUIT

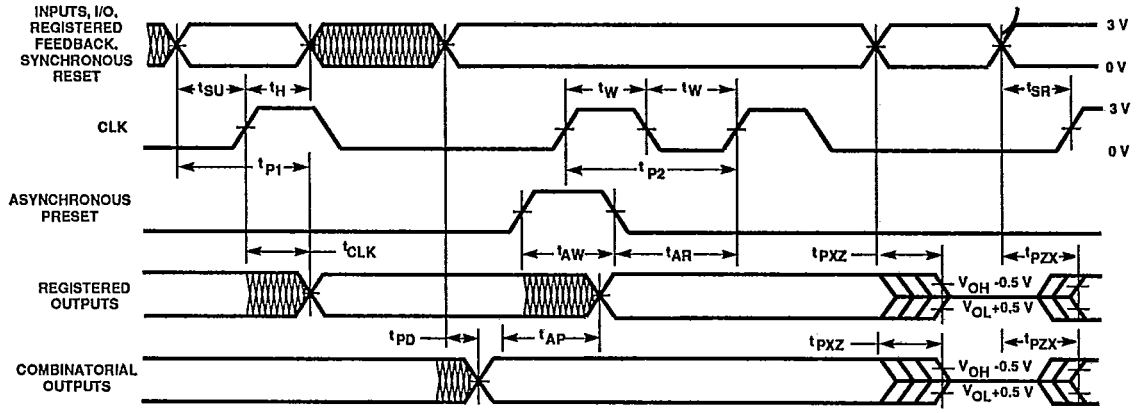


SCHEMATIC OF INPUTS AND OUTPUTS



Notes: 1. t_{PD} is tested with switch S_1 closed. C_L = 50 pF and measured at 1.5 V output level.
2. t_{PZX} is measured at the 1.5 V output level with C_L = 50 pF. S_1 is open for high impedance to "1" test, and closed for high impedance to "0" test.
3. t_{PXZ} is tested with C_L = 5 pF. S_1 is open for "1" to high impedance test, measured at V_{OH} -0.5 V output level: S_1 is closed for "0" to high impedance test measured at V_{OL} +0.5 V output level.
4. Equivalent test loads may be used on automatic test equipment.

SWITCHING WAVEFORMS



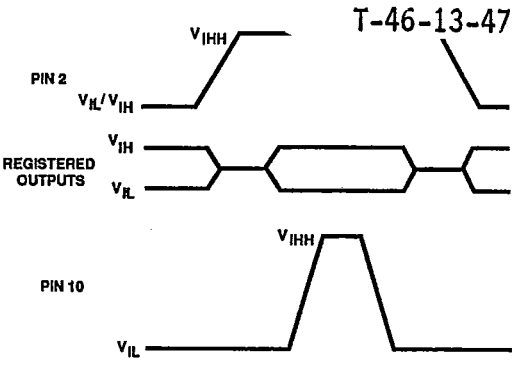
Notes: 1. V_T = 1.5 V
2. Input rise and fall times 2-5 ns typical.

OUTPUT REGISTER PRELOAD

The PRELOAD function allows the register to be loaded from the output pins. This feature aids functional testing of sequential designs by allowing direct setting of output states. The procedure is as follows:

1. Raise V_{CC} to 4.5 V.
2. Disable output registers by setting pin 2 to V_{IHH} (12 V).
3. Apply the desired value (V_{IL}/V_{IH}) to all registered output pins. Leave combinatorial outputs floating.
4. Pulse pin 10 to V_{IHH}, then back to 0 V.
5. Remove V_{IL}/V_{IH} from all registered output pins.
6. Remove high voltage from pin 2.
7. Enable output registers per programmed pattern.
8. Verify for V_{OL}/V_{OH} at all registered output pins.

Note: V_{IHH} = 11.0 (Min.), 11.5 (Typ.) and 12.0 (Max.).



KEY TO SWITCHING WAVEFORMS

WAVEFORMS	INPUTS	OUTPUTS
	DON'T CARE; MAY CHANGE PERMITTED	CHANGING; STATE UNKNOWN
	DOES NOT APPLY	CENTER LINE IS HIGH IMPEDANCE STATE
	MUST BE STEADY	WILL BE STEADY

f_{MAX} PARAMETERS

The parameter f_{MAX} is the maximum speed at which the PAL device is guaranteed to operate. Because flexibility inherent to PAL devices allows a choice of clocked flip-flop designs, for the convenience of the user, f_{MAX} is specified to address two major classes of synchronous designs.

The simplest type of synchronous design can be described as a data path application. In this case, data is presented to the data terminal of the flip-flop and clocked through; no feedback is employed (Figure 1). Under these conditions, the frequency of operation is limited by the greater of the data setup time (t_{SU}) or the minimum clock period (t_W high + t_W low, or t_{P2}). This parameter is designated f_{MAX} (no feedback).

For synchronous sequential designs, i.e., state machines, where logical feedback is required, inputs to flip-flop data terminals originate from the device input pins or flip-flop outputs via the internal feedback paths (Figure 2). Under these conditions, f_{MAX} is defined as the reciprocal of ($t_{SU} + t_{CLK}$), or t_{P1}, and is designated f_{MAX}

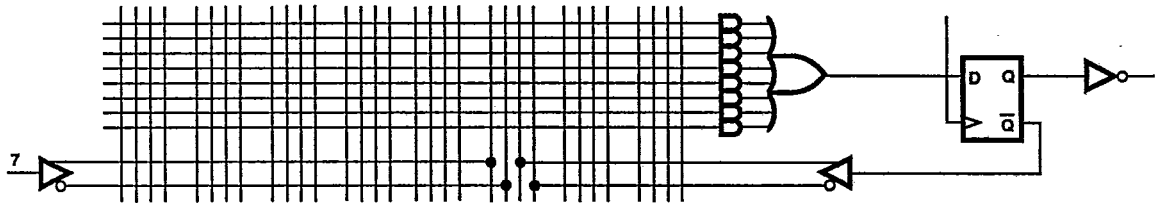


Figure 1. Data Path Register Configuration Without Feedback, Q: = I

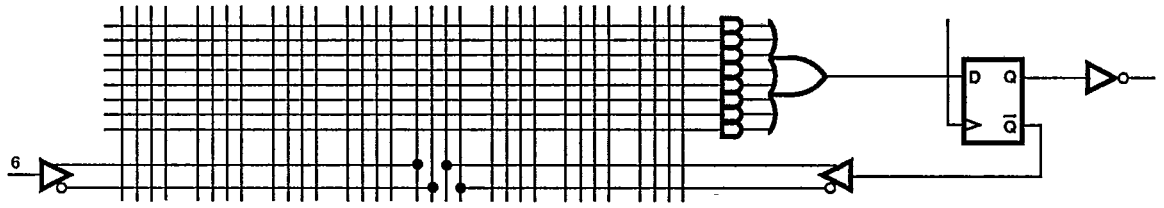


Figure 2. State Machine Configuration With Feedback, Q: = I + $\overline{Q}$

USE OF XOR PRODUCT TERM

The speed of the PAL32VX10/A is specified according to the use of the Exclusive-OR (XOR) product term in the macrocell. Note that the macrocell data input is a function of the two-input XOR gate, whose inputs are the OR of the product terms P_1-P_n and the single additional XOR product term (Figure 3).

The specification for the path through the single XOR product term is 5 ns slower than through the P_1-P_n product terms and the OR gate. As a result, if the single XOR product term is changing, the macrocell data input will not be available until 5 ns later than if only the P_1-P_n product terms were changing.

This difference between paths affects t_{PD}, t_{SU} and f_{MAX} (feedback). As a result, these three parameters are specified both for only the P_1-P_n product terms changing ("Product terms P_1-P_n") and with the single XOR product term changing ("Product term XOR") (Figure 4).

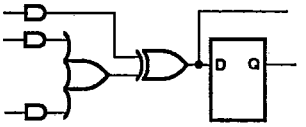
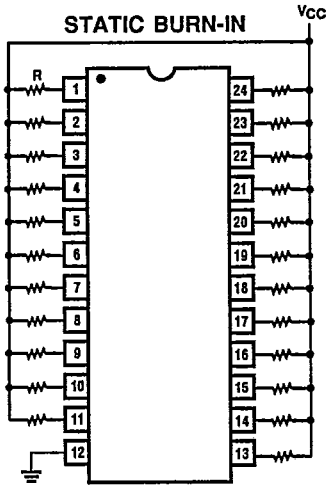


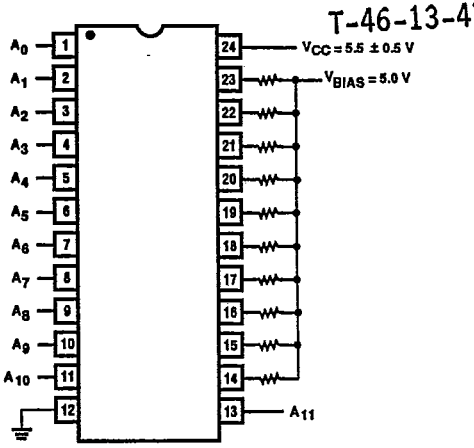
Figure 3.

Specification		Explanation
t_{PD}, t_{SU}, f_{MAX} (feedback)	Product Terms P_1-P_n	If only the P_1-P_n product terms are changing (XOR term is not changing)
	Product Term XOR	If XOR term is changing

STATIC BURN-IN



DYNAMIC BURN-IN



Note: R = 330 Ω ±5%

$T_{ambient}$ = 125°C
V_{CC} = 5.5 V ±0.5 V
Square wave pulses on A_0 to A_{11} are:

1. 50% ±15% duty cycle
2. Logic "0" = -1 V to 0.7 V
3. Logic "1" = 2.4 V to V_{CC}
4. Frequency of each address is to be one-half of each preceeding input, with A_0 beginning at 100 kHz
   e.g., A_0 = 100 kHz
   A_1 = 50 kHz ±10%
   A_2 = 25 kHz ±10%
   A_n = 1/2 A_{n-1} ±10%

The PAL32VX10/A can be programmed to function as one of the following System Building Blocks/HMSI™ devices:

Function	HMSI Part Number	f_{MAX} MHz	t_{pd} ns	PAL32VX10 f_{MAX} MHz	PAL32VX10A f_{MAX} MHz
8-Bit Shift Register	SN54LS498	10.5	–	16.7	18
Multifunction 8-Bit Register	SN54LS380	10.5	–	16.7	18
16:1 Multiplexer	SN54LS450	–	45	35	30
Dual 8:1 Multiplexer	SN54LS451	–	45	35	30
Quad 4:1 Multiplexer	SN54LS453	–	45	35	30

Note: Both the HMSI and PAL32VX10A devices are available in the same device packaging.

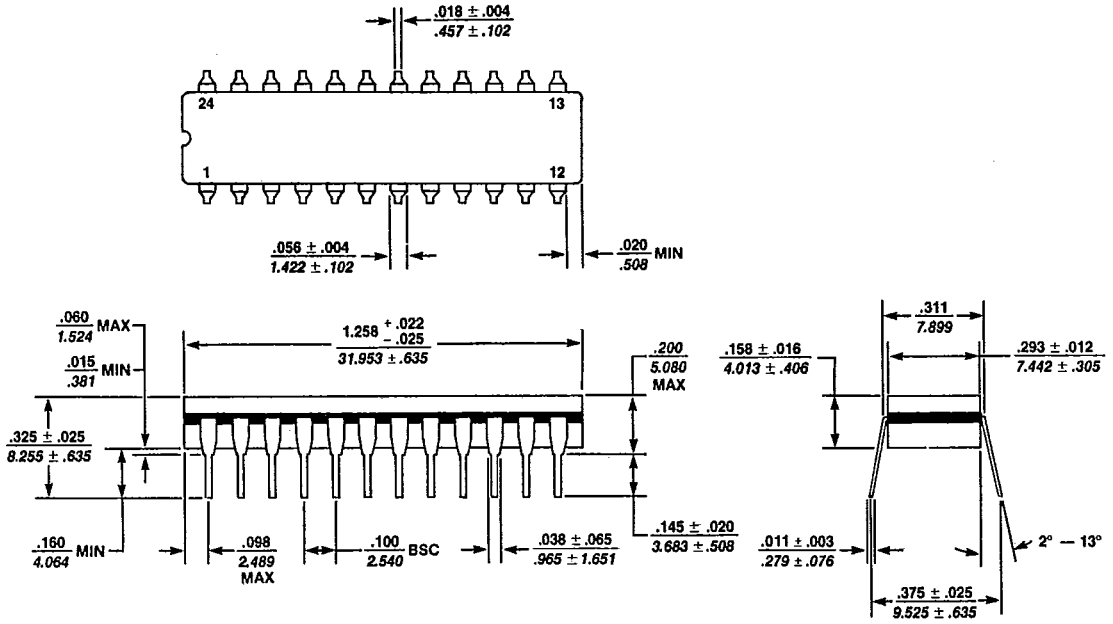
AMD Packaging	Mil-M-38510 Appendix C Case Outline
24JS (Ceramic DIP)	D-9
24W (Cerpack)	F-6
(28)L (Leadless Chip Carrier) (See Note)	C-4

Note: Reconnect pinout scheme is 1, 8, 15, and 22

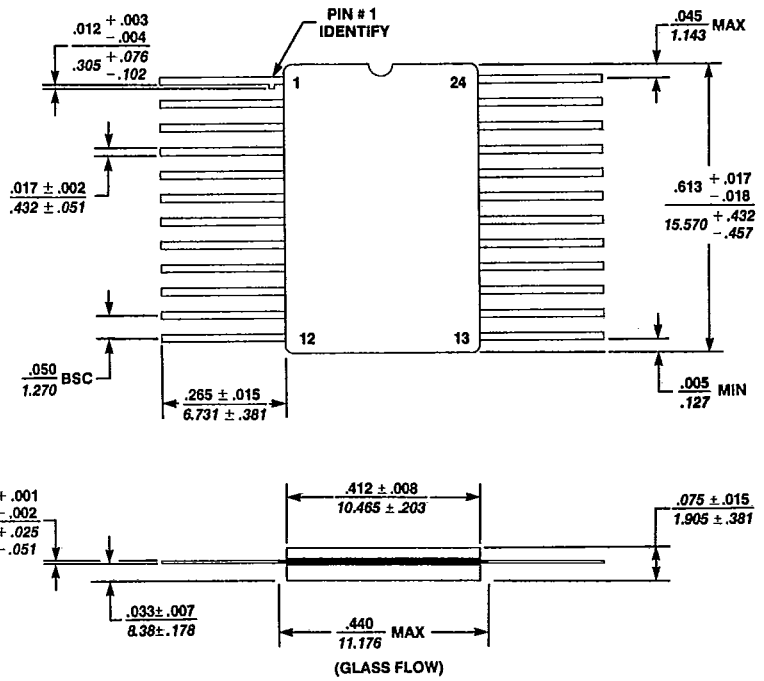
PHYSICAL DIMENSIONS

24JS CERAMIC DIP

T-46-13-47



24W CERPACK

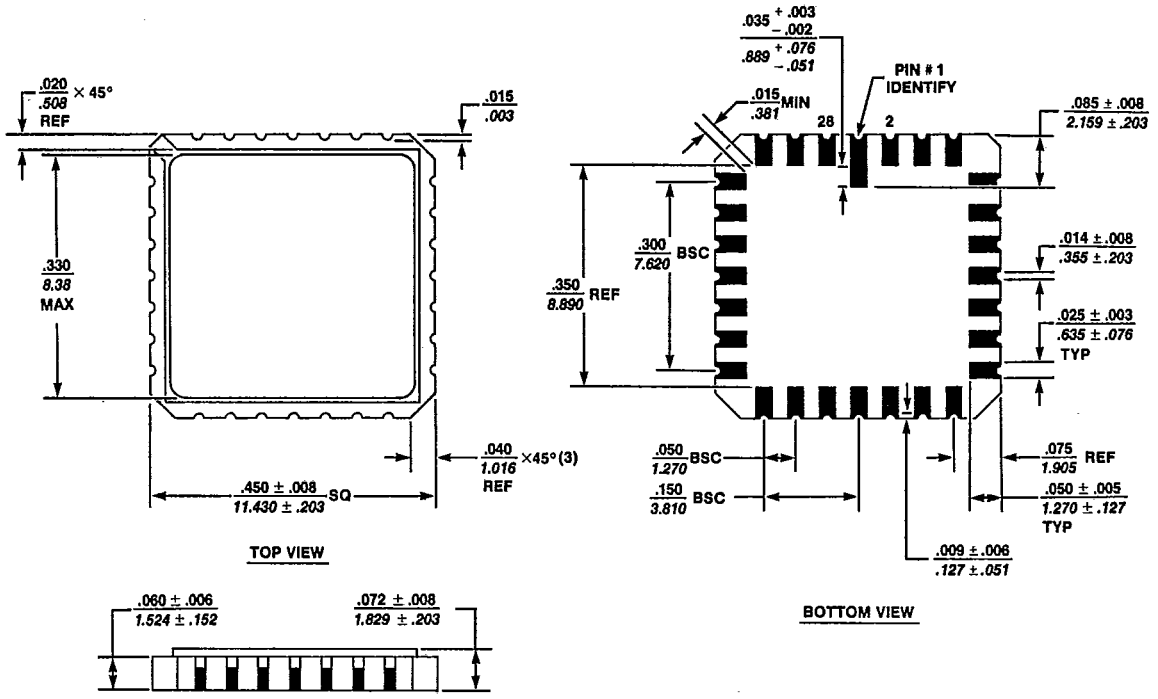


(GLASS FLOW)

UNLESS OTHERWISE SPECIFIED:
ALL DIMENSIONS MIN.-MAX. IN INCHES
ALL DIMENSIONS MIN.-MAX. IN MILLIMETERS
ALL TOLERANCES ARE ±.007 INCHES

PHYSICAL DIMENSIONS
28L LEADLESS CHIP CARRIER

T-46-13-47



UNLESS OTHERWISE SPECIFIED:
ALL DIMENSIONS MIN.-MAX. IN INCHES
ALL DIMENSIONS MIN.-MAX. IN MILLIMETERS
ALL TOLERANCES ARE ± .007 INCHES