OKI Semiconductor

# MSM56V16160F

**2-Bank × 524,288 Word × 16 Bit SYNCHRONOUS DYNAMIC RAM**

## DESCRIPTION

The MSM56V16160F is a 2-Bank × 524,288-word × 16 bit Synchronous dynamic RAM, fabricated in OKI's CMOS silicon-gate process technology. The device operates at 3.3V. The inputs and outputs are LVTTL compatible.

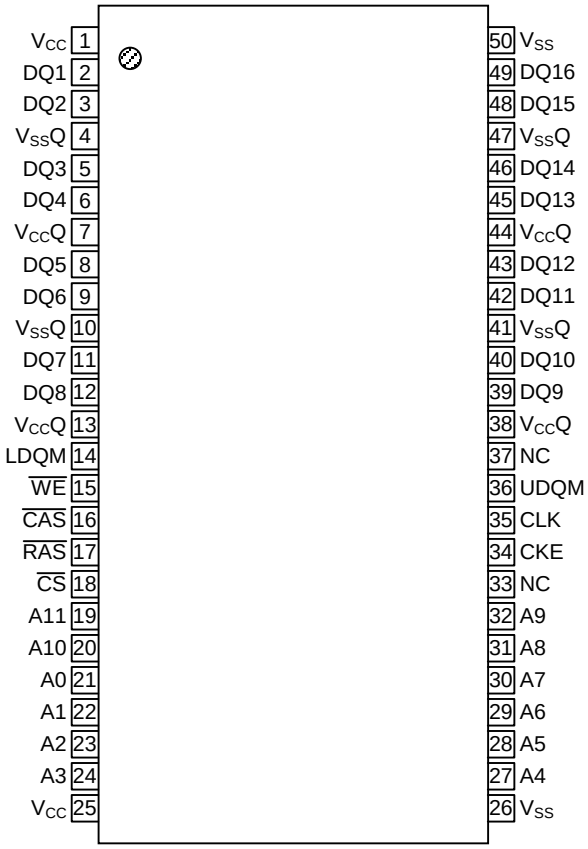
## FEATURES

- Silicon gate , quadruple polysilicon CMOS , 1-transistor memory cell
- 2-bank × 524,288-word × 16bit configuration
- 3.3V power supply ± 0.3V tolerance
- Input : LVTTL compatible
- Output : LVTTL compatible
- Refresh : 4096 cycles/64 ms
- Programmable data transfer mode
  - $\overline{\text{CAS}}$ Latency (1,2,3)
  - Burst Length (1,2,4,8,Full page)
  - Data scramble (sequential , interleave)
- CBR auto-refresh, Self-refresh capability
- Package:
  50-pin 400mil plastic TSOP (Type II) (TSOPII50-P-400-0.80-K) (Product : MSM56V16160F-xxTS-K)
  xx : indicates speed rank.

## PRODUCT FAMILY

| Family | Max. Frequency | Access Time (Max.) | |
|---|---|---|---|
| | | $t_{AC2}$ | $t_{AC3}$ |
| MSM56V16160F-8 | 125MHz | 9ns | 6ns |
| MSM56V16160F-10 | 100MHz | 9ns | 9ns |

## PIN CONFIGRATION (TOP VIEW)




50-Pin Plastic TSOP (II)
(K Type)

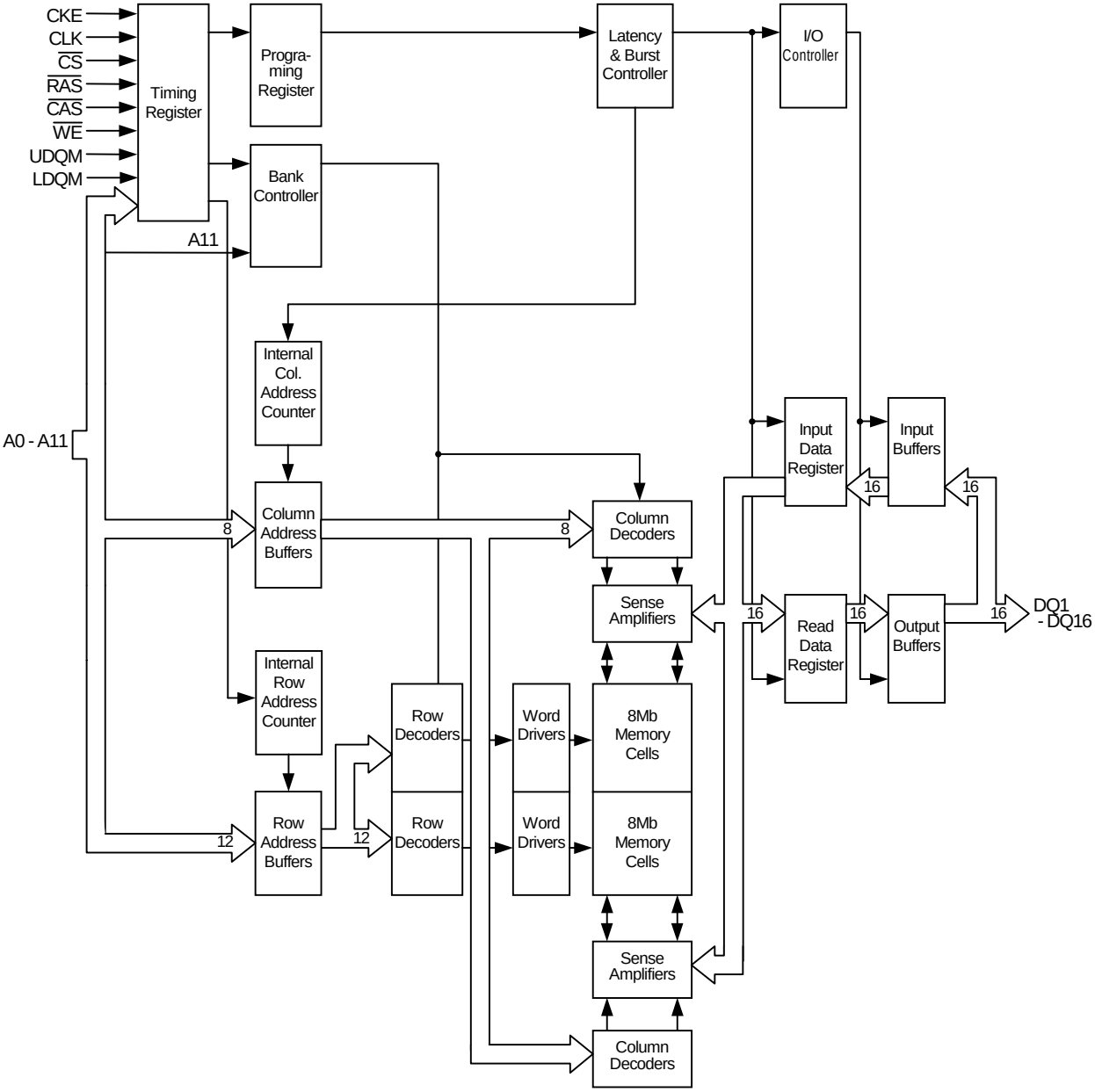
| Pin Name | Function | Pin Name | Function |
|---|---|---|---|
| CLK | System Clock | UDQM, LDQM | Data Input/Output Mask |
| $\overline{CS}$ | Chip Select | DQi | Data Input/Output |
| CKE | Clock Enable | $V_{CC}$ | Power Supply (3.3V) |
| A0–A10 | Address | $V_{SS}$ | Ground (0V) |
| A11 | Bank Select Address | $V_{CC}Q$ | Data Output Power Supply (3.3V) |
| $\overline{RAS}$ | Row Address Strobe | $V_{SS}Q$ | Data Output Ground (0V) |
| $\overline{CAS}$ | Column Address Strobe | NC | No Connection |
| $\overline{WE}$ | Write Enable | | |

Note: The same power supply voltage must be provided to every $V_{CC}$ pin and $V_{CC}Q$ pin.
The same GND voltage level must be provided to every $V_{SS}$ pin and $V_{SS}Q$ pin.

## PIN DESCRIPTION

| | |
|---|---|
| CLK | Fetches all inputs at the “H” edge. |
| $\overline{CS}$ | Disables or enables device operation by asserting or deactivating all inputs except CLK, CKE, UDQM and LDQM. |
| CKE | Masks system clock to deactivate the subsequent CLK operation.<br>If CKE is deactivated, system clock will be masked so that the subsequent CLK operation is deactivated. CKE should be asserted at least one cycle prior to a new command. |
| Address | Row & column multiplexed.<br>Row address : RA0 – RA10<br>Column Address : CA0 – CA7 |
| A11 | Slects bank to be activated during row address latch time and selects bank for precharge and read/write during column address latch time. A11=”L” : Bank A, A11=”H” : Bank B |
| $\overline{RAS}$<br>$\overline{CAS}$<br>$\overline{WE}$ | Functionality depends on the combination. For details, see the function truth table. |
| UDQM,<br>LDQM | Masks the read data of two clocks later when UDQM and LDQM are set “H” at the “H” edge of the clock signal. Masks the write data of the same clock when UDQM and LDQM are set “H” at the “H” edge of the clock signal. UDQM controls upper byte and LDQM controls lower byte. |
| DQi | Data inputs/outputs are multiplexed on the same pin. |

## BLOCK DIAGRAM



# ELECTRICAL CHARACTERISTICS

## Absolute Maximum Ratings

(Voltages referenced to $V_{SS}$)

| Parameter | Symbol | Rating | Unit |
|---|---|---|---|
| Voltage on Any Pin Relative to $V_{SS}$ | $V_{IN}$, $V_{OUT}$ | −0.5 to $V_{CC}$ + 0.5 | V |
| $V_{CC}$ Supply Voltage | $V_{CC}$, $V_{CC}Q$ | −0.5 to 4.6 | V |
| Storage Temperature | $T_{stg}$ | −55 to 150 | °C |
| Power Dissipation | $P_D$* | 600 | mW |
| Short Circuit Current | $I_{OS}$ | 50 | mA |
| Operating Temperature | $T_{opr}$ | 0 to 70 | °C |

*: Ta = 25°C

## Recommended Operating Conditions

(Voltages referenced to $V_{SS}$ = 0V)

| Parameter | Symbol | Min. | Typ. | Max. | Unit |
|---|---|---|---|---|---|
| Power Supply Voltage | $V_{CC}$, $V_{CC}Q$ | 3.0 | 3.3 | 3.6 | V |
| Input High Voltage | $V_{IH}$ | 2.0 | — | $V_{CC}$ + 0.2 | V |
| Input Low Voltage | $V_{IL}$ | −0.3 | — | 0.8 | V |

## Capacitance

($V_{BIAS}$ = 1.4V, Ta = 25°C, f = 1MHz)

| Parameter | Symbol | Min. | Max. | Unit |
|---|---|---|---|---|
| Input Capacitance (CLK) | $C_{CLK}$ | 2.5 | 4 | pF |
| Input Capacitance ($\overline{RAS}$, $\overline{CAS}$, $\overline{WE}$, $\overline{CS}$, CKE, UDQM, LDQM, A0-A11) | $C_{IN}$ | 2.5 | 5 | pF |
| Input/Output Capacitance (DQ1-DQ16) | $C_{OUT}$ | 4 | 6.5 | pF |

## DC Characteristics

| Parameter | Symbol | Condition | | | MSM56V16160 | | | | Unit | Note |
|---|---|---|---|---|---|---|---|---|---|---|
| | | | | | F-8 | | F-10 | | | |
| | | Bank | CKE | Others | Min | Max | Min | Max | | |
| Output High Voltage | $V_{OH}$ | — | — | $I_{OH}$ = −2.0mA | 2.4 | — | 2.4 | — | V | |
| Output Low Voltage | $V_{OL}$ | — | — | $I_{OL}$ = 2.0mA | — | 0.4 | — | 0.4 | V | |
| Input Leakage Current | $I_{LI}$ | — | — | — | −10 | 10 | −10 | 10 | µA | |
| Input Leakage Current | $I_{LO}$ | — | — | — | −10 | 10 | −10 | 10 | µA | |
| Average power supply current (Operating) | $I_{CC1}$ | One Bank Active | CKE≥$V_{IH}$ | $t_{CC}$=min.<br>$t_{RC}$=min.<br>No Burst | — | 80 | — | 70 | mA | 1,2 |
| | $I_{CC1D}$ | Both Banks Active | CKE≥$V_{IH}$ | $t_{CC}$=min.<br>$t_{RC}$=min.<br>$t_{RRD}$=min.<br>No Burst | — | 115 | — | 95 | mA | 1,2 |
| Power supply current (Standby) | $I_{CC2}$ | Both Banks Precharge | CKE≥$V_{IH}$ | $t_{CC}$=min. | — | 35 | — | 30 | mA | 3 |
| Average power supply current (Clock Suspension) | $I_{CC3S}$ | Both Banks Active | CKE≤$V_{IL}$ | $t_{CC}$=min. | — | 3 | — | 3 | mA | 2 |
| Average power supply current (Active Standby ) | $I_{CC3}$ | One Bank Active | CKE≥$V_{IH}$ | $t_{CC}$=min. | — | 40 | — | 35 | mA | 3 |
| Power supply current (Burst) | $I_{CC4}$ | Both Banks Active | CKE≥$V_{IH}$ | $t_{CC}$=min. | — | 125 | — | 100 | mA | 1,2 |
| Power supply current (Auto-Refresh) | $I_{CC5}$ | One Bank Active | CKE≥$V_{IH}$ | $t_{CC}$=min.<br>$t_{RC}$=min. | — | 80 | — | 70 | mA | 2 |
| Average power supply current (Self-Refresh) | $I_{CC6}$ | Both Banks Precharge | CKE≤$V_{IL}$ | $t_{CC}$=min. | — | 2 | — | 2 | mA | |
| Average power supply current (Power Down) | $I_{CC7}$ | Both Banks Precharge | CKE≤$V_{IL}$ | $t_{CC}$=min. | — | 2 | — | 2 | mA | |

Notes: 1. Measured with outputs open.
2. The address and data can be changed once or left unchanged during one cycle.
3. The address and data can be changed once or left unchanged during two cycles.

## Mode Set Address Keys

| $\overline{\text{CAS}}$ Latency | | | | Burst Type | | Burst Length | | | | |
|---|---|---|---|---|---|---|---|---|---|---|
| A6 | A5 | A4 | CL | A3 | BT | A2 | A1 | A0 | BT = 0 | BT = 1 |
| 0 | 0 | 0 | Reserved | 0 | Sequential | 0 | 0 | 0 | 1 | 1 |
| 0 | 0 | 1 | 1 | 1 | Interleave | 0 | 0 | 1 | 2 | 2 |
| 0 | 1 | 0 | 2 | | | 0 | 1 | 0 | 4 | 4 |
| 0 | 1 | 1 | 3 | | | 0 | 1 | 1 | 8 | 8 |
| 1 | 0 | 0 | Reserved | | | 1 | 0 | 0 | Reserved | Reserved |
| 1 | 0 | 1 | Reserved | | | 1 | 0 | 1 | Reserved | Reserved |
| 1 | 1 | 0 | Reserved | | | 1 | 1 | 0 | Reserved | Reserved |
| 1 | 1 | 1 | Reserved | | | 1 | 1 | 1 | Full Page | Reserved |

Notes: A7, A8, A9, A10 and A11 should stay “L” during mode set cycle.

POWER ON SEQUENCE

1. With inputs in NOP state, turn on the power supply and start the system clock.
2. After the $V_{CC}$ voltage has reached the specified level, pause for 200μs or more with the input kept in NOP state.
3. Issue the precharge all bank command.
4. Apply a CBR auto-refresh eight or more times.
5. Enter the mode register setting command.

## AC Characteristic (1/2)

Note 1,2

| Parameter | | Symbol | MSM56V16160 | | | | Unit | Note |
|---|---|---|---|---|---|---|---|---|
| | | | F-8 | | F-10 | | | |
| | | | Min. | Max. | Min. | Max. | | |
| Clock Cycles Time | CL = 3 | $t_{CC}$ | 8 | — | 10 | — | ns | |
| | CL = 2 | | 12 | — | 15 | — | ns | |
| | CL = 1 | | 24 | — | 30 | — | ns | |
| Access Time from Clock | CL = 3 | $t_{AC}$ | — | 6 | — | 9 | ns | 3,4 |
| | CL = 2 | | — | 9 | — | 9 | ns | 3,4 |
| | CL = 1 | | — | 22 | — | 27 | ns | 3,4 |
| Clock High Pulse Time | | $t_{CH}$ | 3 | — | 3 | — | ns | 4 |
| Clock Low Pulse Time | | $t_{CL}$ | 3 | — | 3 | — | ns | 4 |
| Input Setup Time | | $t_{SI}$ | 2 | — | 3 | — | ns | |
| Input Hold Time | | $t_{HI}$ | 1 | — | 1 | — | ns | |
| Output Low Impedance Time from Clock | | $t_{OLZ}$ | 3 | — | 3 | | ns | |
| Output High Impedance Time from Clock | | $t_{OHZ}$ | — | 8 | — | 8 | ns | |
| Output Hold from Clock | | $t_{OH}$ | 3 | — | 3 | — | ns | 3 |
| $\overline{RAS}$ Cycle Time | | $t_{RC}$ | 70 | — | 90 | — | ns | |
| $\overline{RAS}$ Precharge Time | | $t_{RP}$ | 20 | — | 30 | — | ns | |
| $\overline{RAS}$ Active Time | | $t_{RAS}$ | 48 | $10^5$ | 60 | $10^5$ | ns | |
| $\overline{RAS}$ to $\overline{CAS}$ Delay Time | | $t_{RCD}$ | 20 | — | 30 | — | ns | |
| Write Recovery Time | | $t_{WR}$ | 8 | — | 15 | — | ns | |
| $\overline{RAS}$ to $\overline{RAS}$ Bank Active Delay Time | | $t_{RRD}$ | 20 | — | 20 | — | ns | |
| Refresh Time | | $t_{REF}$ | — | 64 | — | 64 | ms | |
| Power-down Exit setup Time | | $t_{PDE}$ | $t_{SI}$+1CLK | — | $t_{SI}$+1CLK | — | ns | |
| Input Level Transition Time | | $t_T$ | — | 3 | — | 3 | ns | |
| $\overline{CAS}$ to $\overline{CAS}$ Delay Time(Min.) | | $l_{CCD}$ | 1 | | 1 | | Cycle | |
| Clock Disable Time from CKE | | $l_{CKE}$ | 1 | | 1 | | Cycle | |
| Data Output High Impedance Time from UDQM, LDQM | | $l_{DOZ}$ | 2 | | 2 | | Cycle | |
| Data Input Mask Time from UDQM, LDQM | | $l_{DOD}$ | 0 | | 0 | | Cycle | |
| Data Input Mask Time from Write Command | | $l_{DWD}$ | 0 | | 0 | | Cycle | |

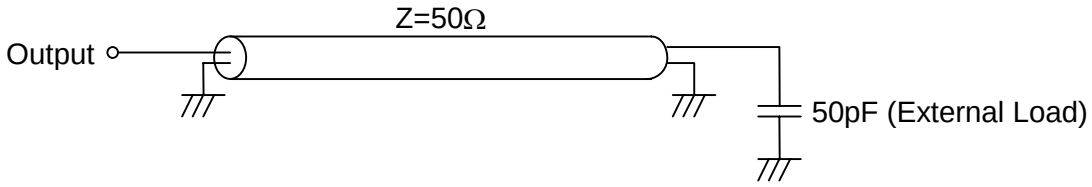
## AC Characteristic (2/2)

Note 1,2

| Parameter | Symbol | MSM56V16160 | | | | Unit | Note |
|---|---|---|---|---|---|---|---|
| | | F-8 | | F-10 | | | |
| | | Min. | Max. | Min. | Max. | | |
| Data Output High Impedance Time from Precharge Command | $l_{ROH}$ | CL | | CL | | Cycle | |
| Active Command Input Time from Mode Register Set Command Input (Min.) | $l_{MRD}$ | 3 | | 3 | | Cycle | |
| Write Command Input Time from Output | $l_{OWD}$ | 2 | | 2 | | Cycle | |

Notes:

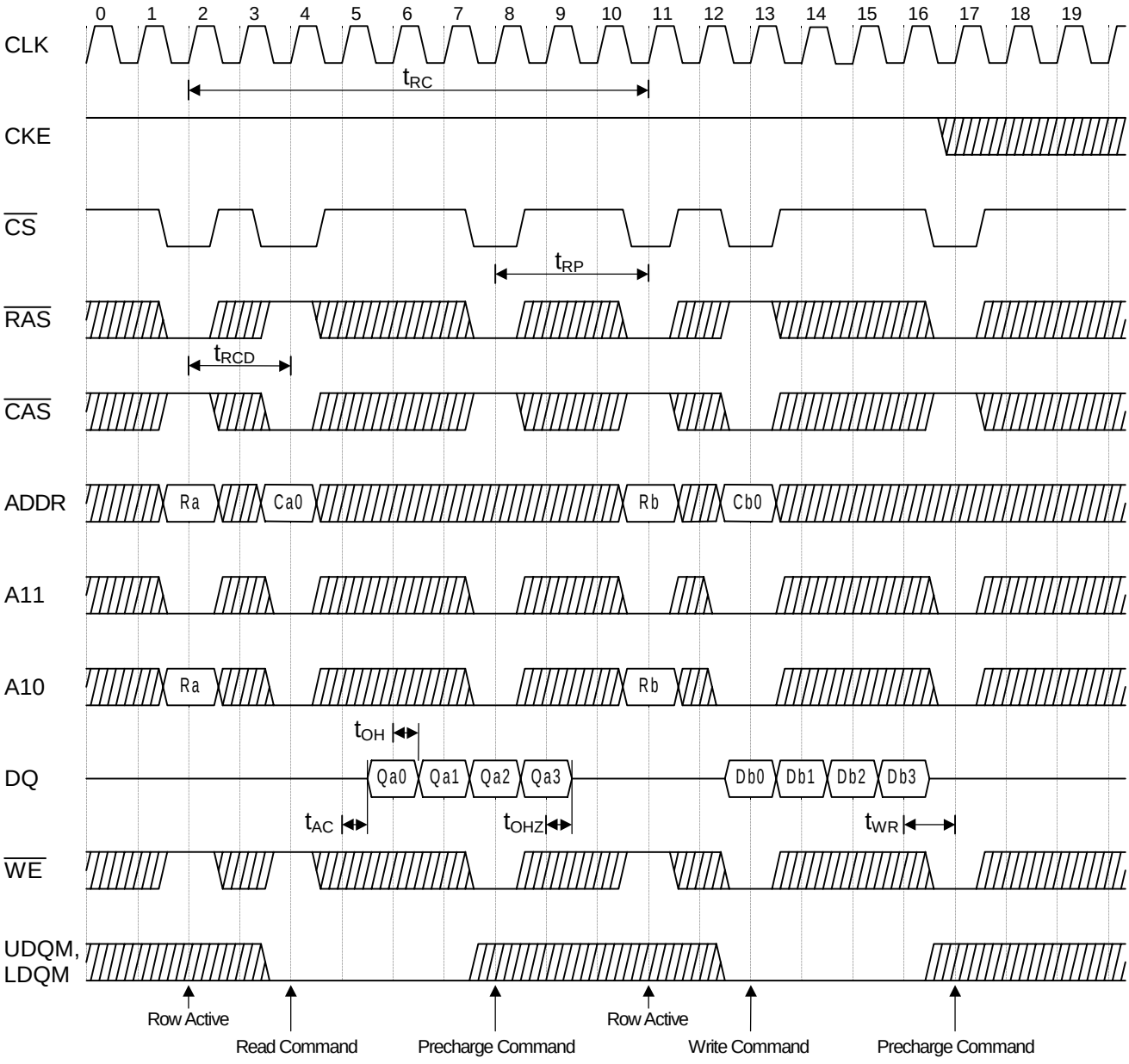
1) AC measurements assume that $t_T$ = 1ns.
2) The reference level for timing of input signals is 1.4V.
3) Output load.



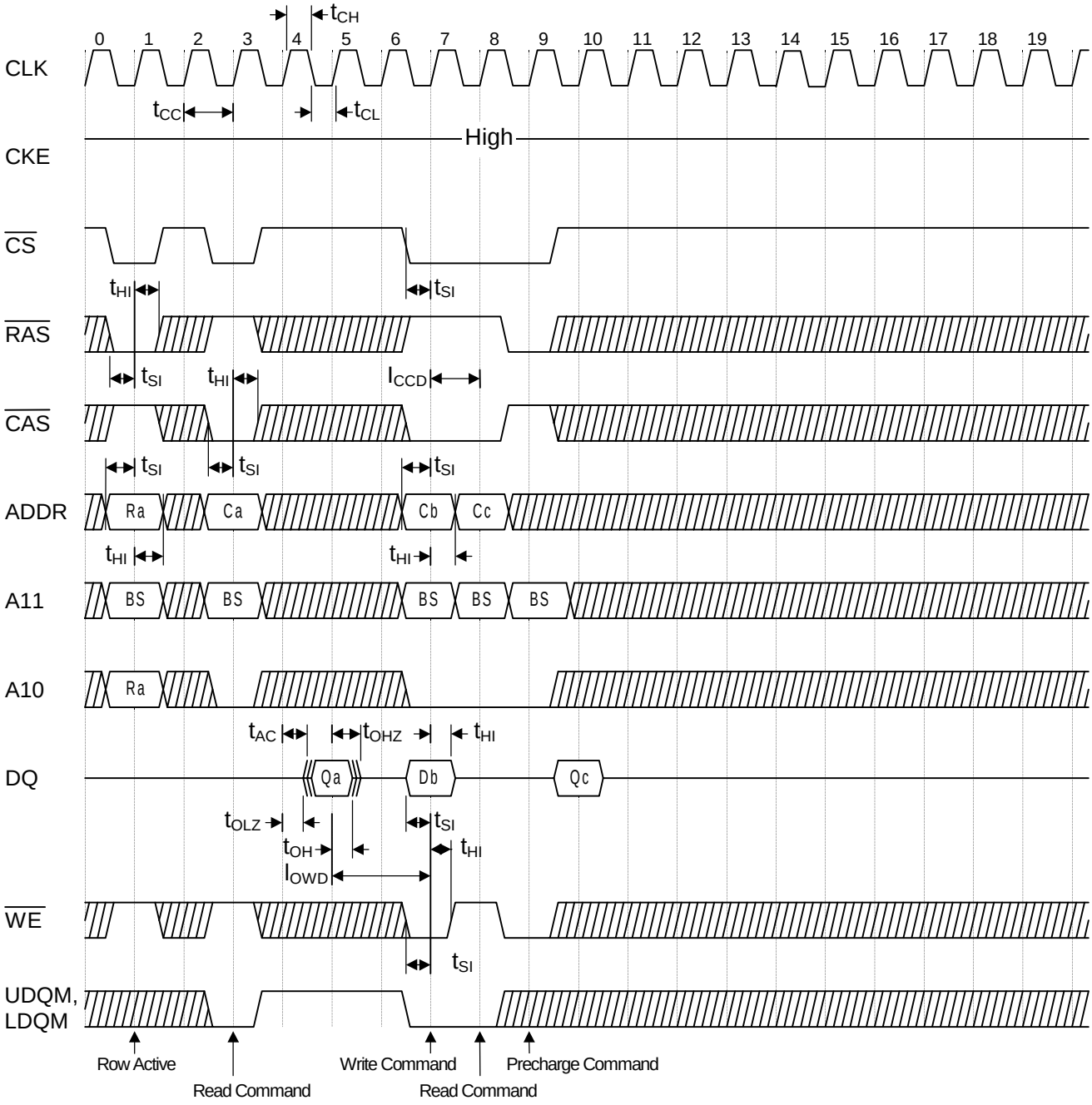

4) The access time is defined at 1.5V.
5) If $t_T$ is longer than 1ns, then the reference level for timing of input signals is $V_{IH}$ and $V_{IL}$.

# TIMING WAVEFORM

- **Read & Write Cycle (Same Bank) @$\overline{CAS}$ Latency=2, Burst Length=4**



- **Single Bit Read-Write-Read Cycle (Same Page) @$\overline{CAS}$ Latency=2, Burst Length=4**



∗Notes : 1. When $\overline{CS}$ is set ”High” at a clock transition from “Low” to ”High”, all inputs except CKE, UDQM and LDQM are invalid.

2. When issuing an active, read or write command, the bank is selected by A11.

| A11 | Active, read or write |
|---|---|
| 0 | Bank A |
| 1 | Bank B |

3. The auto precharge function is enabled or disabled by the A10 input when the read or write command is issued.

| A10 | A11 | Operation |
|---|---|---|
| 0 | 0 | After the end of burst, bank A holds the idle status. |
| 1 | 0 | After the end of burst, bank A is precharged automatically. |
| 0 | 1 | After the end of burst, bank B holds the idle status. |
| 1 | 1 | After the end of burst, bank B is precharged automatically. |

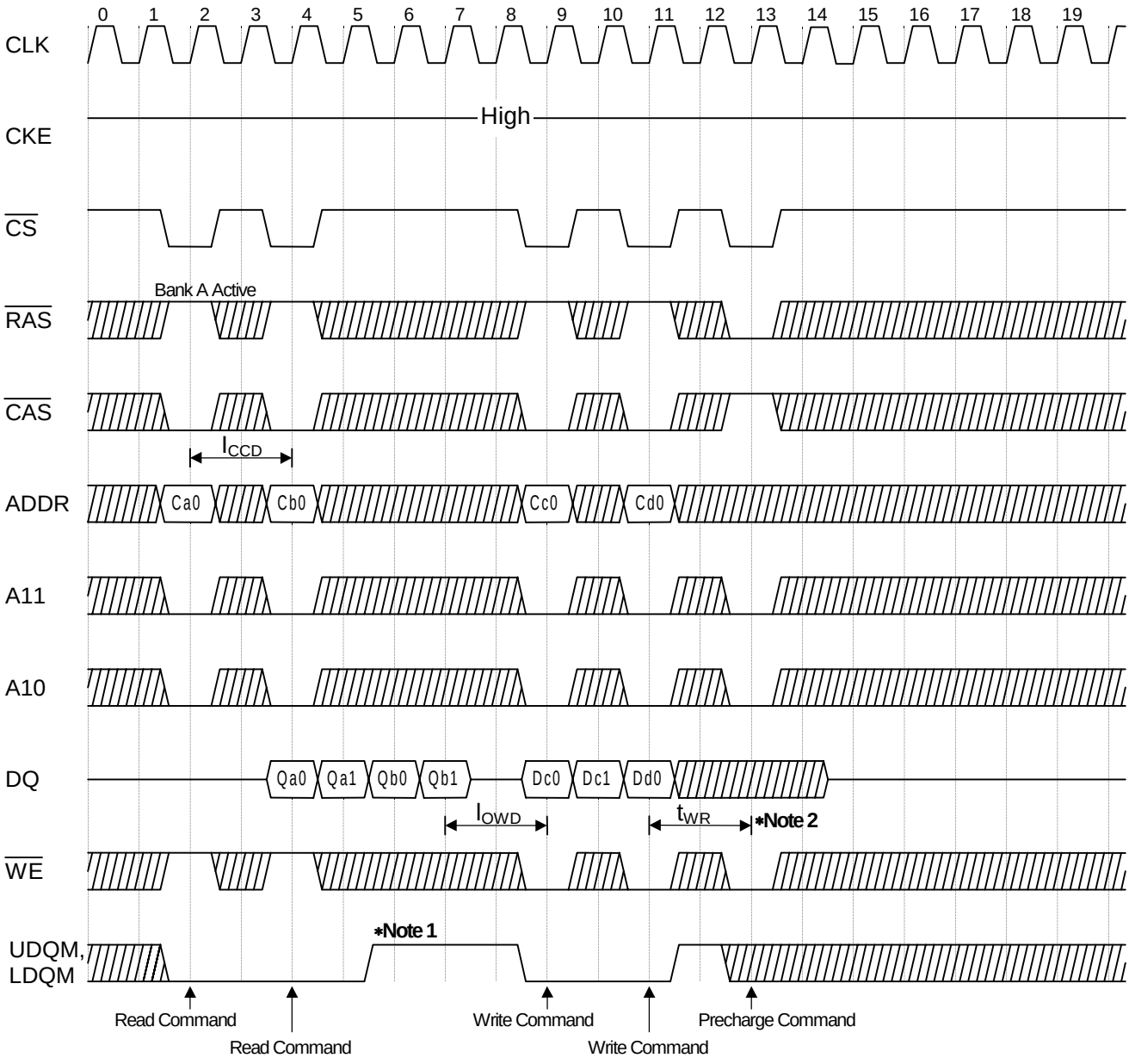
4. When issuing a precharge command, the bank to be precharged is selected by the A10 and A11 inputs.

| A10 | A11 | Operation |
|---|---|---|
| 0 | 0 | Bank A is precharged. |
| 0 | 1 | Bank B is precharged. |
| 1 | X | Both banks A and B are precharged. |

5. The input data and the write command are latched by the same clock (Write latency = 0).

6. The output is forced to high impedance by (1CLK+$t_{OHZ}$) after UDQM, LDQM entry.

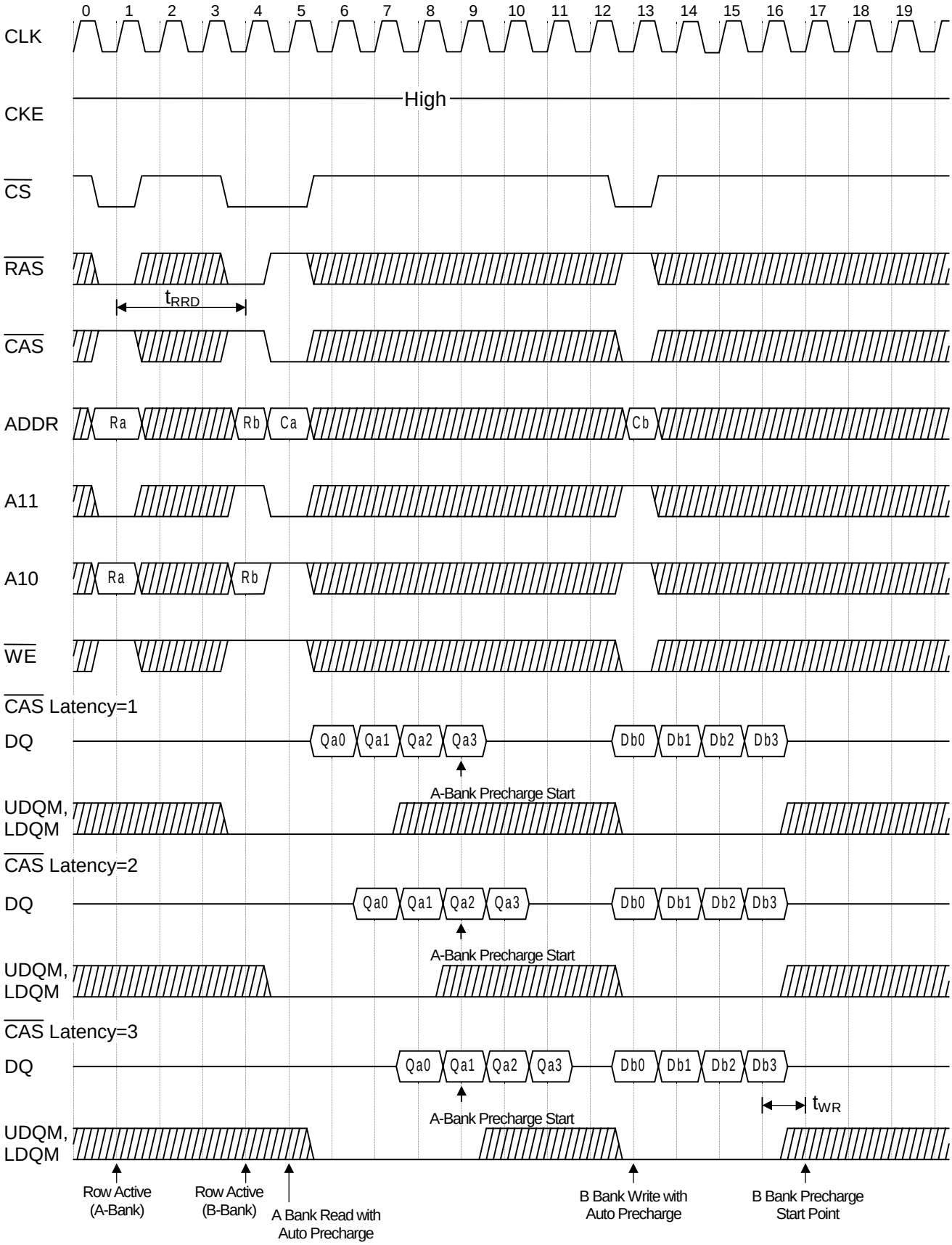
- **Page Read & Write Cycle (Same Bank) @$\overline{CAS}$ Latency=2, Burst Length=4**



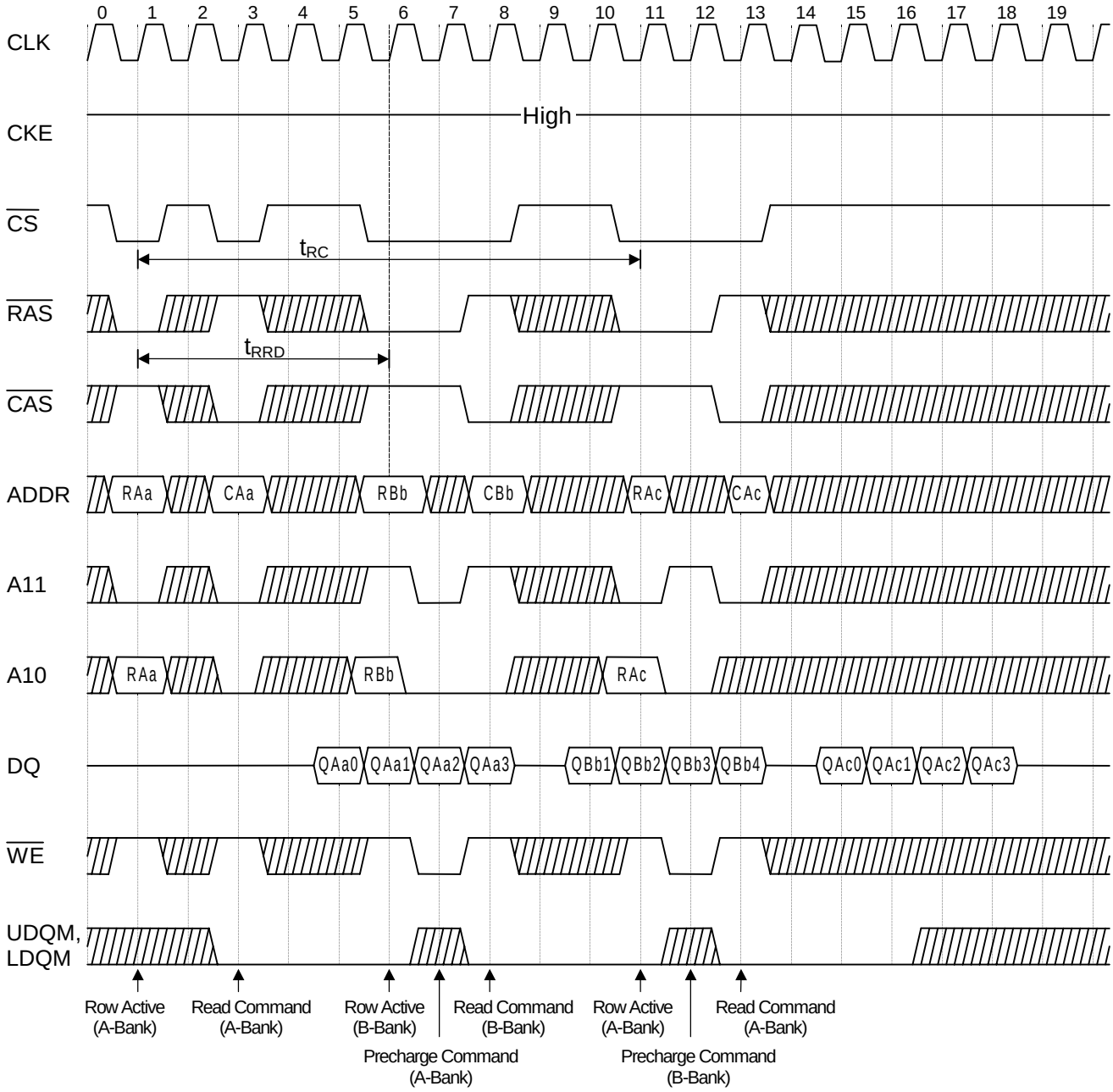

∗Notes: 1. To write data before a burst read ends, UDQM and LDQM should be asserted three cycles prior to the write command to avoid bus contention.

2. To assert row precharge before a burst write ends, wait $t_{WR}$ after the last write data input. Input data during the precharge input cycle will be masked internally.

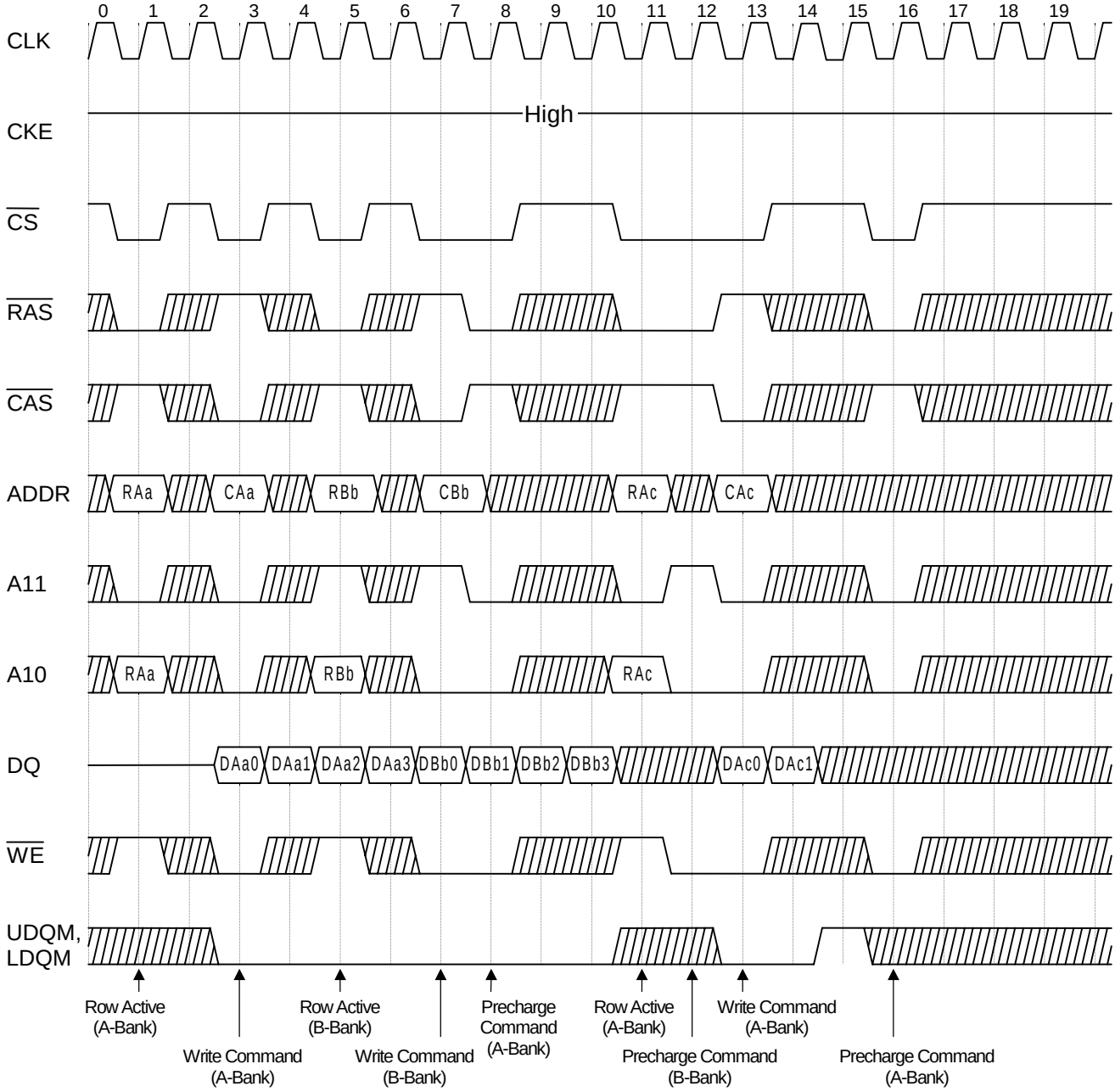
- **Read & Write Cycle with Auto Precharge @ Burst Length=4**



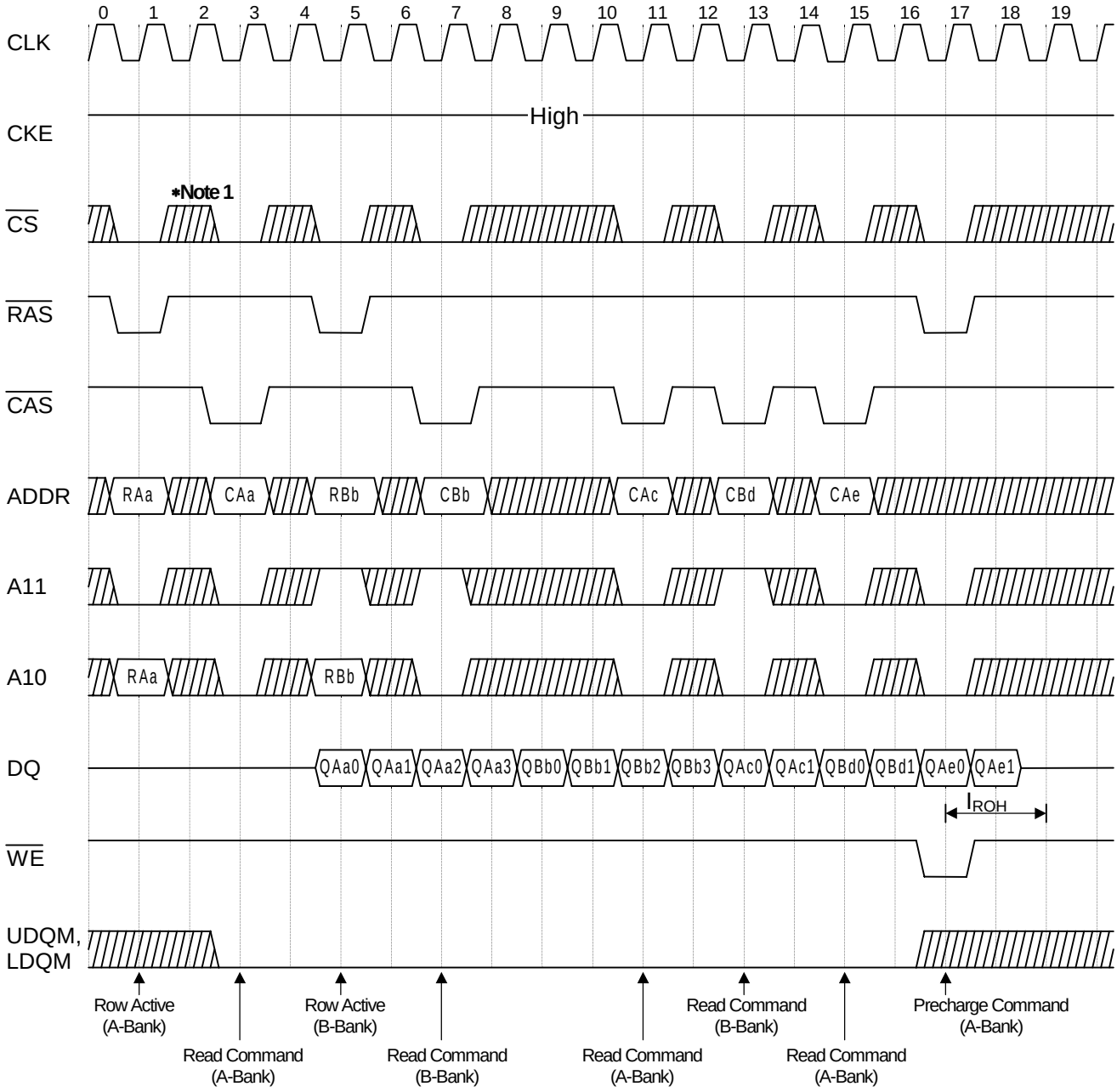
- **Bank Interleave Random Row Read Cycle @$\overline{CAS}$ Latency = 2, Burst Length = 4**



- **Bank Interleave Random Row Write Cycle @$\overline{CAS}$ Latency = 2, Burst Length =4**

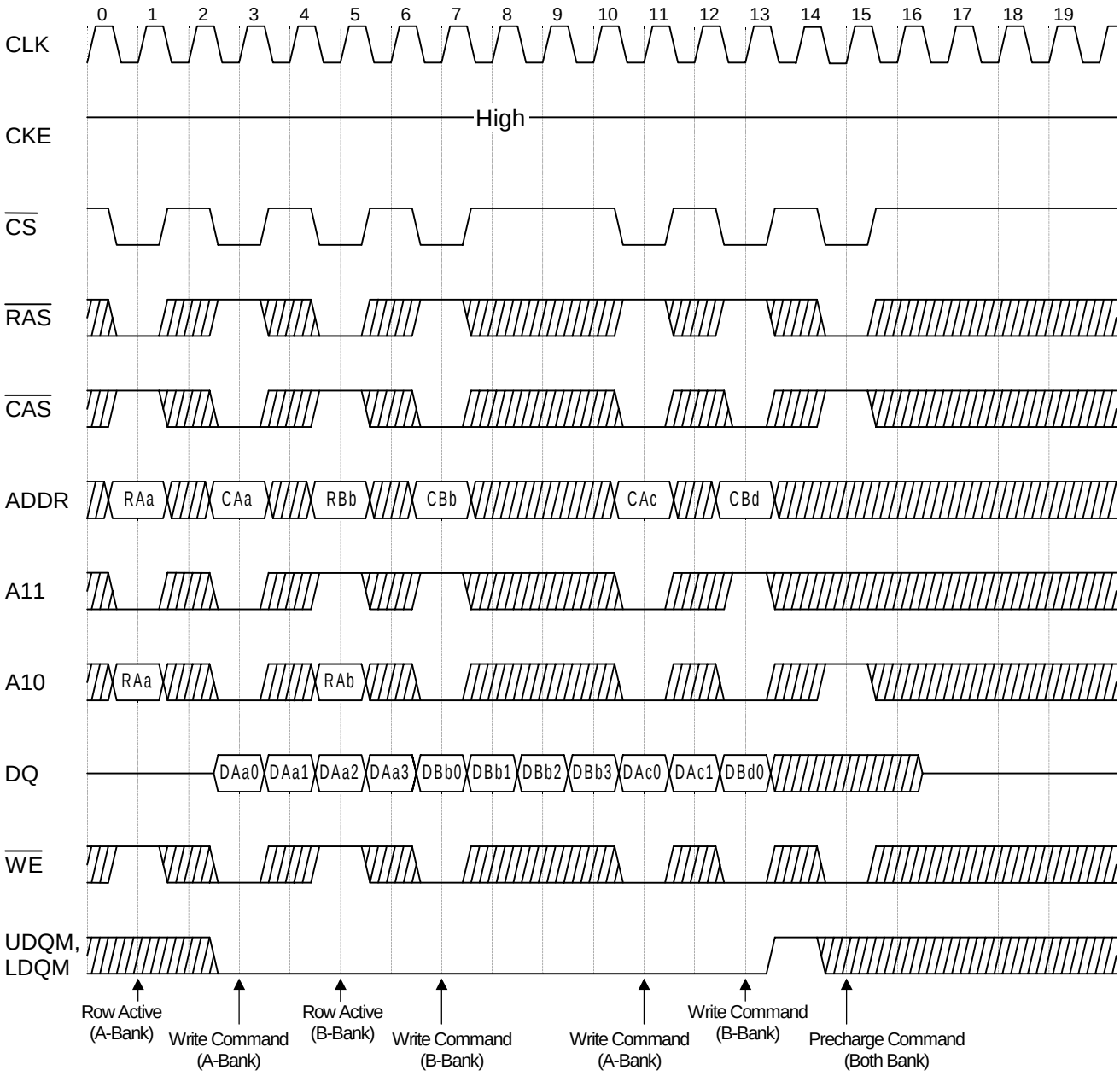


- **Bank Interleave Page Read Cycle @$\overline{CAS}$ Latency = 2, Burst Length =4**

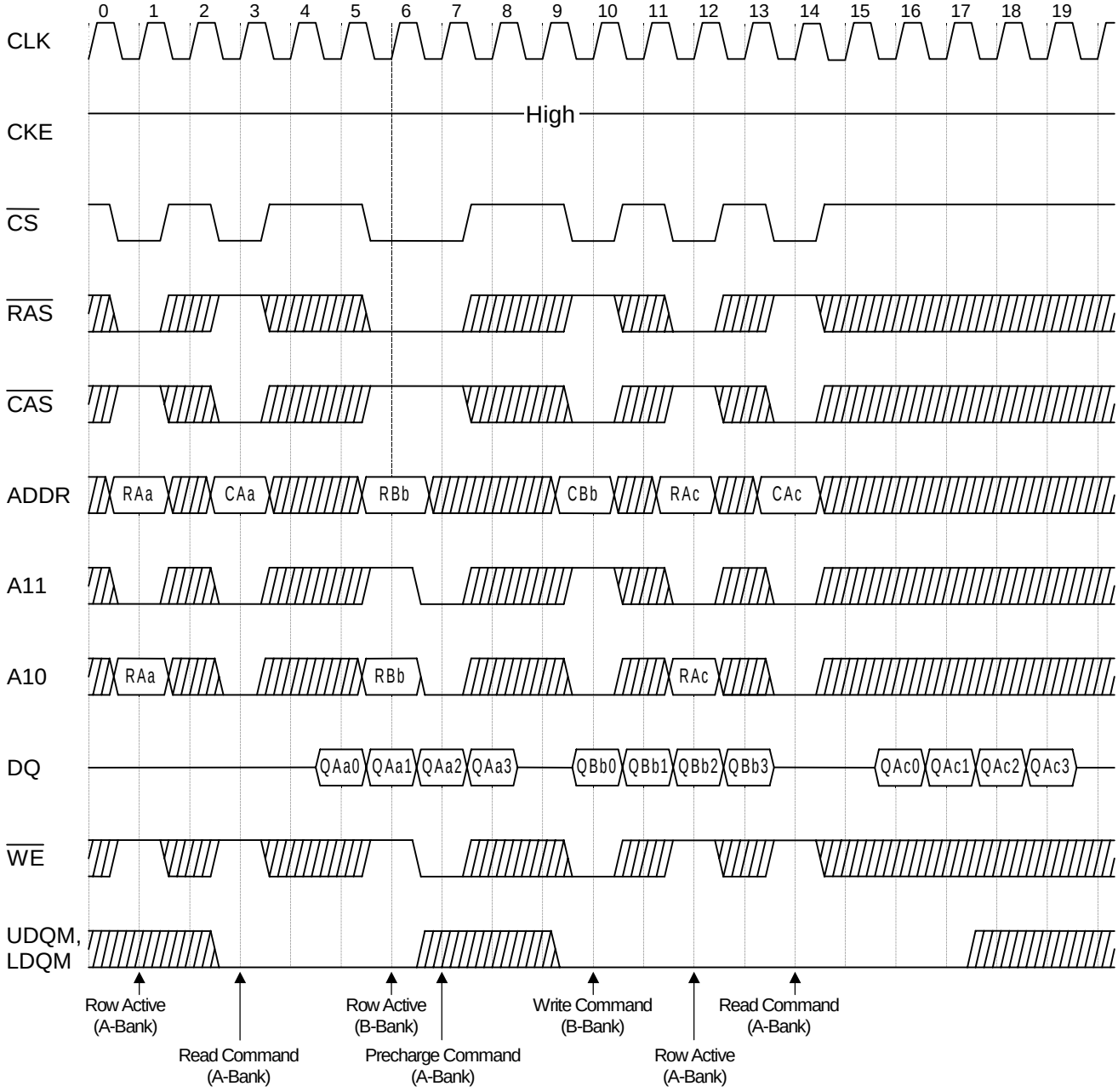



∗Note: 1. $\overline{CS}$ is ignored when $\overline{RAS}$, $\overline{CAS}$ and $\overline{WE}$ are high at the same cycle.

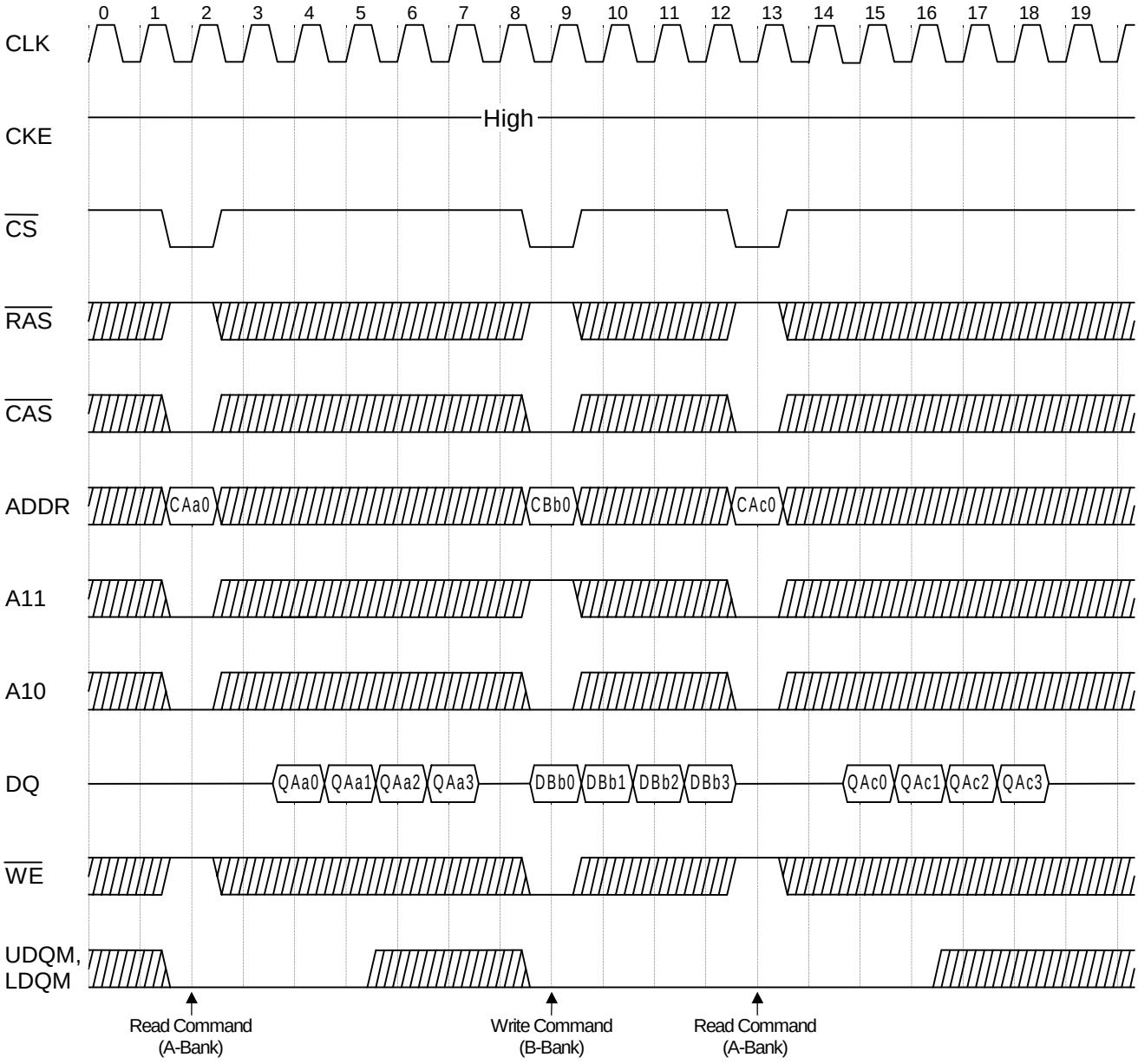
- **Bank Interleave Page Write Cycle @$\overline{CAS}$ Latency = 2, Burst Length=4**



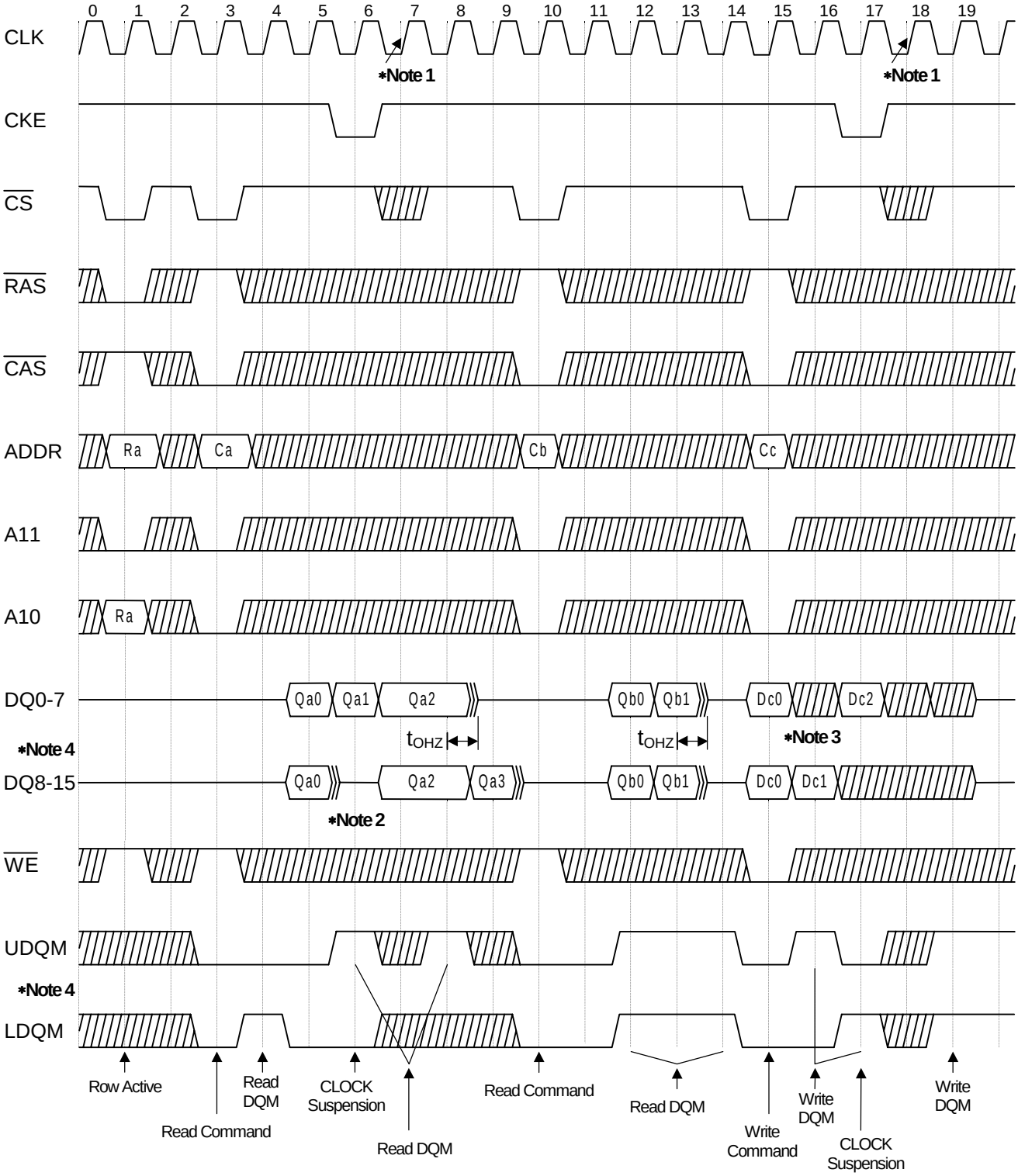
- **Bank Interleave Random Row Read/Write Cycle @$\overline{\text{CAS}}$ Latency = 2, Burst Length = 4**



- **Bank Interleave Page Read/Write Cycle @$\overline{\text{CAS}}$ Latency = 2, Burst Length =4**

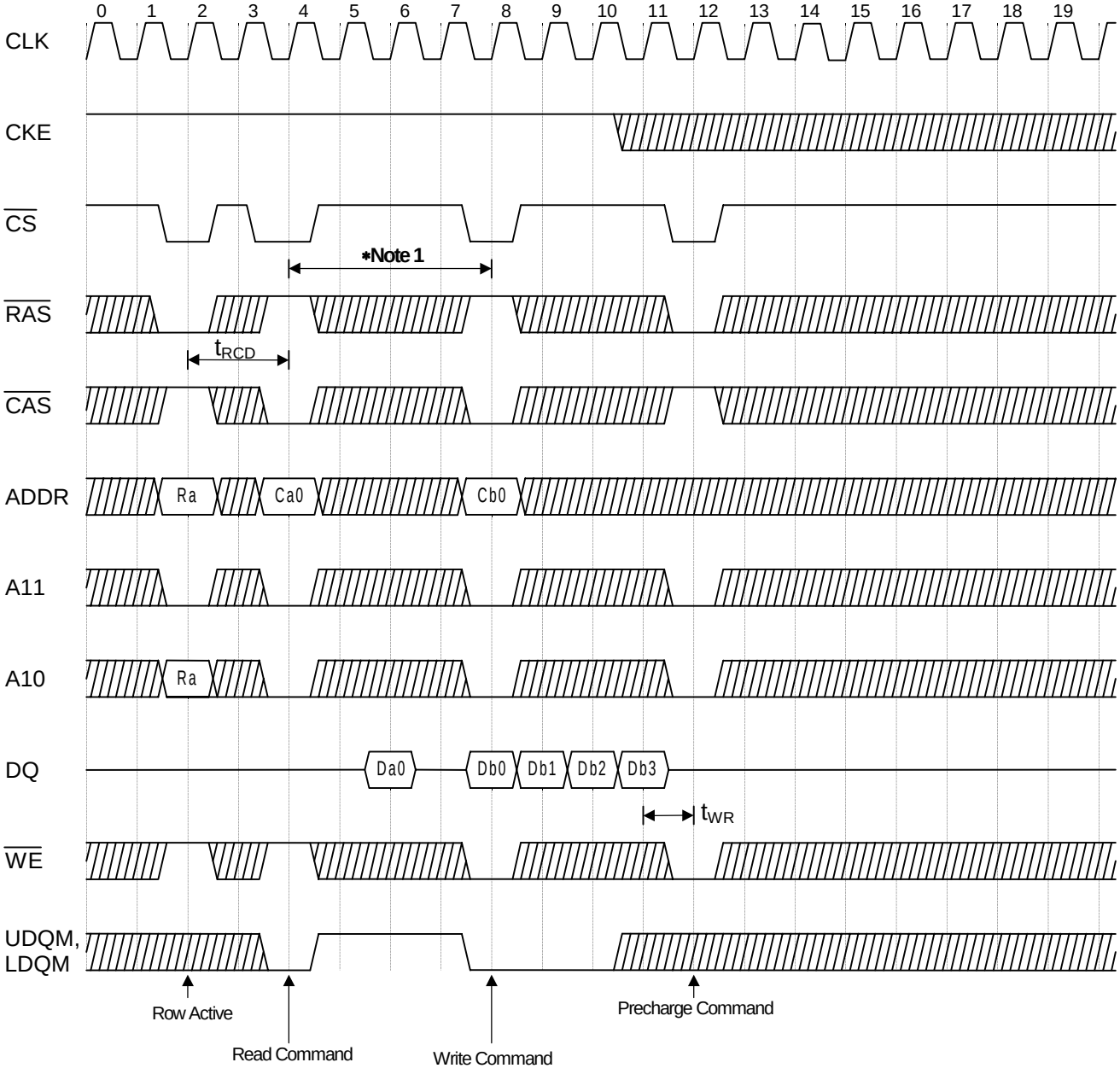


- **Clock Suspension & DQM Operation Cycle @$\overline{CAS}$ Latency = 2, Burst Length =4**



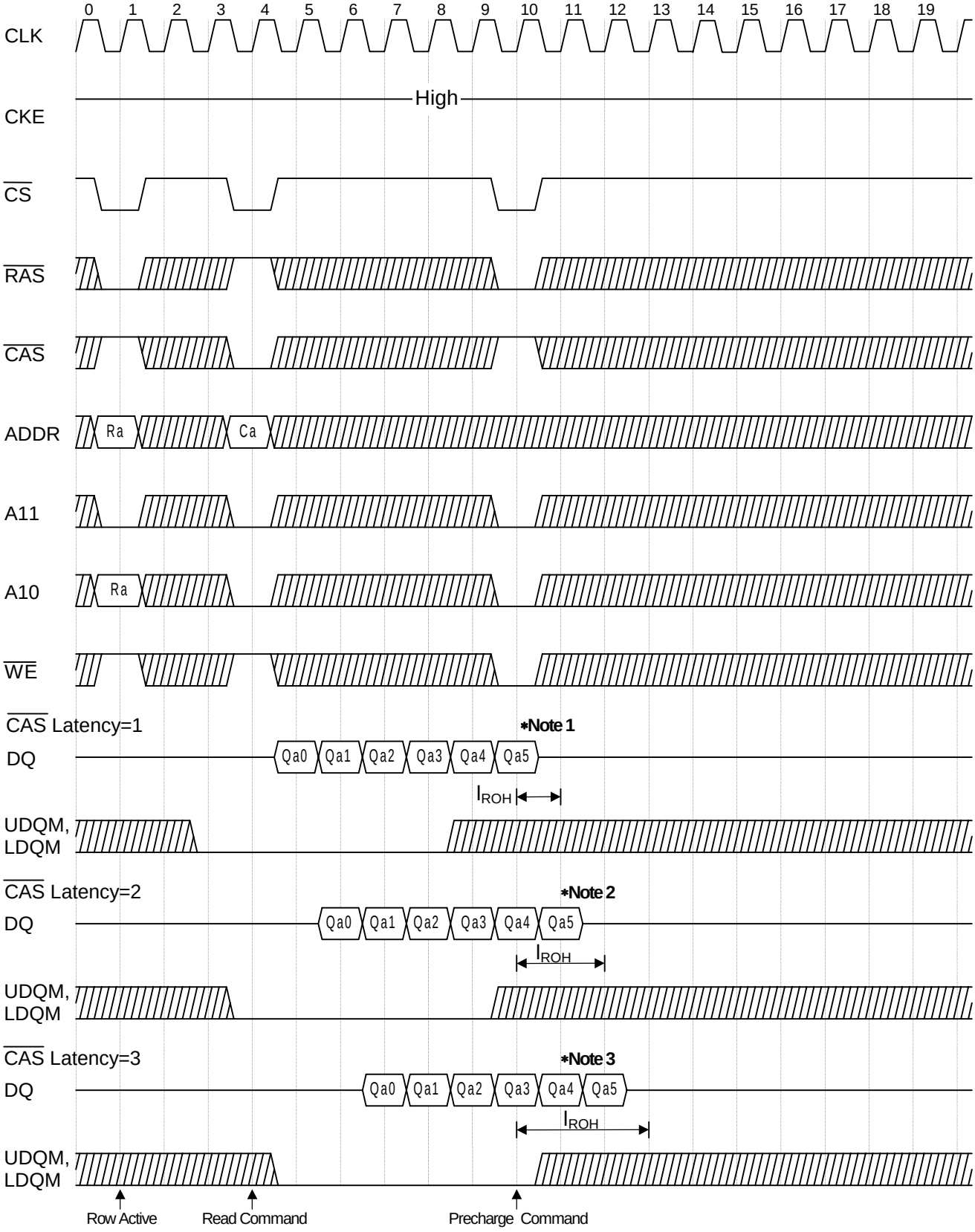

∗Notes:
1. When Clock Suspension is asserted, the next clock cycle is ignored.
2. When LDQM and UDQM are asserted, the read data after two clock cycles is masked.
3. When LDQM and UDQM are asserted, the write data in the same clock cycle is masked.
4. When LDQM is set High, the input/output data of DQ0-7 is masked.
   When UDQM is set High, the input/output data of DQ8-15 is masked.

- **Read to Write Cycle (Same Bank) @$\overline{CAS}$ Latency = 2, Burst Length =4**



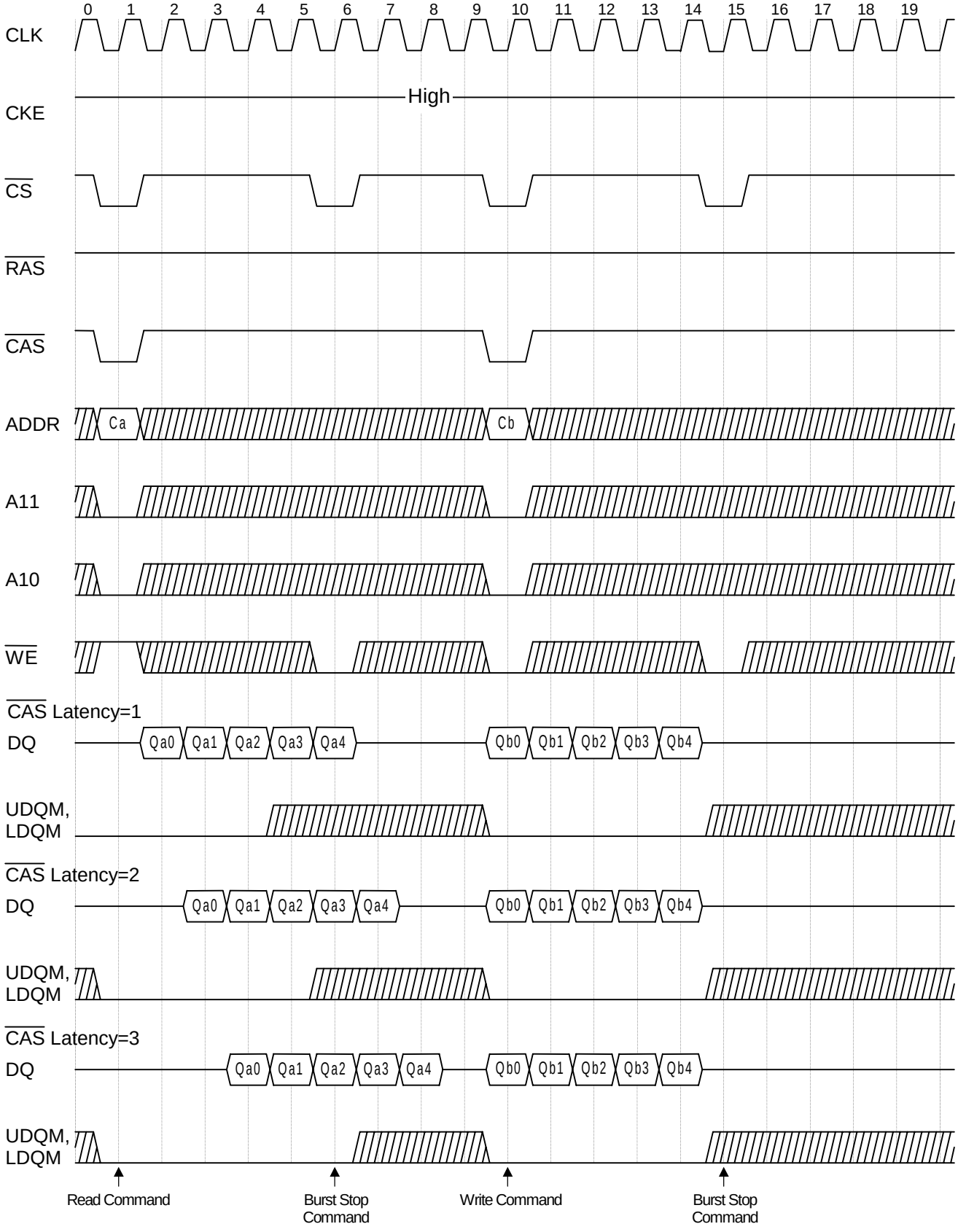

∗Note: 1. In Case $\overline{CAS}$ latency is 3, READ can be interrupted by WRITE.
The minimum command interval is [burst length + 1] cycles.
UDQM and LDQM must be high at least 3 clocks prior to the write command.

- **Read Interruption by Precharge Command @Burst Length =8**

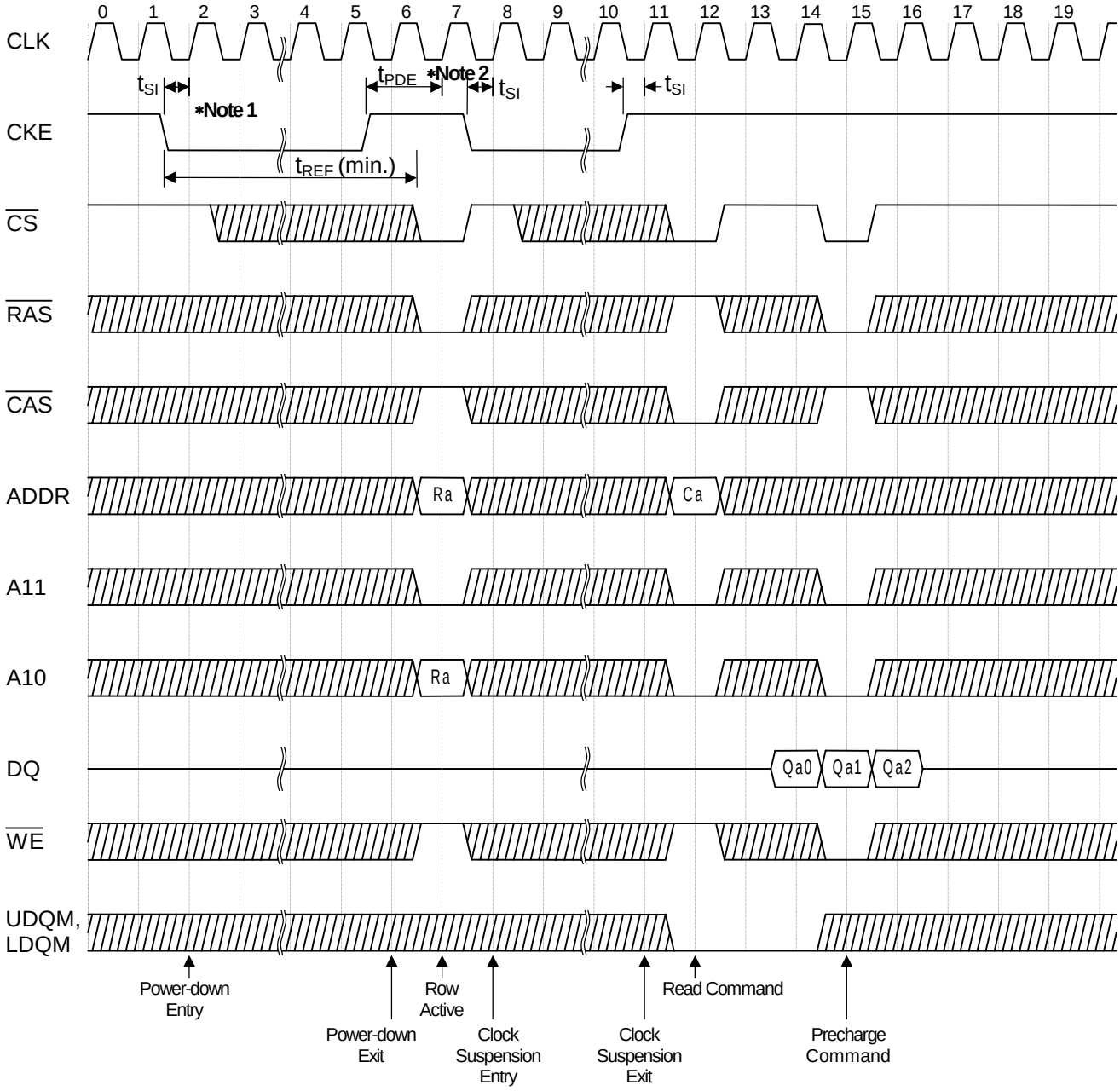



∗Notes:
1. When the $\overline{CAS}$ latency = 1, and if row precharge is asserted before a burst read ends, then the read data will not output after the next clock cycle of the precharge command.
2. When the $\overline{CAS}$ latency = 2, and if row precharge is asserted before burst read ends, then the read data will not output after the second clock cycle of the precharge command.
3. When the $\overline{CAS}$ latency = 3, and if row precharge is asserted before burst read ends, then the read data will not output after the second clock cycle of the precharge command.

- **Burst Stop Command @Burst Length =8**



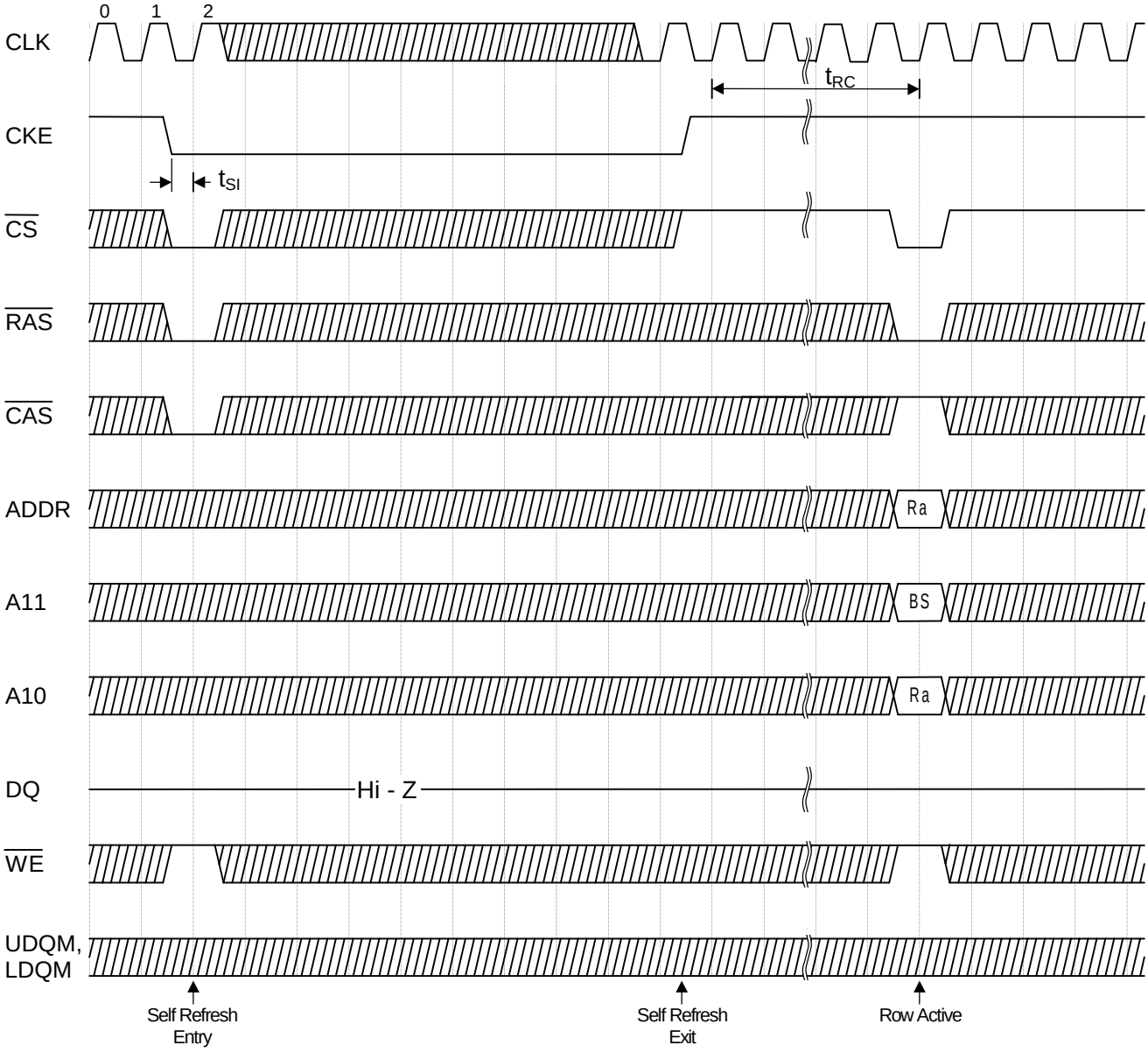
- **Power Down Mode @$\overline{\text{CAS}}$ Latency = 2, Burst Length =4**



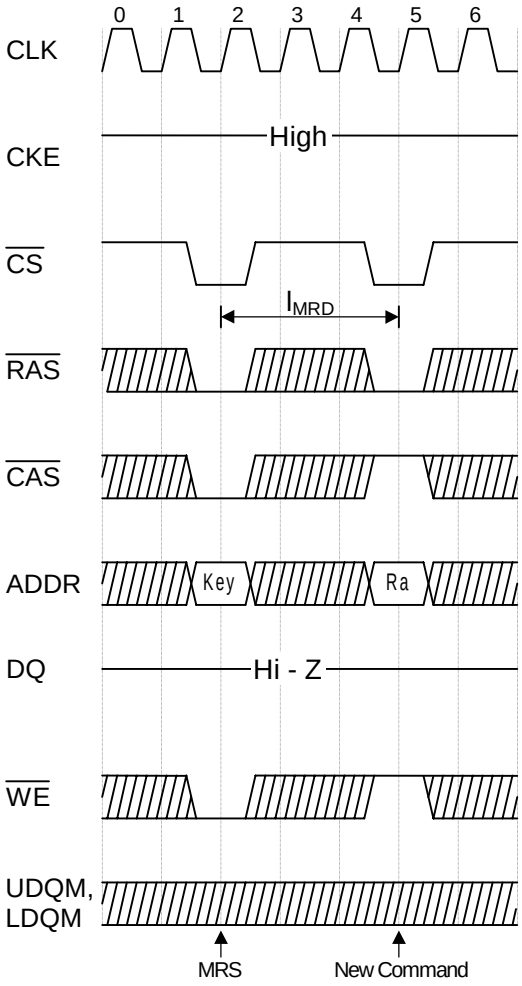

∗Notes: 1. When both banks are in precharge state, and if CKE is set low, then the MSM56V16160F enters power-down mode and maintains the mode while CKE is low.

2. To release the circuit from power-down mode, CKE has to be set high for longer than $t_{PDE}$ ($t_{SI}$ + 1CLK).

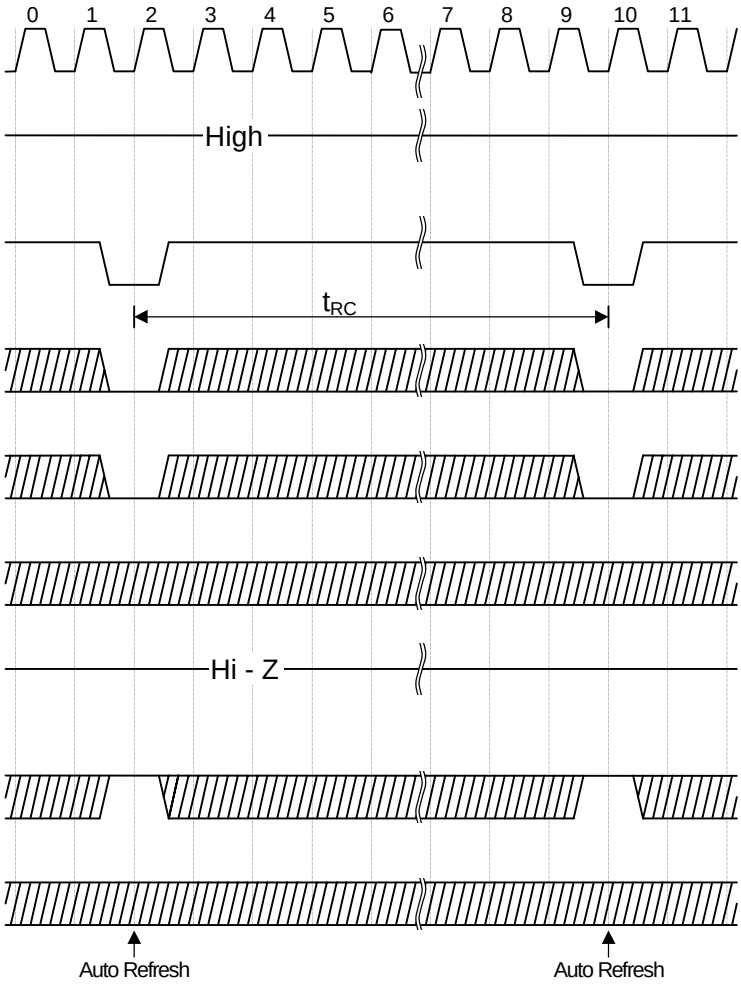
- **Self Refresh Cycle**



- **Mode Register Set Cycle**




- **Auto Refresh Cycle**



# FUNCTION TRUTH TABLE (Table 1) (1/2)

| Current State[1] | $\overline{CS}$ | $\overline{RAS}$ | $\overline{CAS}$ | $\overline{WE}$ | BA | ADDR | Action |
|---|---|---|---|---|---|---|---|
| Idle | H | X | X | X | X | X | NOP |
| | L | H | H | H | X | X | NOP |
| | L | H | H | L | BA | X | ILLEGAL [2] |
| | L | H | L | X | BA | CA | ILLEGAL [2] |
| | L | L | H | H | BA | RA | Row Active |
| | L | L | H | L | BA | A10 | NOP [4] |
| | L | L | L | H | X | X | Auto-Refresh or Self-Refresh [5] |
| | L | L | L | L | L | OP Code | Mode Register Write |
| Row Active | H | X | X | X | X | X | NOP |
| | L | H | H | X | X | X | NOP |
| | L | H | L | H | BA | CA, A10 | Read |
| | L | H | L | L | BA | CA, A10 | Write |
| | L | L | H | H | BA | RA | ILLEGAL [2] |
| | L | L | H | L | BA | A10 | Precharge |
| | L | L | L | X | X | X | ILLEGAL |
| Read | H | X | X | X | X | X | NOP (Continue Row Active after Burst ends) |
| | L | H | H | H | X | X | NOP (Continue Row Active after Burst ends) |
| | L | H | H | L | X | X | Term Burst --> Row Active |
| | L | H | L | H | BA | CA, A10 | Term Burst, start new Burst Read [3] |
| | L | H | L | L | BA | CA, A10 | Term Burst, start new Burst Write [3] |
| | L | L | H | H | BA | RA | ILLEGAL [2] |
| | L | L | H | L | BA | A10 | Term Burst, execute Row Precharge |
| | L | L | L | X | X | X | ILLEGAL |
| Write | H | X | X | X | X | X | NOP (Continue Row Active after Burst ends) |
| | L | H | H | H | X | X | NOP (Continue Row Active after Burst ends) |
| | L | H | H | L | X | X | Term Burst --> Row Active |
| | L | H | L | H | BA | CA, A10 | Term Burst, start new Burst Read [3] |
| | L | H | L | L | BA | CA, A10 | Term Burst, start new Burst Write [3] |
| | L | L | H | H | BA | RA | ILLEGAL [2] |
| | L | L | H | L | BA | A10 | Term Burst, execute Row Precharge [3] |
| | L | L | L | X | X | X | ILLEGAL |
| Read with Auto Precharge | H | X | X | X | X | X | NOP (Continue Burst to End and enter Row Precharge) |
| | L | H | H | H | X | X | NOP (Continue Burst to End and enter Row Precharge) |
| | L | H | H | L | BA | X | ILLEGAL [2] |
| | L | H | L | H | BA | CA, A10 | ILLEGAL [2] |
| | L | H | L | L | X | X | ILLEGAL |
| | L | L | H | X | BA | RA, A10 | ILLEGAL [2] |
| | L | L | L | X | X | X | ILLEGAL |
| Write with Auto Precharge | H | X | X | X | X | X | NOP (Continue Burst to End and enter Row Precharge) |
| | L | H | H | H | X | X | NOP (Continue Burst to End and enter Row Precharge) |
| | L | H | H | L | BA | X | ILLEGAL [2] |
| | L | H | L | H | BA | CA, A10 | ILLEGAL [2] |
| | L | H | L | L | X | X | ILLEGAL |
| | L | L | H | X | BA | RA, A10 | ILLEGAL [2] |
| | L | L | L | X | X | X | ILLEGAL |

# FUNCTION TRUTH TABLE (Table 1) (2/2)

| Current State[1] | $\overline{CS}$ | $\overline{RAS}$ | $\overline{CAS}$ | $\overline{WE}$ | BA | ADDR | Action |
|---|---|---|---|---|---|---|---|
| Precharge | H | X | X | X | X | X | NOP --> Idle after $t_{RP}$ |
| | L | H | H | H | X | X | NOP --> Idle after $t_{RP}$ |
| | L | H | H | L | BA | X | ILLEGAL [2] |
| | L | H | L | X | BA | CA | ILLEGAL [2] |
| | L | L | H | H | BA | RA | ILLEGAL [2] |
| | L | L | H | L | BA | A10 | NOP [4] |
| | L | L | L | X | X | X | ILLEGAL |
| Write Recovery | H | X | X | X | X | X | NOP |
| | L | H | H | H | X | X | NOP |
| | L | H | H | L | BA | X | ILLEGAL [2] |
| | L | H | L | X | BA | CA | ILLEGAL [2] |
| | L | L | H | H | BA | RA | ILLEGAL [2] |
| | L | L | H | L | BA | A10 | ILLEGAL [2] |
| | L | L | L | X | X | X | ILLEGAL |
| Row Active | H | X | X | X | X | X | NOP --> Row Active after $t_{RCD}$ |
| | L | H | H | H | X | X | NOP --> Row Active after $t_{RCD}$ |
| | L | H | H | L | BA | X | ILLEGAL [2] |
| | L | H | L | X | BA | CA | ILLEGAL [2] |
| | L | L | H | H | BA | RA | ILLEGAL [2] |
| | L | L | H | L | BA | A10 | ILLEGAL [2] |
| | L | L | L | X | X | X | ILLEGAL |
| Refresh | H | X | X | X | X | X | NOP --> Idle after $t_{RC}$ |
| | L | H | H | X | X | X | NOP --> Idle after $t_{RC}$ |
| | L | H | L | X | X | X | ILLEGAL |
| | L | L | H | X | X | X | ILLEGAL |
| | L | L | L | X | X | X | ILLEGAL |
| Mode Register Access | H | X | X | X | X | X | NOP |
| | L | H | H | H | X | X | NOP |
| | L | H | H | L | X | X | ILLEGAL |
| | L | H | L | X | X | X | ILLEGAL |
| | L | L | X | X | X | X | ILLEGAL |

ABBREVIATIONS

RA = Row Address BA = Bank Address NOP = No OPeration command

CA = Column Address AP = Auto Precharge

∗Notes : 1. All inputs are enabled when CKE is set high for at least 1 cycle prior to the inputs.

2. Illegal to bank in specified state, but may be legal in some cases depending on the state of bank selection.

3. Satisfy the timing of $I_{CCD}$ and $t_{WR}$ to prevent bus contention.

4. NOP to bank precharging or in idle state. Precharges activated bank by BA or A10.

5. Illegal if any bank is not idle.

## FUNCTION TRUTH TABLE for CKE (Table 2)

| Current State (n) | CKEn-1 | CKEn | $\overline{CS}$ | $\overline{RAS}$ | $\overline{CAS}$ | $\overline{WE}$ | ADDR | Action |
|---|---|---|---|---|---|---|---|---|
| Self Refresh | H | X | X | X | X | X | X | INVALID |
| | L | H | H | X | X | X | X | Exit Self Refresh --> ABI |
| | L | H | L | H | H | H | X | Exit Self Refresh --> ABI |
| | L | H | L | H | H | L | X | ILLEGAL |
| | L | H | L | H | L | X | X | ILLEGAL |
| | L | H | L | L | X | X | X | ILLEGAL |
| | L | L | X | X | X | X | X | NOP (Maintain Self Refresh) |
| Power Down | H | X | X | X | X | X | X | INVALID |
| | L | H | H | X | X | X | X | Exit Power Down --> ABI |
| | L | H | L | H | H | H | X | Exit Power Down --> ABI |
| | L | H | L | H | H | L | X | ILLEGAL |
| | L | H | L | H | L | X | X | ILLEGAL |
| | L | H | L | L | X | X | X | ILLEGAL [6] |
| | L | L | X | X | X | X | X | NOP (Continue power down mode) |
| All Banks Idle [6] (ABI) | H | H | X | X | X | X | X | Refer to Table 1 |
| | H | L | H | X | X | X | X | Enter Power Down |
| | H | L | L | H | H | H | X | Enter Power Down |
| | H | L | L | H | H | L | X | ILLEGAL |
| | H | L | L | H | L | X | X | ILLEGAL |
| | H | L | L | L | H | L | X | ILLEGAL |
| | H | L | L | L | L | H | X | Enter Self Refresh |
| | H | L | L | L | L | L | X | ILLEGAL |
| | L | L | X | X | X | X | X | NOP |
| Any State Other than Listed Above | H | H | X | X | X | X | X | Refer to Operations in Table 1 |
| | H | L | X | X | X | X | X | Begin Clock Suspend Next Cycle |
| | L | H | X | X | X | X | X | Enable Clock of Next Cycle |
| | L | L | X | X | X | X | X | Continue Clock Suspension |

∗Notes : 6. Power-down and self-refresh can be entered only when all the banks are in an idle state.

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