Integrated Device Technology, Inc.

CMOS PARALLEL-TO-SERIAL FIFO 2048 x 9-BIT & 4096 x 9-BIT

IDT 72131
IDT 72141

T-46-35

FEATURES:

- 35ns parallel port access time
- 50MHz serial port shift rate
- Easily expandable in depth and width
- Programmable word lengths including 7-9, 16-18, and 32-36 bits using Flexishift™ serial output without using any additional components
- Multiple status flags: Full, Almost-Full (1/8 from full), Half-Full, Almost-Empty (1/8 from empty), and Empty
- Asynchronous and simultaneous read and write operations
- Dual-ported zero fall-through time architecture
- Retransmit capability in single device mode
- Produced with high performance, low-power CEMOS™ technology
- Available in 28-pin ceramic and plastic DIP, 32-pin LCC and J-leaded PLCC
- Military product compliant to MIL-STD-883, Class B

DESCRIPTION:

The IDT72131/72141 are high-speed, low power parallel-to-serial FIFOs. These FIFOs are ideally suited to serial communications applications, tape/disk controllers, and local area networks (LANs). The IDT72131/72141 can be configured with the IDT's serial-to-parallel FIFOs (IDT72132/72142) for bidirectional serial data buffering.

The FIFO has a 9-bit parallel input port and a serial output port. Wider and deeper parallel-to-serial data buffers can be built using multiple IDT72131/72141 chips. IDT's unique Flexishift™ serial expansion logic (SOX, $\overline{NR}$) makes width expansion possible with no additional components. These FIFOs will expand to a variety of word widths including 8, 9, 16, and 32 bits. The IDT72131/141 can also be directly connected for depth expansion.

Five flags are provided to monitor the FIFO. The full and empty flags prevent any FIFO data overflow or underflow conditions. The almost-full (7/8), half-full, and almost-empty (1/8) flags signal memory utilization within the FIFO.

The IDT72131/72141 is fabricated using IDT's high-speed submicron CEMOS™ technology. Military grade product is manufactured in compliance with the latest revision of MIL-STD-883, Class B.

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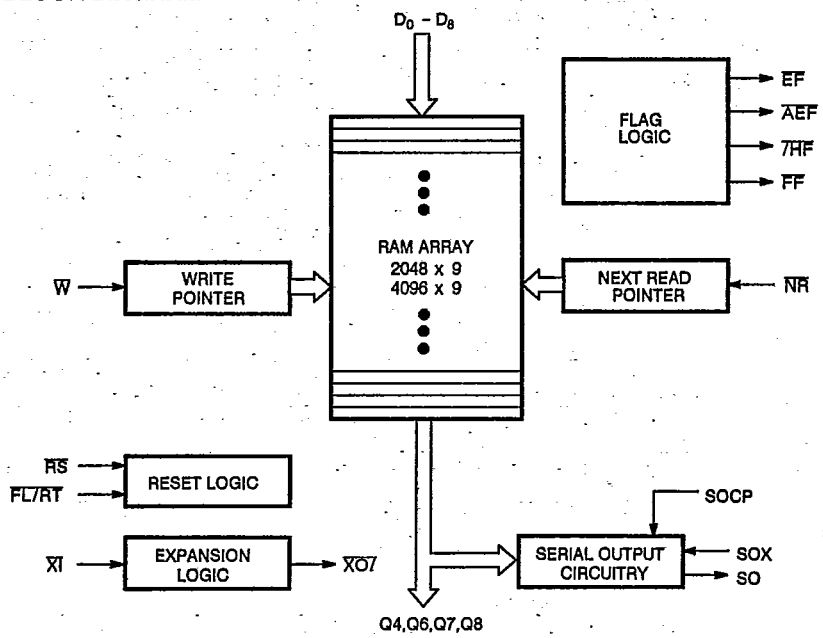
FUNCTIONAL BLOCK DIAGRAM



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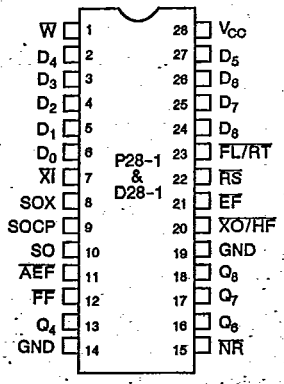
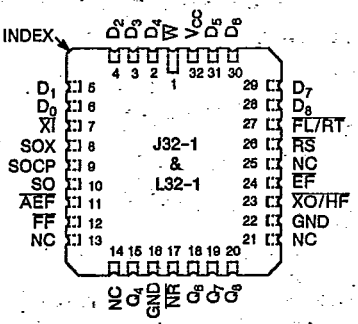
PIN CONFIGURATIONS



DIP
TOP VIEW



LCC/PLCC
TOP VIEW

PIN DESCRIPTIONS

SYMBOL	NAME	I/O	DESCRIPTION
$D_0 - D_8$	Inputs	I	Data Inputs for 9-bit wide data.
$\overline{RS}$	Reset	I	When $\overline{RS}$ is set low, internal READ and WRITE pointers are set to the first location of the RAM array. $\overline{HF}$ and $\overline{FF}$ go high, and $\overline{AEF}$ and $\overline{EF}$ go low. A reset is required before an initial WRITE after power-up. $\overline{W}$ must be high and SCOP low during $\overline{RS}$ cycle. SOCP must have also completed its serial word so that $\overline{NR}$ is high.
$\overline{W}$	Write	I	A write cycle is initiated on the falling edge of WRITE if the Full Flag ($\overline{FF}$) is not set. Data set-up and hold times must be adhered to with respect to the rising edge of WRITE. Data is stored in the RAM array sequentially and independently of any ongoing read operation.
SOCP	Serial Output Clock	I	A serial bit read cycle is initiated on the rising edge of SOCP if the Empty Flag ($\overline{EF}$) is not set. In both Depth and Serial Word Width Expansion modes, all of the SOCP pins are tied together.
$\overline{NR}$	Next Read	I	To program the Serial Out data word width, connect $\overline{NR}$ with one of the Data Set pins (Q_4, Q_6, Q_7 and Q_8). For example, $\overline{NR}$ - Q_7 programs for a 8-bit Serial Out word width.
$\overline{FL/RT}$	First Load/ Retransmit	I	This is a dual purpose input. In the single device configuration ($\overline{XI}$ grounded), activating retransmit ($\overline{FL/RT}$-low) will set the internal READ pointer to the first location. There is no effect on the WRITE pointer. SOCP and W must be high before setting $\overline{FL/RT}$ low. Retransmit is not compatible with depth expansion. In the depth expansion configuration, $\overline{FL/RT}$ grounded indicates the first activated device.
$\overline{XI}$	Expansion In	I	In the single device configuration, $\overline{XI}$ is grounded. In depth expansion or daisy chain expansion, $\overline{XI}$ is connected to $\overline{XO}$ (expansion out) of the previous device.
SOX	Serial Output Expansion	I	In the Serial Output Expansion mode, SOX is tied high on the device that will source the lower order bits of the serial word. The device or devices that source the next higher order serial bits have their SOX pin tied to the Q_8 pin of the device that will source the next lower order bits of the serial word. Data is then clocked out least significant bit first. For single device operation, SOX is tied high.
SO	Serial Output	O	Serial data is output on the Serial Output (SO) pin. Data is clocked out Least Significant Bit first. In the Serial Width Expansion mode the SO pins are tied together and each SO pin is tristated at the end of the byte.
$\overline{FF}$	Full Flag	O	When $\overline{FF}$ goes low, the device is full and further WRITE operations are inhibited. When $\overline{FF}$ is high, the device is not full.
$\overline{EF}$	Empty Flag	O	When $\overline{EF}$ goes low, the device is empty and further READ operations are inhibited. When $\overline{EF}$ is high, the device is not empty.
$\overline{AEF}$	Almost-Empty/ Almost-Full Flag	O	When $\overline{AEF}$ is low, the device is empty to 1/8 full or 7/8 to completely full. When $\overline{AEF}$ is high, the device is greater than 1/8 full, but less than 7/8 full.
$\overline{XO}/\overline{HF}$	Expansion Out/ Half-Full Flag	O	This is a dual purpose output. In the single device configuration ($\overline{XI}$ grounded), the device is more than half full when $\overline{HF}$ is low. In the depth expansion configuration ($\overline{XO}$ connected to $\overline{XI}$ of the next device), a pulse is sent from $\overline{XO}$ to $\overline{XI}$ when the last location in the RAM array is filled.
Q_4, Q_6, Q_7 and Q_8	Data Set	O	The appropriate Data Set pin (Q_4, Q_6, Q_7 or Q_8) is connected to $\overline{NR}$ to program the Serial Out data word width. For example: Q_6 - $\overline{NR}$ programs a 7-bit word width, Q_8 - $\overline{NR}$ programs a 9-bit word width, etc.
V_{CC}	Power Supply		Single Power Supply of 5V.
GND	Ground		Single Ground at 10V.

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STATUS FLAGS

NUMBER OF WORDS IN FIFO		FF	AEF	HF	EF
IDT72131	IDT72141				
0	0	H	L	H	L
1-255	1-511	H	L	H	H
256-1024	512-2048	H	H	H	H
1025-1792	2049-3584	H	H	L	H
1793-2047	3585-4095	H	L	L	H
2048	4096	L	L	L	H

ABSOLUTE MAXIMUM RATINGS (1)

SYMBOL	RATING	COMMERCIAL	MILITARY	UNIT
V_{TERM}	Terminal Voltage with Respect to GND	-0.5 to +7.0	-0.5 to +7.0	V
T_A	Operating Temperature	0 to +70	-55 to +125	°C
T_{BIAS}	Temperature Under Bias	-55 to +125	-65 to +135	°C
T_{STG}	Storage Temperature	-55 to +125	-65 to +150	°C
I_{OUT}	DC Output Current	50	50	mA

NOTE:
1. Stresses greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

RECOMMENDED DC OPERATING CONDITIONS

SYMBOL	PARAMETER	MIN.	TYP.	MAX.	UNIT
V_{CCM}	Military Supply Voltage	4.5	5.0	5.5	V
V_{CC}	Commercial Supply Voltage	4.5	5.0	5.5	V
GND	Supply Voltage	0	0	0	V
V_{IH}	Input High Voltage Commercial	2.0	–	–	V
V_{IH}	Input High Voltage Military	2.2	–	–	V
V_{IL} (1)	Input Low Voltage Commercial & Military	–	–	0.8	V

NOTE:
1. 1.5V undershoots are allowed for 10ns once per cycle.

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DC ELECTRICAL CHARACTERISTICS

(Commercial: V_{CC}= 5V ±10%, T_A = 0°C to +70°C; Military: V_{CC}= 5V ±10%, T_A= -55°C to +125°C)

SYMBOL	PARAMETER	IDT72131/IDT72141 COMMERCIAL			IDT72131/IDT72141 MILITARY			UNIT
		MIN.	TYP.	MAX.	MIN.	TYP.	MAX.	
I_{IL} (1)	Input Leakage Current (Any Input)	-1	–	1	-10	–	10	µA
I_{OL} (2)	Output Leakage Current	-10	–	10	-10	–	10	µA
V_{OH}	Output Logic "1" Voltage	2.4	–	–	2.4	–	–	V
V_{OL}	Output Logic "0" Voltage	–	–	0.4	–	–	0.4	V
I_{CC1} (3)	Power Supply Current	–	90	140	–	100	160	mA
I_{CC2} (3)	Average Standby Current ($\overline{R}$ = $\overline{W}$ = $\overline{RST}$ = $\overline{FL}/\overline{RT}$ = V_{IH})	–	8	12	–	12	25	mA
I_{CC3} (L) (3, 4)	Power Down Current	–	–	2	–	–	4	mA
I_{CC3} (S) (3, 4)	Power Down Current	–	–	8	–	–	12	mA

NOTES:
1. Measurements with 0.4 ≤ V_{IN} ≤ V_{OUT}.
2. $\overline{R}$ ≥ V_{IH}, 0.4 ≤ V_{OUT} ≤ V_{CC}
3. I_{CC} measurements are made with outputs open.
4. $\overline{RS}$ = $\overline{FL}/\overline{RT}$ = $\overline{W}$ = $\overline{R}$ = V_{CC}-0.2V; all other inputs ≥ V_{CC} -0.2V or ≤ 0.2V

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AC ELECTRICAL CHARACTERISTICS[1]

(Commercial: V_{CC} = 5V ±10%, T_A = 0°C to +70°C; Military: V_{CC} = 5V ±10%, T_A = -55°C to +125°C)

SYMBOL	PARAMETER	COM'L 72131x35 72141x35		MIL. 72131x40 72141x40		MILITARY AND COMMERCIAL 72131x50 72141x50		72131x65 72141x65		72131x80 72141x80		72131x120 72141x120		UNIT
		MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	
t_S	Parallel Shift Frequency	–	22.2	–	20	–	15	–	12.5	–	10	–	7	MHz
t_{SOCP}	Serial-Out Shift Frequency	–	50	–	50	–	40	–	33	–	28	–	25	MHz
PARALLEL INPUT MODE TIMINGS														
t_{DS}	Data Set-up Time	18	–	20	–	30	–	30	–	40	–	40	–	ns
t_{DH}	Data Hold Time	0	–	0	–	5	–	10	–	10	–	10	–	ns
t_{WC}	Write Cycle Time	45	–	50	–	65	–	80	–	100	–	140	–	ns
t_{WPW}	Write Pulse Width	35	–	40	–	50	–	65	–	80	–	120	–	ns
t_{WR}	Write Recovery Time	10	–	10	–	15	–	15	–	20	–	20	–	ns
t_{WEF}	Write High to $\overline{EF}$ High	–	30	–	35	–	45	–	60	–	60	–	60	ns
t_{WFF}	Write Low to $\overline{FF}$ Low	–	30	–	35	–	45	–	60	–	60	–	60	ns
t_{WF}	Write Low to Transitioning $\overline{HF}$, $\overline{AEF}$	–	45	–	50	–	65	–	80	–	100	–	140	ns
t_{WPF}	Write Pulse Width After $\overline{FF}$ High	35	–	40	–	50	–	65	–	80	–	120	–	ns
SERIAL OUTPUT MODE TIMIMGS														
t_{SOHZ}	SOCP Rising Edge to SO at High Z[1]	5	16	5	16	5	26	5	20	5	25	5	35	ns
t_{SOLZ}	SOCP Rising Edge to SO at Low Z[1]	5	22	5	22	5	22	5	22	5	30	5	35	ns
t_{SOPD}	SOCP Rising Edge to Valid Data on SO	–	18	–	18	–	18	–	22	–	30	–	35	ns
t_{SOX}	SOX Set-up Time to SOCP Rising Edge	5	–	5	–	5	–	5	–	5	–	5	–	ns
t_{SOCW}	Serial In Clock Width High/Low	8	–	8	–	10	–	10	–	15	–	15	–	ns
t_{SOCEF}	SOCP Rising Edge (Bit 0 – First Word) to $\overline{EF}$ Low	–	20	–	25	–	25	–	30	–	30	–	30	ns
t_{SOCFF}	SOCP Rising Edge to $\overline{FF}$ High	–	30	–	35	–	40	–	50	–	60	–	65	ns
t_{SOCF}	SOCP Rising Edge to $\overline{HF}$, $\overline{AEF}$, High	–	30	–	35	–	40	–	50	–	60	–	65	ns
t_{REFSO}	Recovery Time SOCP After $\overline{EF}$ High	35	–	40	–	50	–	65	–	80	–	120	–	ns
RESET TIMINGS														
t_{RSC}	Reset Cycle Time	45	–	50	–	65	–	80	–	100	–	140	–	ns
t_{RS}	Reset Pulse Width	35	–	40	–	50	–	65	–	80	–	120	–	ns
t_{RSS}	Reset Set-up Time	35	–	40	–	50	–	65	–	80	–	120	–	ns
t_{RSR}	Reset Recovery Time	10	–	10	–	15	–	15	–	20	–	20	–	ns
t_{RSF1}	Reset to $\overline{EF}$ and $\overline{AEF}$ Low	–	45	–	50	–	65	–	80	–	100	–	140	ns
t_{RSF2}	Reset to $\overline{HF}$ and $\overline{FF}$ High	–	45	–	50	–	65	–	80	–	100	–	140	ns
RETRANSMIT TIMINGS														
t_{RTC}	Retransmit Cycle Time	45	–	50	–	65	–	80	–	100	–	140	–	ns
t_{RT}	Retransmit Pulse Width	35	–	40	–	50	–	65	–	80	–	120	–	ns
t_{RTS}	Retransmit Set-up Time	35	–	40	–	50	–	65	–	80	–	120	–	ns
t_{RTR}	Retransmit Recovery Time	10	–	10	–	15	–	15	–	20	–	20	–	ns
DEPTH EXPANSION MODE DELAYS														
t_{XOL}	Read/Write to $\overline{XO}$ Low	–	35	–	40	–	50	–	65	–	80	–	120	ns
t_{XOH}	Read/Write to $\overline{XO}$ High	–	35	–	40	–	50	–	65	–	80	–	120	ns
t_X	$\overline{XI}$ Pulse Width	35	–	40	–	50	–	65	–	80	–	120	–	ns
t_{XIR}	$\overline{XI}$ Recovery Time	10	–	10	–	10	–	10	–	10	–	10	–	ns
t_{XIS}	$\overline{XI}$ Set-up Time	15	–	15	–	15	–	15	–	15	–	15	–	ns

NOTE: 1. Guaranteed by design minimum times, not tested.

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AC TEST CONDITIONS

Input Pulse Levels	GND to 3.0V
Input Rise/Fall Times	3ns
Input Timing Reference Levels	1.5V
Output Reference Levels	1.5V
Output Load	See Figure 1

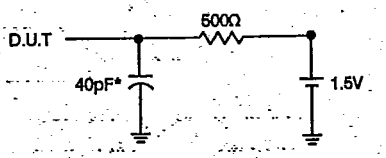

Figure A. Output Load.

*Includes jig and scope capacitances.

CAPACITANCE (T_A = +25°C, f = 1.0MHz)

SYMBOL	PARAMETER[1]	CONDITIONS	MAX.	UNIT
C_{IN}	Input Capacitance	V_{IN} = 0V	10	pF
C_{OUT}	Output Capacitance	V_{OUT} = 0V	12	pF

NOTE:
1. This parameter is sampled and not 100% tested.

FUNCTIONAL DESCRIPTION

Parallel Data Input

The data is written into the FIFO in parallel through the D_{0-8} input data lines. A write cycle is initiated on the falling edge of the Write ($\overline{W}$) signal provided the Full Flag ($\overline{FF}$) is not asserted. If the $\overline{W}$ signal changes from HIGH-to-LOW and the Full Flag ($\overline{FF}$) is already set, the write line is inhibited internally from incrementing the write pointer and no write operation occurs.

Data set-up and hold times must be met with respect to the rising edge of Write. The data is written to the RAM at the write pointer. On the rising edge of $\overline{W}$, the write pointer is incremented. Write operations can occur simultaneously or asynchronously with read operations.

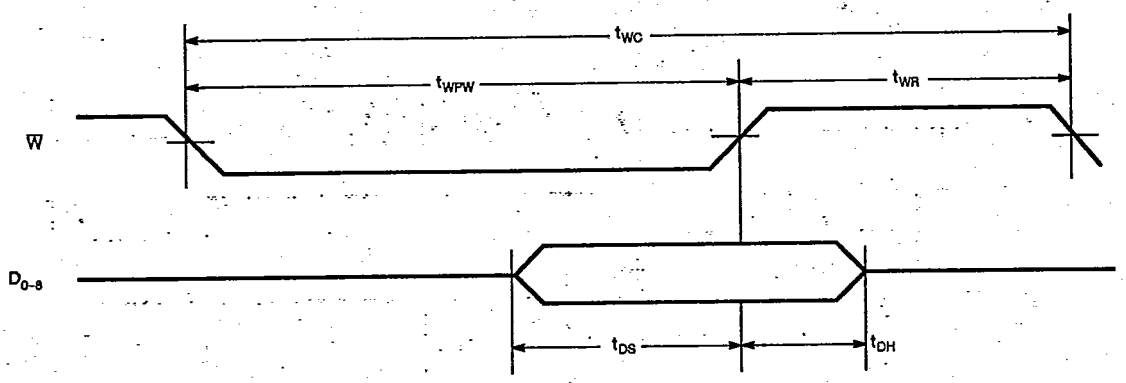

Figure 1. Write Operation

Serial Data Output

The serial data is output on the SO pin. The data is clocked out on the rising edge of SOCP providing the Empty Flag ($\overline{EF}$) is not asserted. If the Empty Flag is asserted then the next data word is inhibited from moving to the output register and being clocked out by SOCP. NOTE: SOCP should not be clocked while the Empty Flag is low. If it is, then two things will occur. One, invalid data will be read by SOCP and two, SOCP will be out of sync with Next Read ($\overline{NR}$).

The serial word is shifted out Least Significant Bit first, that is the first bit will be D_0, then D_1 and so on up to the serial word width. The serial word width must be programmed by connecting the appropriate Data Set line (Q_4, Q_6, Q_7, or Q_8) to the $\overline{NR}$ input. The Data Set lines are taps off a digital delay line. Selecting one of these taps, programs the width of the serial word to be read and shifted out.

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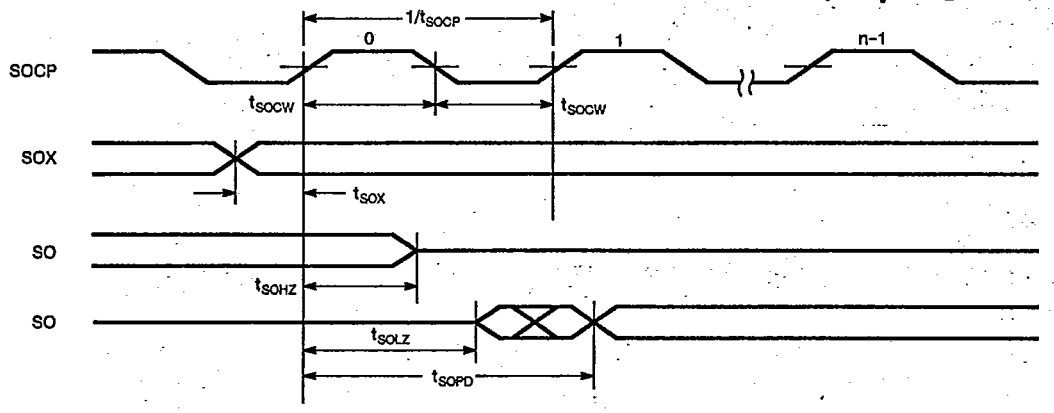

Figure 2. Read Operation

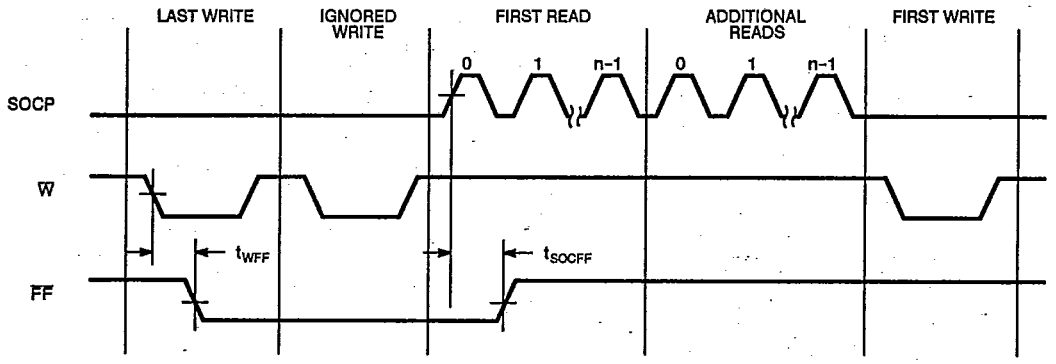

Figure 3. Full Flag from Last Write to First Read

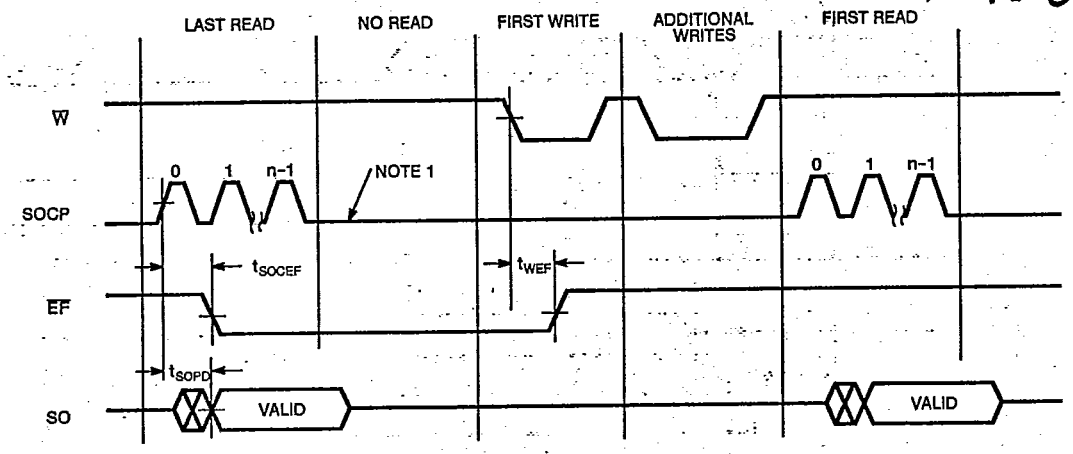

Figure 4. Empty Flag from Last Read to First Write

NOTE:
1. SOCP should not be clocked until $\overline{EF}$ goes high.

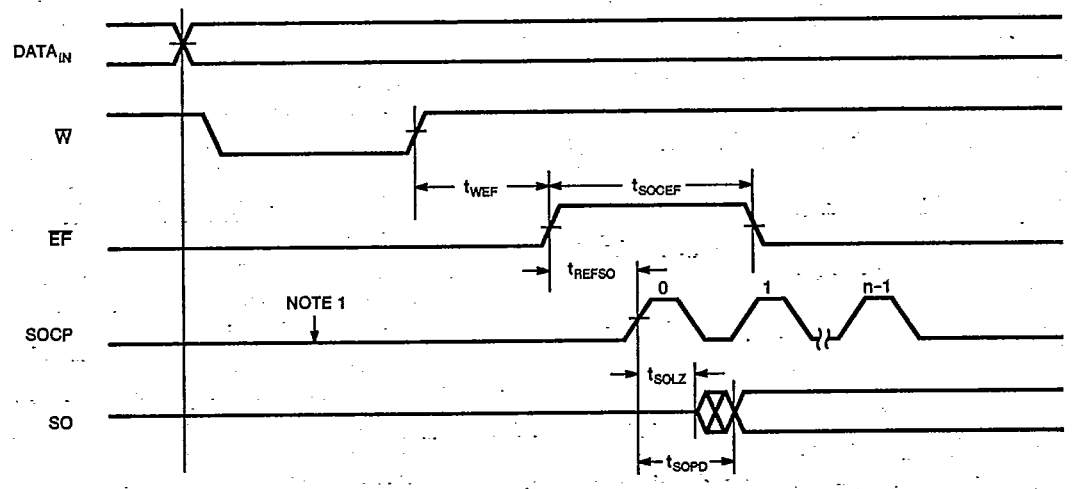

Figure 5. Empty Boundry Condition Timing

NOTE:
1. SOCP should not be clocked until $\overline{EF}$ goes high.

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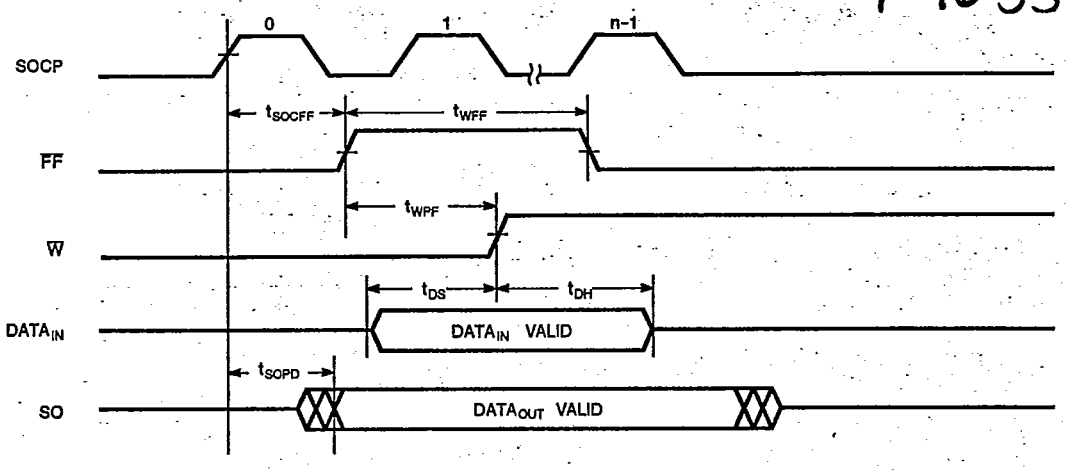

Figure 6. Full Boundry Condition Timing

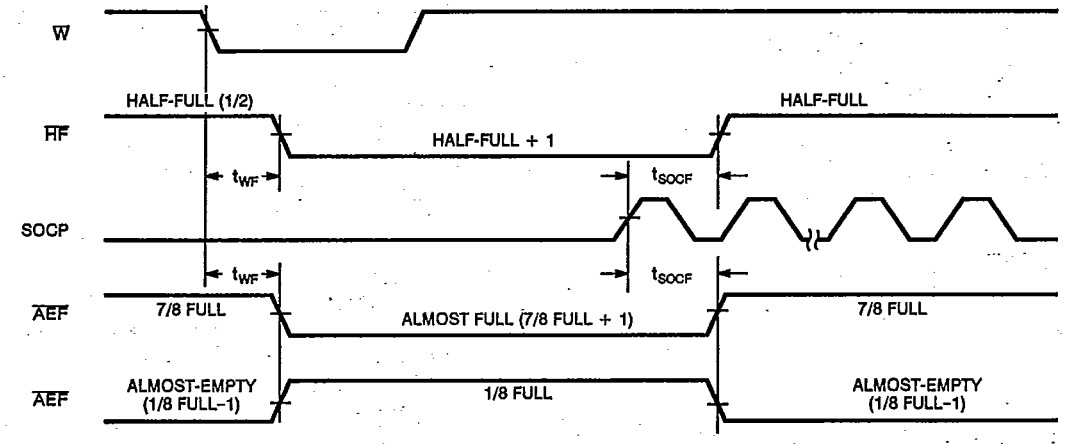

Figure 7. Half Full, Almost Full and Almost Empty Timings

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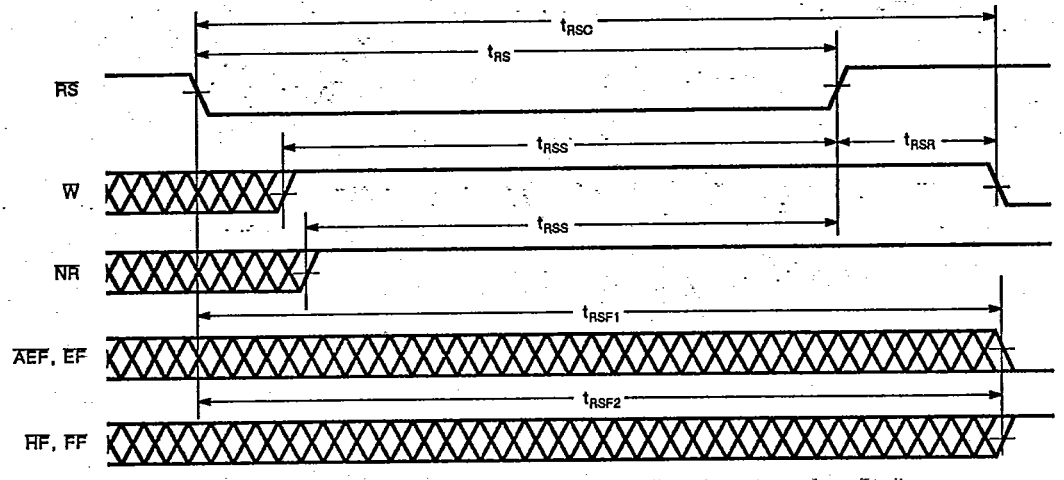

Figure 8. Reset

NOTES:
1. EF, FF and HF may change status during Reset, but flags will be valid at t_{RSC}.
2. NR is set high by SOCP staying low at the completion of a serial word.

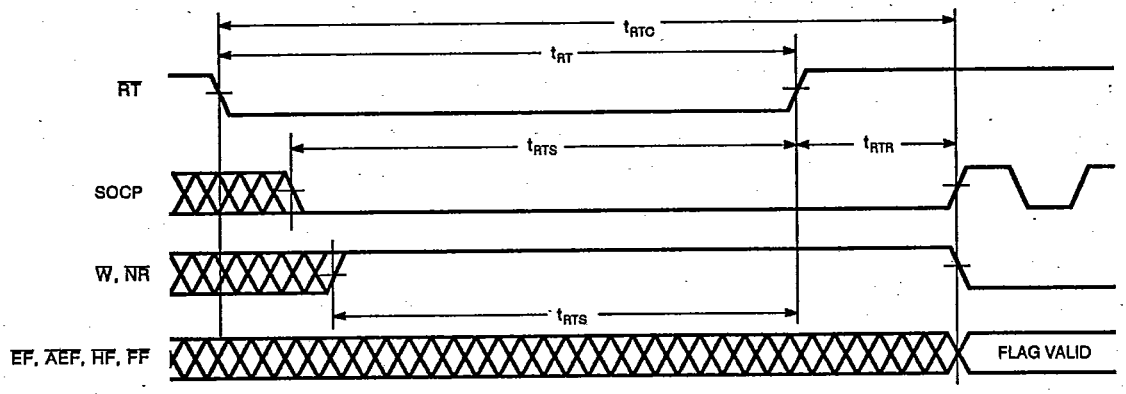

Figure 9. Retransmit

NOTE:
1. EF, AEF, HF and FF may change status during Retransmit, but flags will be valid at t_{RTC}.

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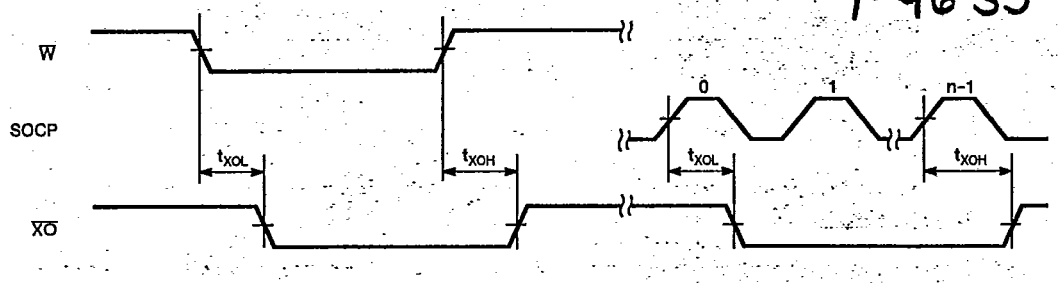

Figure 10. Expansion-Out

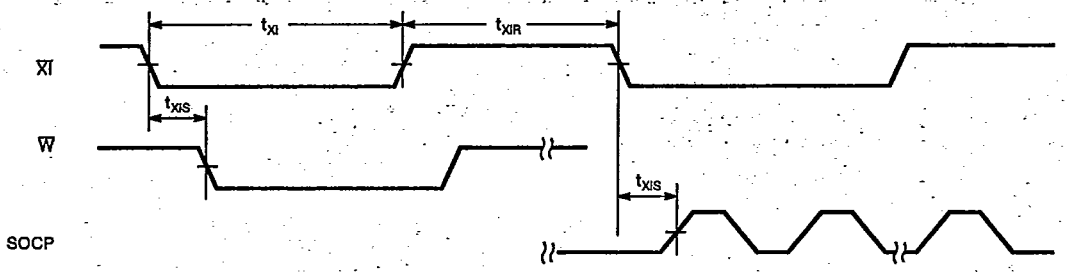

Figure 11. Expansion-In

OPERATING CONFIGURATIONS

Single Device Configuration

In the standalone case, the SOX line is tied HIGH and not used. On the first LOW-to-HIGH of the SOCP clock, all of the Data Set lines (Q_4, Q_8) go low and a new serial word is started. The Data Set lines then go high on the equivalent SOCP clock pulse. This continues until the Q line connected to NR goes high completing the serial word. The cycle is then repeated with the next LOW-to-HIGH transition of SOCP.

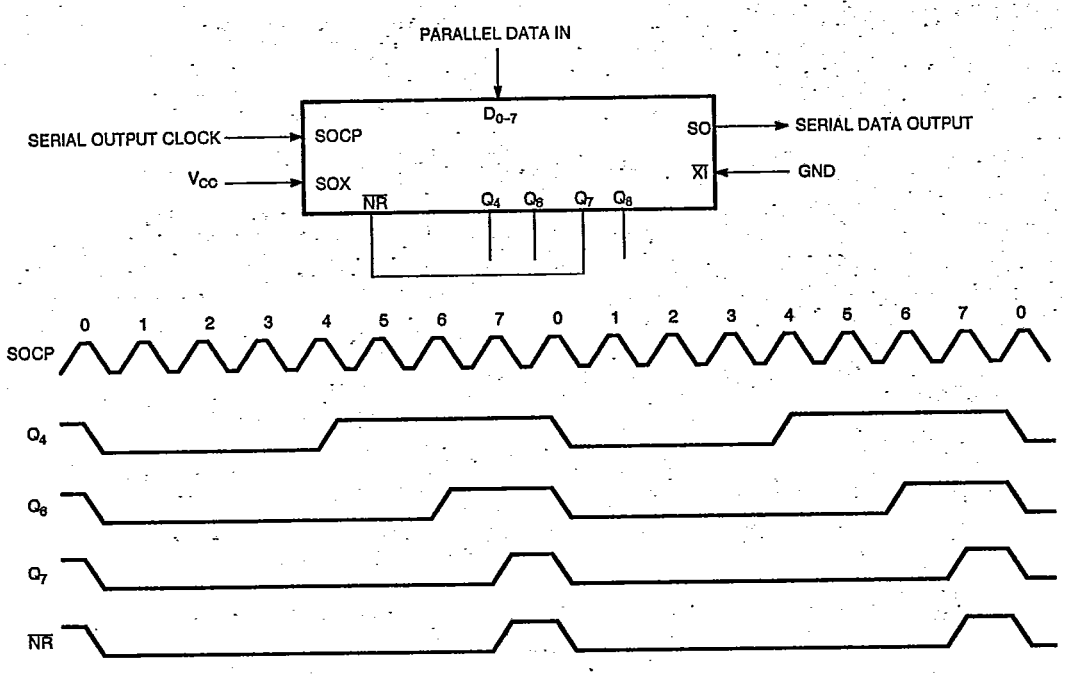

Figure 12. Eight-Bit Word Single Device Configuration

TRUTH TABLES

TABLE 1: RESET AND RETRANSMIT– SINGLE DEVICE CONFIGURATION/WIDTH EXPANSION MODE

MODE	INPUTS			INTERNAL STATUS		OUTPUTS		
	$\overline{RS}$	$\overline{FL}$	$\overline{XI}$	READ POINTER	WRITE POINTER	$\overline{AEF}$, $\overline{EF}$	$\overline{FF}$	$\overline{HF}$
Reset	0	X	0	Location Zero	Location Zero	0	1	1
Retransmit	1	0	0	Location Zero	Unchanged	X	X	X
Read/Write	1	1	0	Increment(1)	Increment(1)	X	X	X

NOTE:
1. Pointer will increment if appropriate flag is HIGH.

Width Expansion Configuration

In the cascaded case, word widths of more than 9 bits can be achieved by using more than one device. By tying the SOX line of the least significant device HIGH and the SOX of the subsequent devices to the appropriate Data Set lines of the previous devices, a cascaded serial word is achieved.

On the first LOW-to-HIGH clock edge of SOCP, all the lines go LOW. Just as in the standalone case, on each corresponding clock cycle, the equivalent Data Set line goes HIGH in order of least to most significant. When the Data Set line which is connected to the SOX input of the next device goes HIGH, the D_0 of that device goes HIGH, thus cascading from one device to the next. The Data Set line of the most significant bit programs the serial word width by being connected to all NR inputs.

The Serial Data Output (SO) of each device in the serial word must be tied together. Since the SO pin is three stated, only the device which is currently shifting out is enabled and driving the 1-bit bus.

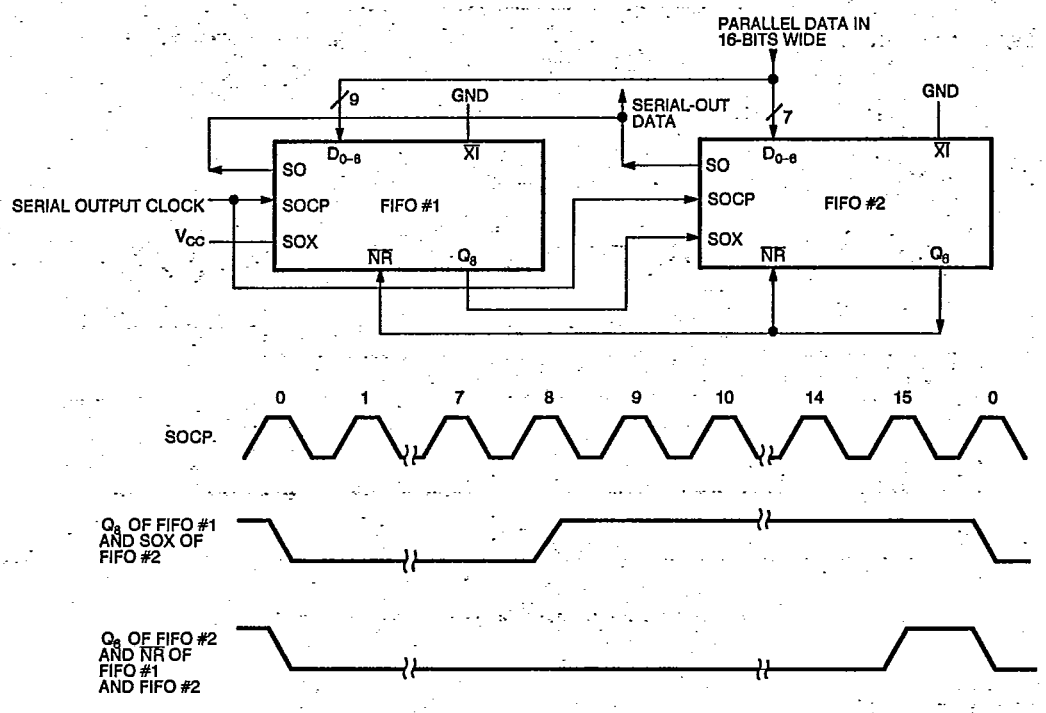

Figure 13. Width Expansion for 16-bit Parallel Data In. The Parallel Data In is tied to D_{0-8} of FIFO #1 and D_{0-8} of FIFO #2

Depth Expansion (Daisy Chain) Mode

The IDT72131/41 can be easily adapted to applications where the requirements are for greater than 2048/4096 words. Figure 14 demonstrates Depth Expansion using three IDT72131/41. Any depth can be attained by adding additional IDT72131/41. The IDT72131/41 operates in the Depth Expansion configuration when the following conditions are met:

1. The first device must be designated by grounding the First Load ($\overline{FL}$) control input.
2. All other devices must have $\overline{FL}$ in the high state.
3. The Expansion Out ($\overline{XO}$) pin of each device must be tied to the Expansion In ($\overline{XI}$) pin of the next device.
4. External logic is needed to generate a composite Full Flag ($\overline{FF}$) and Empty Flag ($\overline{EF}$). This requires the OR-ing of all $\overline{EF}$s and OR-ing of all $\overline{FF}$s (i.e., all must be set to generate the correct composite $\overline{FF}$ or $\overline{EF}$).
5. The Retransmit ($\overline{RT}$) function and Half-Full Flag ($\overline{HF}$) are not available in the Depth Expansion mode.

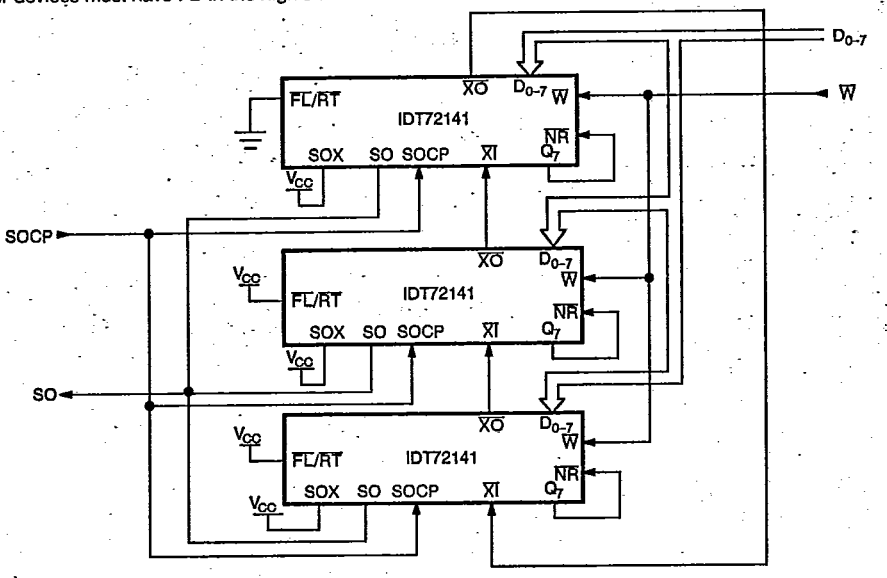

Figure 14. An 12K x 8 Parallel-In Serial-Out FIFO

TABLE 2: RESET AND FIRST LOAD TRUTH TABLE — DEPTH EXPANSION/COMPOUND EXPANSION MODE

MODE	INPUTS			INTERNAL STATUS		OUTPUTS	
	$\overline{RS}$	$\overline{FL}$	$\overline{XI}$	READ POINTER	WRITE POINTER	$\overline{EF}$	$\overline{FF}$
Reset-First Device	0	0	(1)	Location Zero	Location Zero	0	1
Reset all Other Devices	0	1	(1)	Location Zero	Location Zero	0	1
Read/Write	1	X	(1)	X	X	X	X

NOTES:

1. $\overline{XI}$ is connected to $\overline{XO}$ of previous device.
2. $\overline{RS}$ = Reset Input, $\overline{FL}/\overline{RT}$ = First Load/Retransmit, $\overline{EF}$ = Empty Flag Output, $\overline{FF}$ = Full Flag Output, $\overline{XI}$ = Expansion Input

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