128K X 36, 256K X 18 3.3V Synchronous SRAMs 2.5V I/O, Pipelined Outputs, Burst Counter, Single Cycle Deselect

IDT71V25761
IDT71V25781

Features

- **128K x 36, 256K x 18 memory configurations**
- **Supports high system speed:**
  Commercial:
  – *200MHz 3.1ns clock access time*
  Commercial and Industrial:
  – *183MHz 3.3ns clock access time*
  – *166MHz 3.5ns clock access time*
- **$\overline{LBO}$ input selects interleaved or linear burst mode**
- **Self-timed write cycle with global write control ($\overline{GW}$), byte write enable ($\overline{BWE}$), and byte writes ($\overline{BW}$x)**
- **3.3V core power supply**
- **Power down controlled by ZZ input**
- **2.5V I/O**
- **Packaged in a JEDEC Standard 100-pin plastic thin quad flatpack (TQFP), 119 ball grid array (BGA) and 165 fine pitch ball grid array**

Description

The IDT71V25761/781 are high-speed SRAMs organized as 128K x 36/256K x 18. The IDT71V25761/781 SRAMs contain write, data, address and control registers. Internal logic allows the SRAM to generate a self-timed write based upon a decision which can be left until the end of the write cycle.

The burst mode feature offers the highest level of performance to the system designer, as the IDT71V25761/718 can provide four cycles of data for a single address presented to the SRAM. An internal burst address counter accepts the first cycle address from the processor, initiating the access sequence. The first cycle of output data will be pipelined for one cycle before it is available on the next rising clock edge. If burst mode operation is selected ($\overline{ADV}$=LOW), the subsequent three cycles of output data will be available to the user on the next three rising clock edges. The order of these three addresses are defined by the internal burst counter and the $\overline{LBO}$ input pin.

The IDT71V25761/781 SRAMs utilize IDT's latest high-performance CMOS process and are packaged in a JEDEC standard 14mm x 20mm 100-pin thin plastic quad flatpack (TQFP) as well as a 119 ball grid array (BGA) and 165 fine pitch ball grid array (fBGA).

Pin Description Summary

A_0-A_{17}	Address Inputs	Input	Synchronous
$\overline{CE}$	Chip Enable	Input	Synchronous
CS_0, $\overline{CS_1}$	Chip Selects	Input	Synchronous
$\overline{OE}$	Output Enable	Input	Asynchronous
$\overline{GW}$	Global Write Enable	Input	Synchronous
$\overline{BWE}$	Byte Write Enable	Input	Synchronous
$\overline{BW_1}$, $\overline{BW_2}$, $\overline{BW_3}$, $\overline{BW_4}$(1)	Individual Byte Write Selects	Input	Synchronous
CLK	Clock	Input	N/A
$\overline{ADV}$	Burst Address Advance	Input	Synchronous
$\overline{ADSC}$	Address Status (Cache Controller)	Input	Synchronous
$\overline{ADSP}$	Address Status (Processor)	Input	Synchronous
$\overline{LBO}$	Linear / Interleaved Burst Order	Input	DC
ZZ	Sleep Mode	Input	Asynchronous
I/O_0-I/O_{31}, I/O_{P1}-I/O_{P4}	Data Input / Output	I/O	Synchronous
V_{DD}, V_{DDQ}	Core Power, I/O Power	Supply	N/A
V_{SS}	Ground	Supply	N/A

5297 tbl 01

NOTE:
1. $\overline{BW_3}$ and $\overline{BW_4}$ are not applicable for the IDT71V25781.

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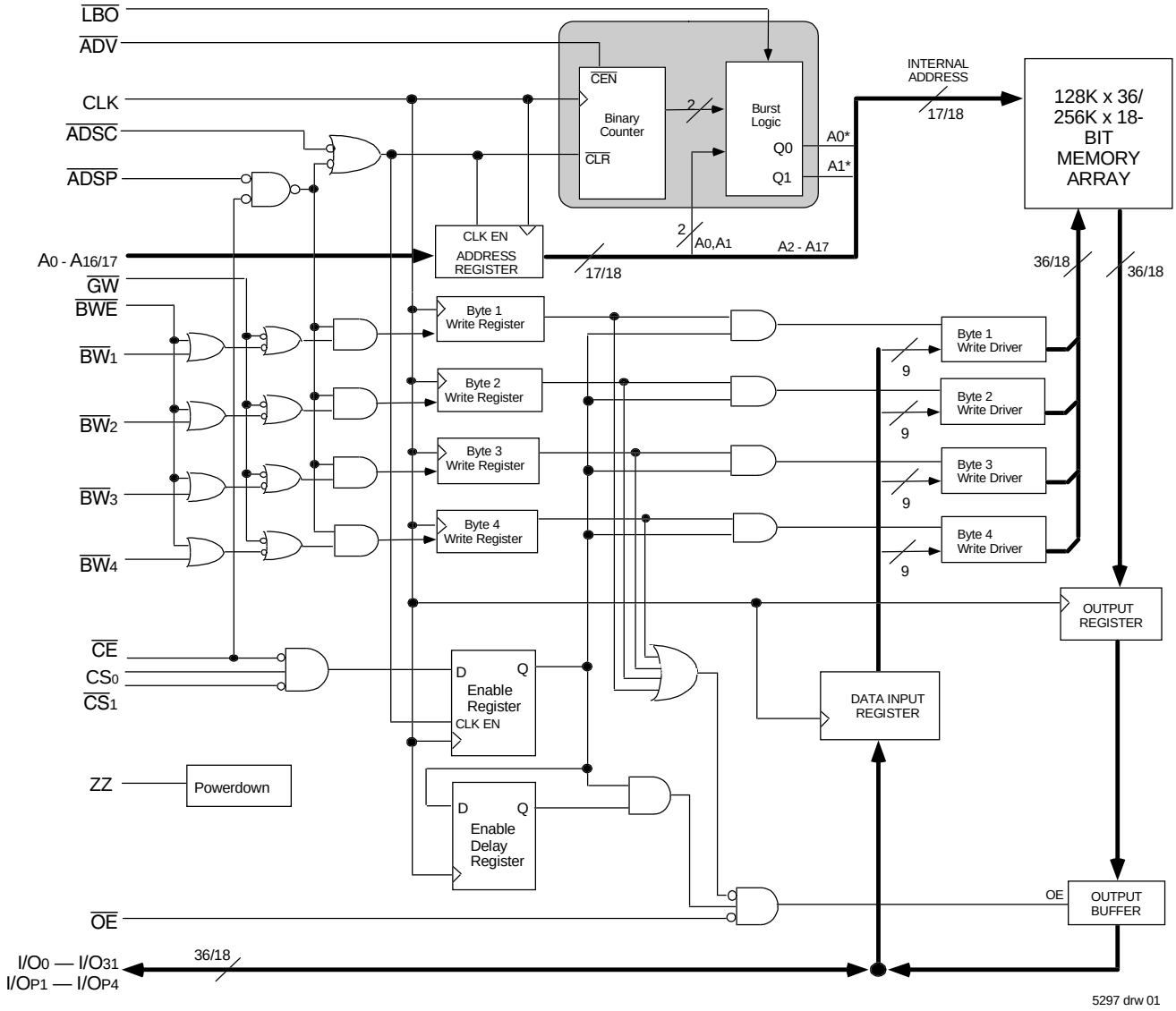
Pin Definitions(1)

Symbol	Pin Function	I/O	Active	Description
A_0-A_{17}	Address Inputs	I	N/A	Synchronous Address inputs. The address register is triggered by a combination of the rising edge of CLK and $\overline{ADSC}$ Low or $\overline{ADSP}$ Low and $\overline{CE}$ Low.
$\overline{ADSC}$	Address Status (Cache Controller)	I	LOW	Synchronous Address Status from Cache Controller. $\overline{ADSC}$ is an active LOW input that is used to load the address registers with new addresses.
$\overline{ADSP}$	Address Status (Processor)	I	LOW	Synchronous Address Status from Processor. $\overline{ADSP}$ is an active LOW input that is used to load the address registers with new addresses. $\overline{ADSP}$ is gated by $\overline{CE}$.
$\overline{ADV}$	Burst Address Advance	I	LOW	Synchronous Address Advance. $\overline{ADV}$ is an active LOW input that is used to advance the internal burst counter, controlling burst access after the initial address is loaded. When the input is HIGH the burst counter is not incremented; that is, there is no address advance.
$\overline{BWE}$	Byte Write Enable	I	LOW	Synchronous byte write enable gates the byte write inputs $\overline{BW_1}$-$\overline{BW_4}$. If $\overline{BWE}$ is LOW at the rising edge of CLK then $\overline{BW}$x inputs are passed to the next stage in the circuit. If $\overline{BWE}$ is HIGH then the byte write inputs are blocked and only $\overline{GW}$ can initiate a write cycle.
$\overline{BW_1}$-$\overline{BW_4}$	Individual Byte Write Enables	I	LOW	Synchronous byte write enables. $\overline{BW_1}$ controls I/O_{0-7}, I/O_{P1}, $\overline{BW_2}$ controls I/O_{8-15}, I/O_{P2}, etc. Any active byte write causes all outputs to be disabled.
$\overline{CE}$	Chip Enable	I	LOW	Synchronous chip enable. $\overline{CE}$ is used with CS_0 and $\overline{CS_1}$ to enable the IDT71V25761/781. $\overline{CE}$ also gates $\overline{ADSP}$.
CLK	Clock	I	N/A	This is the clock input. All timing references for the device are made with respect to this input.
CS_0	Chip Select 0	I	HIGH	Synchronous active HIGH chip select. CS_0 is used with $\overline{CE}$ and $\overline{CS_1}$ to enable the chip.
$\overline{CS_1}$	Chip Select 1	I	LOW	Synchronous active LOW chip select. $\overline{CS_1}$ is used with $\overline{CE}$ and CS_0 to enable the chip.
$\overline{GW}$	Global Write Enable	I	LOW	Synchronous global write enable. This input will write all four 9-bit data bytes when LOW on the rising edge of CLK. $\overline{GW}$ supersedes individual byte write enables.
I/O_0-I/O_{31} I/O_{P1}-I/O_{P4}	Data Input/Output	I/O	N/A	Synchronous data input/output (I/O) pins. Both the data input path and data output path are registered and triggered by the rising edge of CLK.
$\overline{LBO}$	Linear Burst Order	I	LOW	Asynchronous burst order selection input. When $\overline{LBO}$ is HIGH, the interleaved burst sequence is selected. When $\overline{LBO}$ is LOW the Linear burst sequence is selected. $\overline{LBO}$ is a static input and must not change state while the device is operating.
$\overline{OE}$	Output Enable	I	LOW	Asynchronous output enable. When $\overline{OE}$ is LOW the data output drivers are enabled on the I/O pins if the chip is also selected. When $\overline{OE}$ is HIGH the I/O pins are in a high-impedance state.
V_{DD}	Power Supply	N/A	N/A	3.3V core power supply.
V_{DDQ}	Power Supply	N/A	N/A	2.5V I/O Supply.
V_{SS}	Ground	N/A	N/A	Ground.
NC	No Connect	N/A	N/A	NC pins are not electrically connected to the device.
ZZ	Sleep Mode	I	HIGH	Asynchronous sleep mode input. ZZ HIGH will gate the CLK internally and power down the IDT71V25761/781 to its lowest power consumption level. Data retention is guaranteed in Sleep Mode.

5297 tbl 02

NOTE:
1. All synchronous inputs must meet specified setup and hold times with respect to CLK.

Functional Block Diagram



Absolute Maximum Ratings(1)

Symbol	Rating	Commercial & Industrial	Unit
V_{TERM}(2)	Terminal Voltage with Respect to GND	-0.5 to +4.6	V
V_{TERM}(3,6)	Terminal Voltage with Respect to GND	-0.5 to V_{DD}	V
V_{TERM}(4,6)	Terminal Voltage with Respect to GND	-0.5 to V_{DD} +0.5	V
V_{TERM}(5,6)	Terminal Voltage with Respect to GND	-0.5 to V_{DDQ} +0.5	V
T_A(7)	**Commercial** Operating Temperature	-0 to +70	°C
	Industrial Operating Temperature	-40 to +85	°C
T_{BIAS}	Temperature Under Bias	-55 to +125	°C
T_{STG}	Storage Temperature	-55 to +125	°C
P_T	Power Dissipation	2.0	W
I_{OUT}	DC Output Current	50	mA

5297 tbl 03

NOTES:
1. Stresses greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.
2. V_{DD} terminals only.
3. V_{DDQ} terminals only.
4. Input terminals only.
5. I/O terminals only.
6. This is a steady-state DC parameter that applies after the power supplies have ramped up. Power supply sequencing is not necessary; however, the voltage on any input or I/O pin cannot exceed V_{DDQ} during power supply ramp up.
7. T_A is the "instant on" case temperature.

Recommended Operating Temperature and Supply Voltage

Grade	Temperature(1)	Vss	V_{DD}	V_{DDQ}
Commercial	0°C to +70°C	0V	3.3V±5%	2.5V±5%
Industrial	-40°C to +85°C	0V	3.3V±5%	2.5V±5%

5297 tbl 04

NOTES:
1. T_A is the "instant on" case temperature.

Recommended DC Operating Conditions

Symbol	Parameter	Min.	Typ.	Max.	Unit
V_{DD}	Core Supply Voltage	3.135	3.3	3.465	V
V_{DDQ}	I/O Supply Voltage	2.375	2.5	2.625	V
V_{SS}	Supply Voltage	0	0	0	V
V_{IH}	Input High Voltage - Inputs	1.7	—	V_{DD} +0.3	V
V_{IH}	Input High Voltage - I/O	1.7	—	V_{DDQ} +0.3(1)	V
V_{IL}	Input Low Voltage	-0.3(2)	—	0.7	V

5297 tbl 05

NOTES:
1. V_{IH} (max) = V_{DDQ} + 1.0V for pulse width less than $t_{CYC/2}$, once per cycle.
2. V_{IL} (min) = -1.0V for pulse width less than $t_{CYC/2}$, once per cycle.

100 pin TQFP Capacitance
(T_A = +25°C, f = 1.0MHz)

Symbol	Parameter(1)	Conditions	Max.	Unit
C_{IN}	Input Capacitance	V_{IN} = 3dV	5	pF
$C_{I/O}$	I/O Capacitance	V_{OUT} = 3dV	7	pF

5297 tbl 07

119 BGA Capacitance
(T_A = +25°C, f = 1.0MHz)

Symbol	Parameter(1)	Conditions	Max.	Unit
C_{IN}	Input Capacitance	V_{IN} = 3dV	7	pF
$C_{I/O}$	I/O Capacitance	V_{OUT} = 3dV	7	pF

5297 tbl 07a

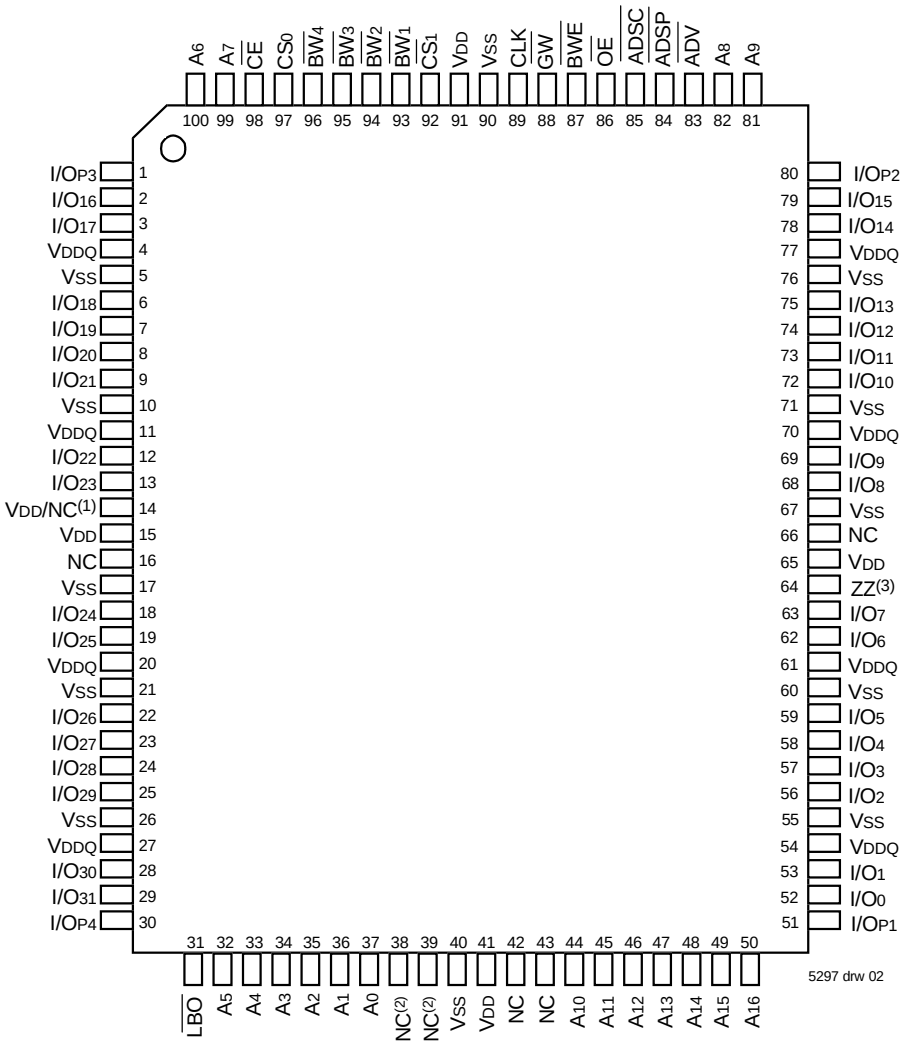
165 fBGA Capacitance
(T_A = +25°C, f = 1.0MHz)

Symbol	Parameter(1)	Conditions	Max.	Unit
C_{IN}	Input Capacitance	V_{IN} = 3dV	TBD	pF
$C_{I/O}$	I/O Capacitance	V_{OUT} = 3dV	TBD	pF

5297 tbl 07b

NOTE:
1. This parameter is guaranteed by device characterization, but not production tested.

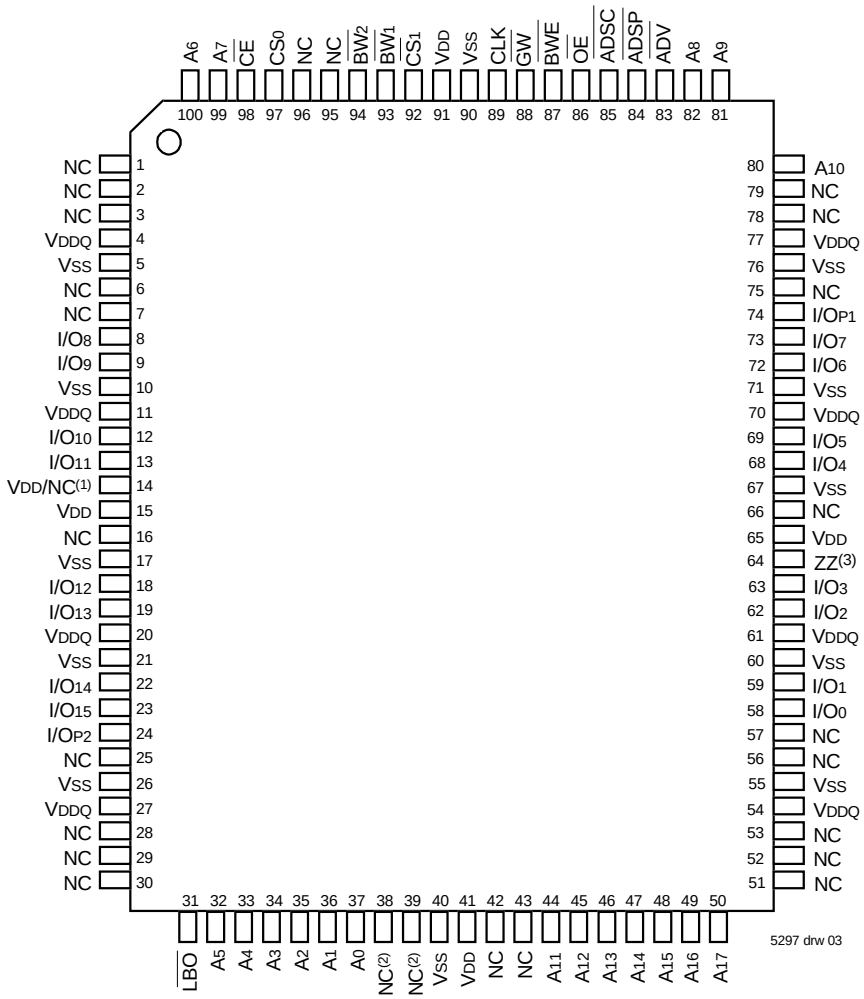
Pin Configuration – 128K x 36



100 TQFP
Top View

NOTES:
1. Pin 14 can either be directly connected to V_{DD}, or connected to an input voltage ≥ V_{IH}, or left unconnected.
2. Pins 38 and 39 can be either NC or connected to V_{SS}.
3. Pin 64 can be left unconnected and the device will always remain in active mode.

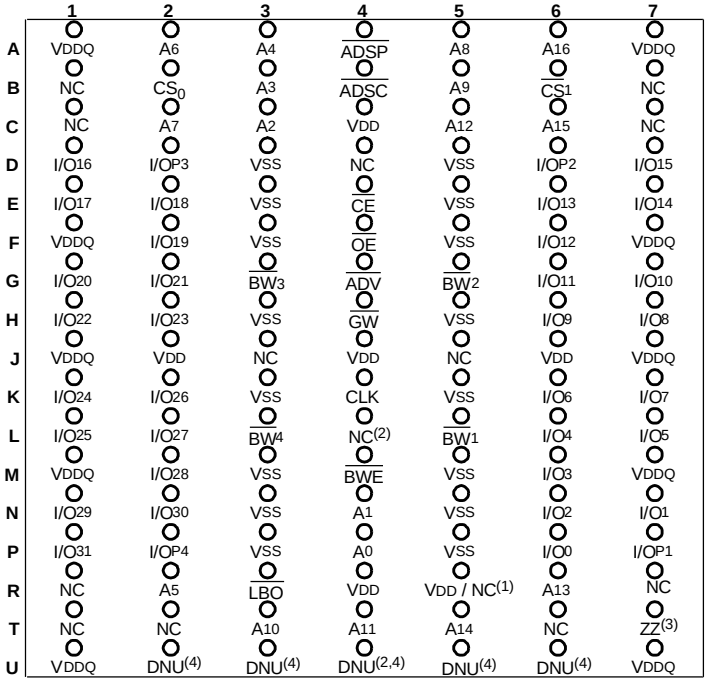
Pin Configuration – 256K x 18



100 TQFP
Top View

NOTES:
1. Pin 14 can either be directly connected to V_{DD}, or connected to an input voltage $\geq V_{IH}$, or left unconnected.
2. Pins 38 and 39 can be either NC or connected to V_{SS}.
3. Pin 64 can be left unconnected and the device will always remain in active mode.

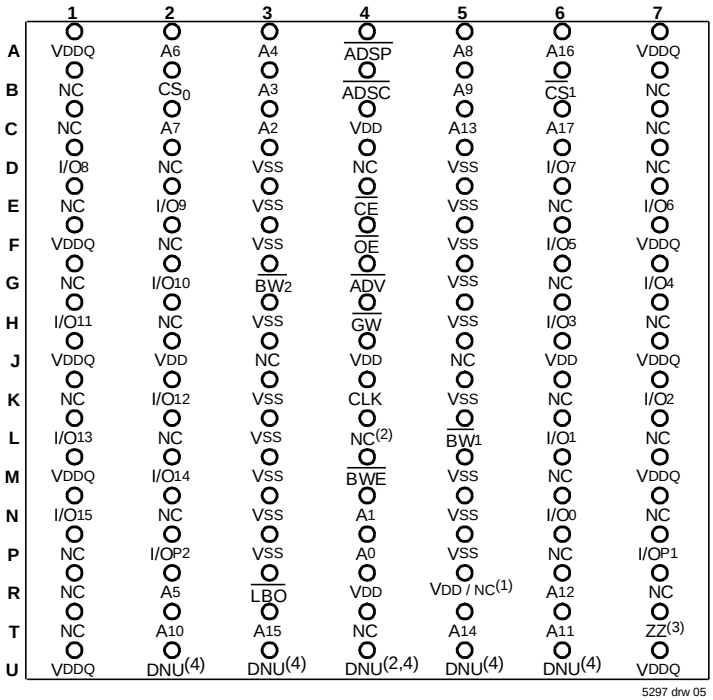
Pin Configuration – 128K x 36, 119 BGA



5297 drw 04

Top View

Pin Configuration – 256K x 18, 119 BGA



5297 drw 05

Top View

NOTES:

1. R5 can either be directly connected to V_{DD}, or connected to an input voltage ≥ V_{IH}, or left unconnected.
2. L4 and U4 can be either NC or connected to V_{SS}.
3. T7 can be left unconnected and the device will always remain in active mode.
4. DNU = Do not use; Pins U2, U3, U4, U5 and U6 are reserved for respective JTAG Pins: TMS, TDI, TCK, TDO and $\overline{TRST}$. Within the current version, these pins are left unconnected.

Pin Configuration – 128K x 36, 165 fBGA

	1	2	3	4	5	6	7	8	9	10	11
A	NC(4)	A7	$\overline{CE_1}$	$\overline{BW_3}$	$\overline{BW_2}$	$\overline{CS_1}$	$\overline{BWE}$	$\overline{ADSC}$	$\overline{ADV}$	A8	NC
B	NC	A6	CS0	$\overline{BW_4}$	$\overline{BW_1}$	CLK	$\overline{GW}$	$\overline{OE}$	$\overline{ADSP}$	A9	NC(4)
C	I/OP3	NC	VDDQ	VSS	VSS	VSS	VSS	VSS	VDDQ	NC	I/OP2
D	I/O17	I/O16	VDDQ	VDD	VSS	VSS	VSS	VDD	VDDQ	I/O15	I/O14
E	I/O19	I/O18	VDDQ	VDD	VSS	VSS	VSS	VDD	VDDQ	I/O13	I/O12
F	I/O21	I/O20	VDDQ	VDD	VSS	VSS	VSS	VDD	VDDQ	I/O11	I/O10
G	I/O23	I/O22	VDDQ	VDD	VSS	VSS	VSS	VDD	VDDQ	I/O9	I/O8
H	VDD(1)	NC(2)	NC	VDD	VSS	VSS	VSS	VDD	NC	NC	ZZ(3)
J	I/O25	I/O24	VDDQ	VDD	VSS	VSS	VSS	VDD	VDDQ	I/O7	I/O6
K	I/O27	I/O26	VDDQ	VDD	VSS	VSS	VSS	VDD	VDDQ	I/O5	I/O4
L	I/O29	I/O28	VDDQ	VDD	VSS	VSS	VSS	VDD	VDDQ	I/O3	I/O2
M	I/O31	I/O30	VDDQ	VDD	VSS	VSS	VSS	VDD	VDDQ	I/O1	I/O0
N	I/OP4	NC	VDDQ	VSS	DNU(5)	NC(4)	NC(2)	VSS	VDDQ	NC	I/OP1
P	NC	NC(4)	A5	A2	DNU(5)	A1	DNU(5)	A10	A13	A14	NC(4)
R	$\overline{LBO}$	NC(4)	A4	A3	DNU(5)	A0	DNU(5)	A11	A12	A15	A16

5297 tbl 17

Pin Configuration – 256K x 18, 165 fBGA

	1	2	3	4	5	6	7	8	9	10	11
A	NC(4)	A7	$\overline{CE_1}$	$\overline{BW_2}$	NC	$\overline{CS_1}$	$\overline{BWE}$	$\overline{ADSC}$	$\overline{ADV}$	A8	A10
B	NC	A6	CS0	NC	$\overline{BW_1}$	CLK	$\overline{GW}$	$\overline{OE}$	$\overline{ADSP}$	A9	NC(4)
C	NC	NC	VDDQ	VSS	VSS	VSS	VSS	VSS	VDDQ	NC	I/OP1
D	NC	I/O8	VDDQ	VDD	VSS	VSS	VSS	VDD	VDDQ	NC	I/O7
E	NC	I/O9	VDDQ	VDD	VSS	VSS	VSS	VDD	VDDQ	NC	I/O6
F	NC	I/O10	VDDQ	VDD	VSS	VSS	VSS	VDD	VDDQ	NC	I/O5
G	NC	I/O11	VDDQ	VDD	VSS	VSS	VSS	VDD	VDDQ	NC	I/O4
H	VDD(1)	NC(2)	NC	VDD	VSS	VSS	VSS	VDD	NC	NC	ZZ(3)
J	I/O12	NC	VDDQ	VDD	VSS	VSS	VSS	VDD	VDDQ	I/O3	NC
K	I/O13	NC	VDDQ	VDD	VSS	VSS	VSS	VDD	VDDQ	I/O2	NC
L	I/O14	NC	VDDQ	VDD	VSS	VSS	VSS	VDD	VDDQ	I/O1	NC
M	I/O15	NC	VDDQ	VDD	VSS	VSS	VSS	VDD	VDDQ	I/O0	NC
N	I/OP2	NC	VDDQ	VSS	DNU(5)	NC(4)	NC(2)	VSS	VDDQ	NC	NC
P	NC	NC(4)	A5	A2	DNU(5)	A1	DNU(5)	A11	A14	A15	NC(4)
R	$\overline{LBO}$	NC(4)	A4	A3	DNU(5)	A0	DNU(5)	A12	A13	A16	A17

5297 tbl 17a

NOTES:
1. H1 can either be directly connected to VDD, or connected to an input voltage ≥ VIH, or left unconnected.
2. H2 and N7 can be either NC or connected to VSS.
3. H11 can be left unconnected and the device will always remain in active mode.
4. Pins P11, N6, B11, A1, R2 and P2 are reserved for 9M, 18M, 36M, 72M, 144M and 288M respectively.
5. DNU = Do not use; Pins P5, P7, R5, R7 and N5 are reserved for respective JTAG Pins: TDI, TDO, TMS, TCK and $\overline{TRST}$ on future revisions. Within this current version, these pins are not connected.

DC Electrical Characteristics Over the Operating Temperature and Supply Voltage Range (V_{DD} = 3.3V ± 5%)

Symbol	Parameter	Test Conditions	Min.	Max.	Unit
$\|I_{LI}\|$	Input Leakage Current	V_{DD} = Max., V_{IN} = 0V to V_{DD}	—	5	µA
$\|I_{LZZ}\|$	ZZ and $\overline{LBO}$ Input Leakage Current[1]	V_{DD} = Max., V_{IN} = 0V to V_{DD}	—	30	µA
$\|I_{LO}\|$	Output Leakage Current	V_{OUT} = 0V to V_{DDQ}, Device Deselected	—	5	µA
V_{OL}	Output Low Voltage	I_{OL} = +6mA, V_{DD} = Min.	—	0.4	V
V_{OH}	Output High Voltage	I_{OH} = -6mA, V_{DD} = Min.	2.0	—	V

5297 tbl 08

NOTE:
1. The $\overline{LBO}$ pin will be internally pulled to V_{DD} if it is not actively driven in the application and the ZZ pin will be internally pulled to V_{SS} if not actively driven.

DC Electrical Characteristics Over the Operating Temperature and Supply Voltage Range[1]

Symbol	Parameter	Test Conditions	200MHz	183MHz		166MHz		Unit
			Com'l Only	Com'l	Ind	Com'l	Ind	
I_{DD}	Operating Power Supply Current	Device Selected, Outputs Open, V_{DD} = Max., V_{DDQ} = Max., $V_{IN} \geq V_{IH}$ or $\leq V_{IL}$, f = f_{MAX}[2]	360	340	350	320	330	mA
I_{SB1}	CMOS Standby Power Supply Current	Device Deselected, Outputs Open, V_{DD} = Max., V_{DDQ} = Max., $V_{IN} \geq V_{HD}$ or $\leq V_{LD}$, f = 0[2,3]	30	30	35	30	35	mA
I_{SB2}	Clock Running Power Supply Current	Device Deselected, Outputs Open, V_{DD} = Max., V_{DDQ} = Max., $V_{IN} \geq V_{HD}$ or $\leq V_{LD}$, f = f_{MAX}[2,3]	130	120	130	110	120	mA
I_{ZZ}	Full Sleep Mode Supply Current	ZZ $\geq V_{HD}$, V_{DD} = Max.	30	30	35	30	35	mA

5297 tbl 09

NOTES:
1. All values are maximum guaranteed values.
2. At f = f_{MAX}, inputs are cycling at the maximum frequency of read cycles of 1/t_{CYC} while $\overline{ADSC}$ = LOW; f=0 means no input lines are changing.
3. For I/Os V_{HD} = V_{DDQ} - 0.2V, V_{LD} = 0.2V. For other inputs V_{HD} = V_{DD} - 0.2V, V_{LD} = 0.2V.

AC Test Conditions (V_{DDQ} = 2.5V)

Input Pulse Levels	0 to 2.5V
Input Rise/Fall Times	2ns
Input Timing Reference Levels	(V_{DDQ}/2)
Output Timing Reference Levels	(V_{DDQ}/2)
AC Test Load	See Figure 1

5297 tbl 10

AC Test Load

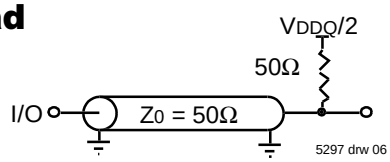


Figure 1. AC Test Load

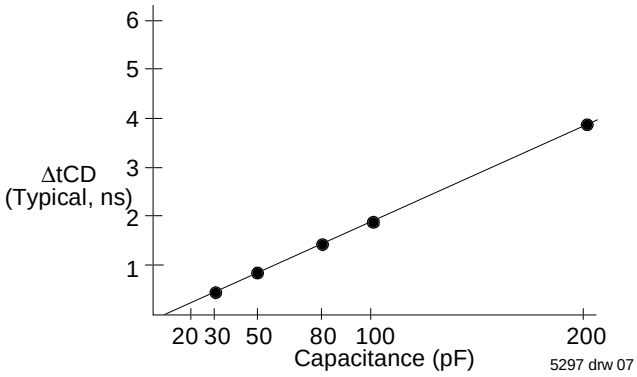


Figure 2. Lumped Capacitive Load, Typical Derating

Synchronous Truth Table(1,3)

Operation	Address Used	$\overline{CE}$	CS_0	$\overline{CS_1}$	$\overline{ADSP}$	$\overline{ADSC}$	$\overline{ADV}$	$\overline{GW}$	$\overline{BWE}$	$\overline{BW}x$	$\overline{OE}$ (2)	CLK	I/O
Deselected Cycle, Power Down	None	H	X	X	X	L	X	X	X	X	X	-	HI-Z
Deselected Cycle, Power Down	None	L	X	H	L	X	X	X	X	X	X	-	HI-Z
Deselected Cycle, Power Down	None	L	L	X	L	X	X	X	X	X	X	-	HI-Z
Deselected Cycle, Power Down	None	L	X	H	X	L	X	X	X	X	X	-	HI-Z
Deselected Cycle, Power Down	None	L	L	X	X	L	X	X	X	X	X	-	HI-Z
Read Cycle, Begin Burst	External	L	H	L	L	X	X	X	X	X	L	-	DOUT
Read Cycle, Begin Burst	External	L	H	L	L	X	X	X	X	X	H	-	HI-Z
Read Cycle, Begin Burst	External	L	H	L	H	L	X	H	H	X	L	-	DOUT
Read Cycle, Begin Burst	External	L	H	L	H	L	X	H	L	H	L	-	DOUT
Read Cycle, Begin Burst	External	L	H	L	H	L	X	H	L	H	H	-	HI-Z
Write Cycle, Begin Burst	External	L	H	L	H	L	X	H	L	L	X	-	DIN
Write Cycle, Begin Burst	External	L	H	L	H	L	X	L	X	X	X	-	DIN
Read Cycle, Continue Burst	Next	X	X	X	H	H	L	H	H	X	L	-	DOUT
Read Cycle, Continue Burst	Next	X	X	X	H	H	L	H	H	X	H	-	HI-Z
Read Cycle, Continue Burst	Next	X	X	X	H	H	L	H	X	H	L	-	DOUT
Read Cycle, Continue Burst	Next	X	X	X	H	H	L	H	X	H	H	-	HI-Z
Read Cycle, Continue Burst	Next	H	X	X	X	H	L	H	H	X	L	-	DOUT
Read Cycle, Continue Burst	Next	H	X	X	X	H	L	H	H	X	H	-	HI-Z
Read Cycle, Continue Burst	Next	H	X	X	X	H	L	H	X	H	L	-	DOUT
Read Cycle, Continue Burst	Next	H	X	X	X	H	L	H	X	H	H	-	HI-Z
Write Cycle, Continue Burst	Next	X	X	X	H	H	L	H	L	L	X	-	DIN
Write Cycle, Continue Burst	Next	X	X	X	H	H	L	L	X	X	X	-	DIN
Write Cycle, Continue Burst	Next	H	X	X	X	H	L	H	L	L	X	-	DIN
Write Cycle, Continue Burst	Next	H	X	X	X	H	L	L	X	X	X	-	DIN
Read Cycle, Suspend Burst	Current	X	X	X	H	H	H	H	H	X	L	-	DOUT
Read Cycle, Suspend Burst	Current	X	X	X	H	H	H	H	H	X	H	-	HI-Z
Read Cycle, Suspend Burst	Current	X	X	X	H	H	H	H	X	H	L	-	DOUT
Read Cycle, Suspend Burst	Current	X	X	X	H	H	H	H	X	H	H	-	HI-Z
Read Cycle, Suspend Burst	Current	H	X	X	X	H	H	H	H	X	L	-	DOUT
Read Cycle, Suspend Burst	Current	H	X	X	X	H	H	H	H	X	H	-	HI-Z
Read Cycle, Suspend Burst	Current	H	X	X	X	H	H	H	X	H	L	-	DOUT
Read Cycle, Suspend Burst	Current	H	X	X	X	H	H	H	X	H	H	-	HI-Z
Write Cycle, Suspend Burst	Current	X	X	X	H	H	H	H	L	L	X	-	DIN
Write Cycle, Suspend Burst	Current	X	X	X	H	H	H	L	X	X	X	-	DIN
Write Cycle, Suspend Burst	Current	H	X	X	X	H	H	H	L	L	X	-	DIN
Write Cycle, Suspend Burst	Current	H	X	X	X	H	H	L	X	X	X	-	DIN

5297 tbl 11

NOTES:
1. L = V_{IL}, H = V_{IH}, X = Don't Care.
2. $\overline{OE}$ is an asynchronous input.
3. ZZ = low for this table.

Synchronous Write Function Truth Table(1, 2)

Operation	$\overline{GW}$	$\overline{BWE}$	$\overline{BW_1}$	$\overline{BW_2}$	$\overline{BW_3}$	$\overline{BW_4}$
Read	H	H	X	X	X	X
Read	H	L	H	H	H	H
Write all Bytes	L	X	X	X	X	X
Write all Bytes	H	L	L	L	L	L
Write Byte 1(3)	H	L	L	H	H	H
Write Byte 2(3)	H	L	H	L	H	H
Write Byte 3(3)	H	L	H	H	L	H
Write Byte 4(3)	H	L	H	H	H	L

5297 tbl 12

NOTES:
1. L = V_{IL}, H = V_{IH}, X = Don't Care.
2. $\overline{BW_3}$ and $\overline{BW_4}$ are not applicable for the IDT71V2578.
3. Multiple bytes may be selected during the same cycle.

Asynchronous Truth Table(1)

Operation(2)	$\overline{OE}$	ZZ	I/O Status	Power
Read	L	L	Data Out	Active
Read	H	L	High-Z	Active
Write	X	L	High-Z – Data In	Active
Deselected	X	L	High-Z	Standby
Sleep Mode	X	H	High-Z	Sleep

5297 tbl 13

NOTES:
1. L = V_{IL}, H = V_{IH}, X = Don't Care.
2. Synchronous function pins must be biased appropriately to satisfy operation requirements.

Interleaved Burst Sequence Table ($\overline{LBO}$=V_{DD})

	Sequence 1		Sequence 2		Sequence 3		Sequence 4	
	A1	A0	A1	A0	A1	A0	A1	A0
First Address	0	0	0	1	1	0	1	1
Second Address	0	1	0	0	1	1	1	0
Third Address	1	0	1	1	0	0	0	1
Fourth Address(1)	1	1	1	0	0	1	0	0

5297 tbl 14

NOTE:
1. Upon completion of the Burst sequence the counter wraps around to its initial state.

Linear Burst Sequence Table ($\overline{LBO}$=Vss)

	Sequence 1		Sequence 2		Sequence 3		Sequence 4	
	A1	A0	A1	A0	A1	A0	A1	A0
First Address	0	0	0	1	1	0	1	1
Second Address	0	1	1	0	1	1	0	0
Third Address	1	0	1	1	0	0	0	1
Fourth Address(1)	1	1	0	0	0	1	1	0

5297 tbl 15

NOTE:
1. Upon completion of the Burst sequence the counter wraps around to its initial state.

AC Electrical Characteristics

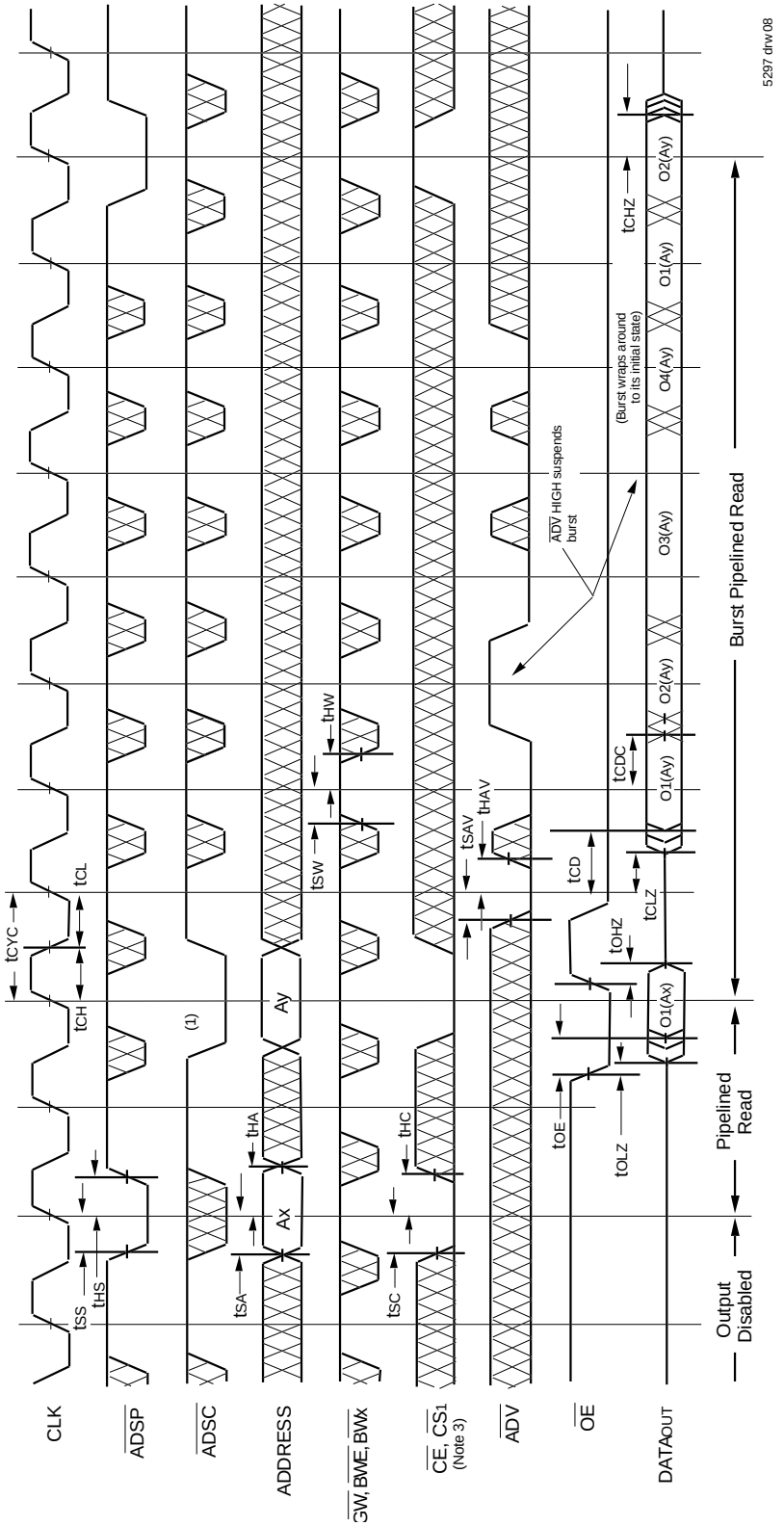
(V_{DD} = 3.3V ±5%, Commercial and Industrial Temperature Ranges)

Symbol	Parameter	200MHz[5]		183MHz		166MHz		Unit
		Min.	Max.	Min.	Max.	Min.	Max.	
t_{CYC}	Clock Cycle Time	5	—	5.5	—	6	—	ns
t_{CH}[1]	Clock High Pulse Width	2	—	2.2	—	2.4	—	ns
t_{CL}[1]	Clock Low Pulse Width	2	—	2.2	—	2.4	—	ns
Output Parameters								
t_{CD}	Clock High to Valid Data	—	3.1	—	3.3	—	3.5	ns
t_{CDC}	Clock High to Data Change	1.0	—	1.0	—	1.0	—	ns
t_{CLZ}[2]	Clock High to Output Active	0	—	0	—	0	—	ns
t_{CHZ}[2]	Clock High to Data High-Z	1.5	3.1	1.5	3.3	1.5	3.5	ns
t_{OE}	Output Enable Access Time	—	3.1	—	3.3	—	3.5	ns
t_{OLZ}[2]	Output Enable Low to Output Active	0	—	0	—	0	—	ns
t_{OHZ}[2]	Output Enable High to Output High-Z	—	3.1	—	3.3	—	3.5	ns
Set Up Times								
t_{SA}	Address Setup Time	1.2	—	1.5	—	1.5	—	ns
t_{SS}	Address Status Setup Time	1.2	—	1.5	—	1.5	—	ns
t_{SD}	Data In Setup Time	1.2	—	1.5	—	1.5	—	ns
t_{SW}	Write Setup Time	1.2	—	1.5	—	1.5	—	ns
t_{SAV}	Address Advance Setup Time	1.2	—	1.5	—	1.5	—	ns
t_{SC}	Chip Enable/Select Setup Time	1.2	—	1.5	—	1.5	—	ns
Hold Times								
t_{HA}	Address Hold Time	0.4	—	0.5	—	0.5	—	ns
t_{HS}	Address Status Hold Time	0.4	—	0.5	—	0.5	—	ns
t_{HD}	Data In Hold Time	0.4	—	0.5	—	0.5	—	ns
t_{HW}	Write Hold Time	0.4	—	0.5	—	0.5	—	ns
t_{HAV}	Address Advance Hold Time	0.4	—	0.5	—	0.5	—	ns
t_{HC}	Chip Enable/Select Hold Time	0.4	—	0.5	—	0.5	—	ns
Sleep Mode and Configuration Parameters								
t_{ZZPW}	ZZ Pulse Width	100	—	100	—	100	—	ns
t_{ZZR}[3]	ZZ Recovery Time	100	—	100	—	100	—	ns
t_{CFG}[4]	Configuration Set-up Time	20	—	22	—	24	—	ns

4876 tbl 16

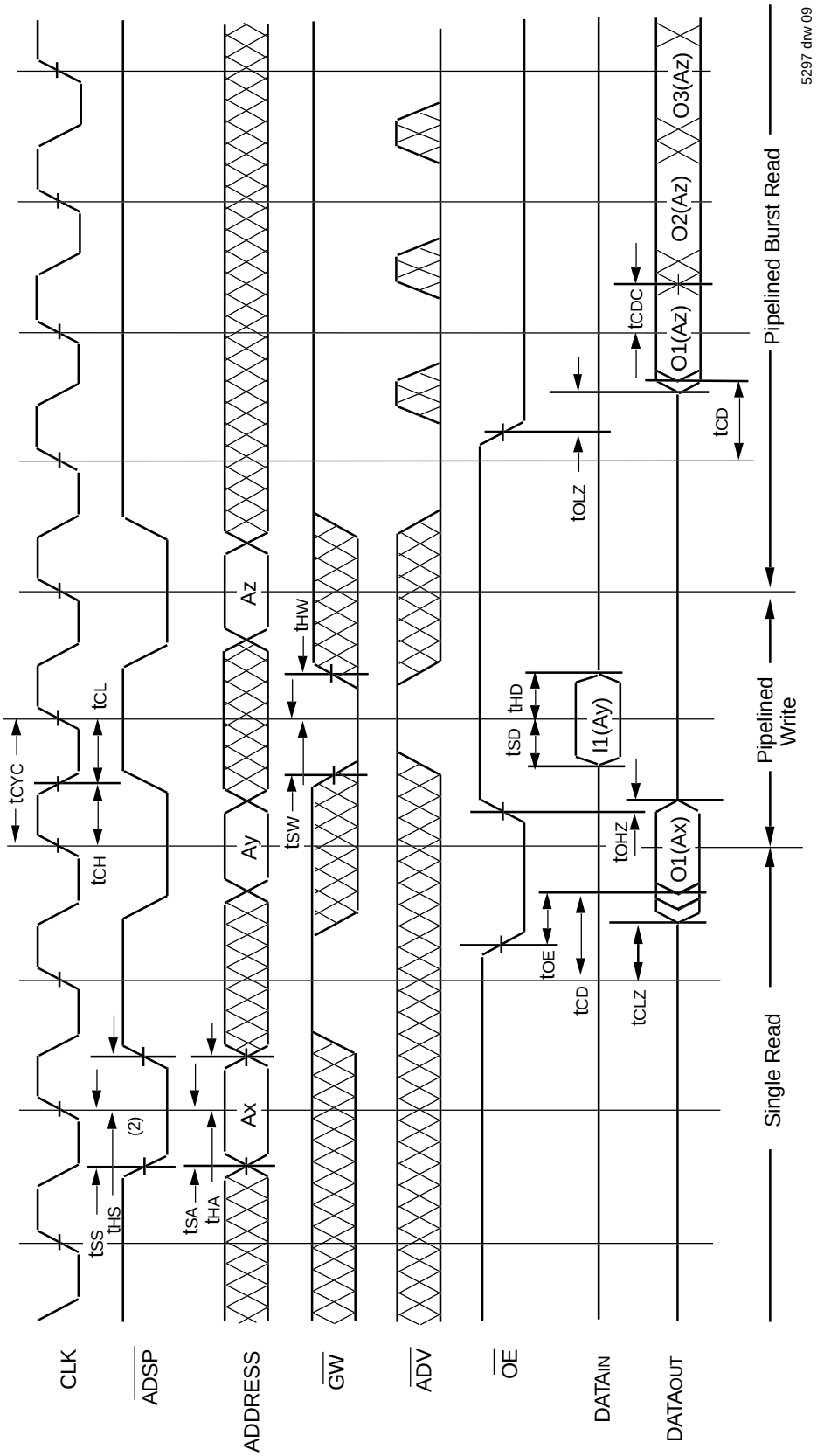
NOTES:
1. Measured as HIGH above V_{IH} and LOW below V_{IL}.
2. Transition is measured ±200mV from steady-state.
3. Device must be deselected when powered-up from sleep mode.
4. t_{CFG} is the minimum time required to configure the device based on the $\overline{LBO}$ input. $\overline{LBO}$ is a static input and must not change during normal operation.
5. Commercial temperature range only.

Timing Waveform of Pipeline Read Cycle(1,2)



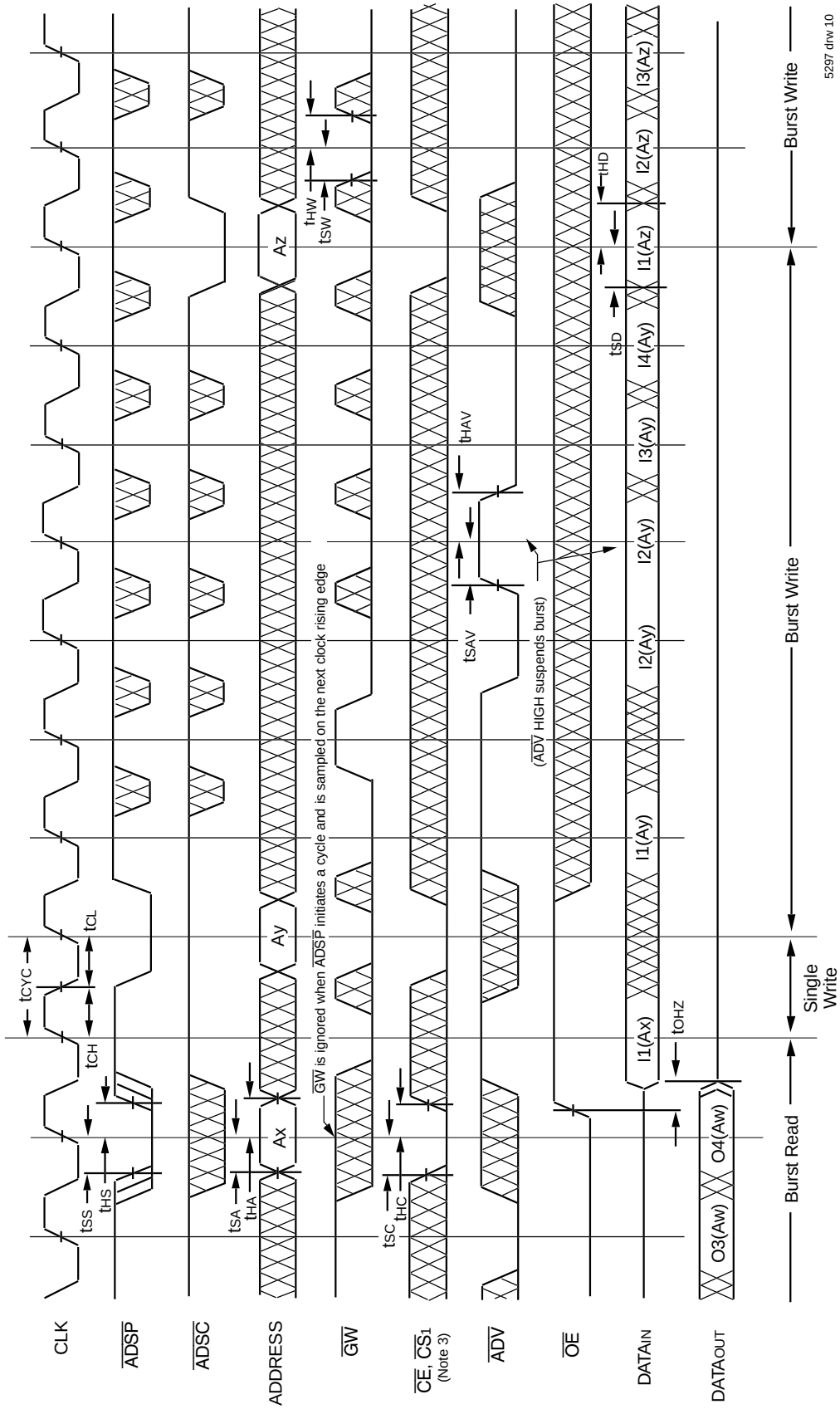
NOTES:
1. O1 (Ax) represents the first output from the external address Ax. O1 (Ay) represents the first output from the external address Ay; O2 (Ay) represents the next output data in the burst sequence of the base address Ay, etc. where A0 and A1 are advancing for the four word burst in the sequence defined by the state of the LBO input.
2. ZZ input is LOW and LBO is Don't Care for this cycle.
3. CS0 timing transitions are identical but inverted to the CE and CS1 signals. For example, when CE and CS1 are LOW on this waveform, CS0 is HIGH.

Timing Waveform of Combined Pipelined Read and Write Cycles(1,2,3)



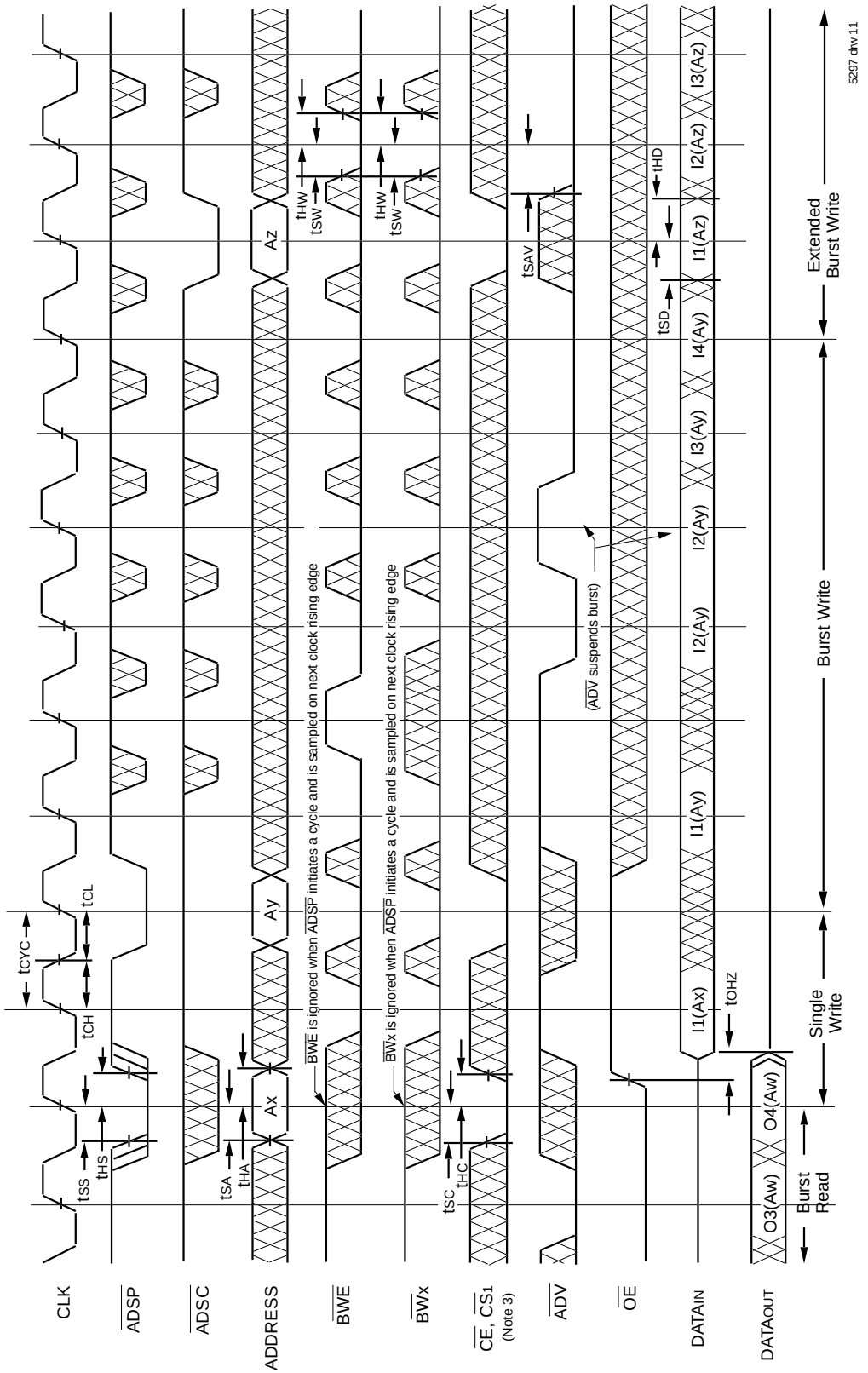
NOTES:
1. Device is selected through entire cycle; $\overline{CE}$ and $\overline{CS}1$ are LOW, CS0 is HIGH.
2. ZZ input is LOW and $\overline{LBO}$ is Don't Care for this cycle.
3. O1 (Ax) represents the first output from the external address Ax. I1 (Ay) represents the first input from the external address Ay; O1 (Az) represents the first output from the external address Az; O2 (Az) represents the next output data in the burst sequence of the base address Az, etc. where A0 and A1 are advancing for the four word burst in the sequence defined by the state of the $\overline{LBO}$ input.

Timing Waveform of Write Cycle No. 1 — $\overline{GW}$ Controlled(1,2,3)



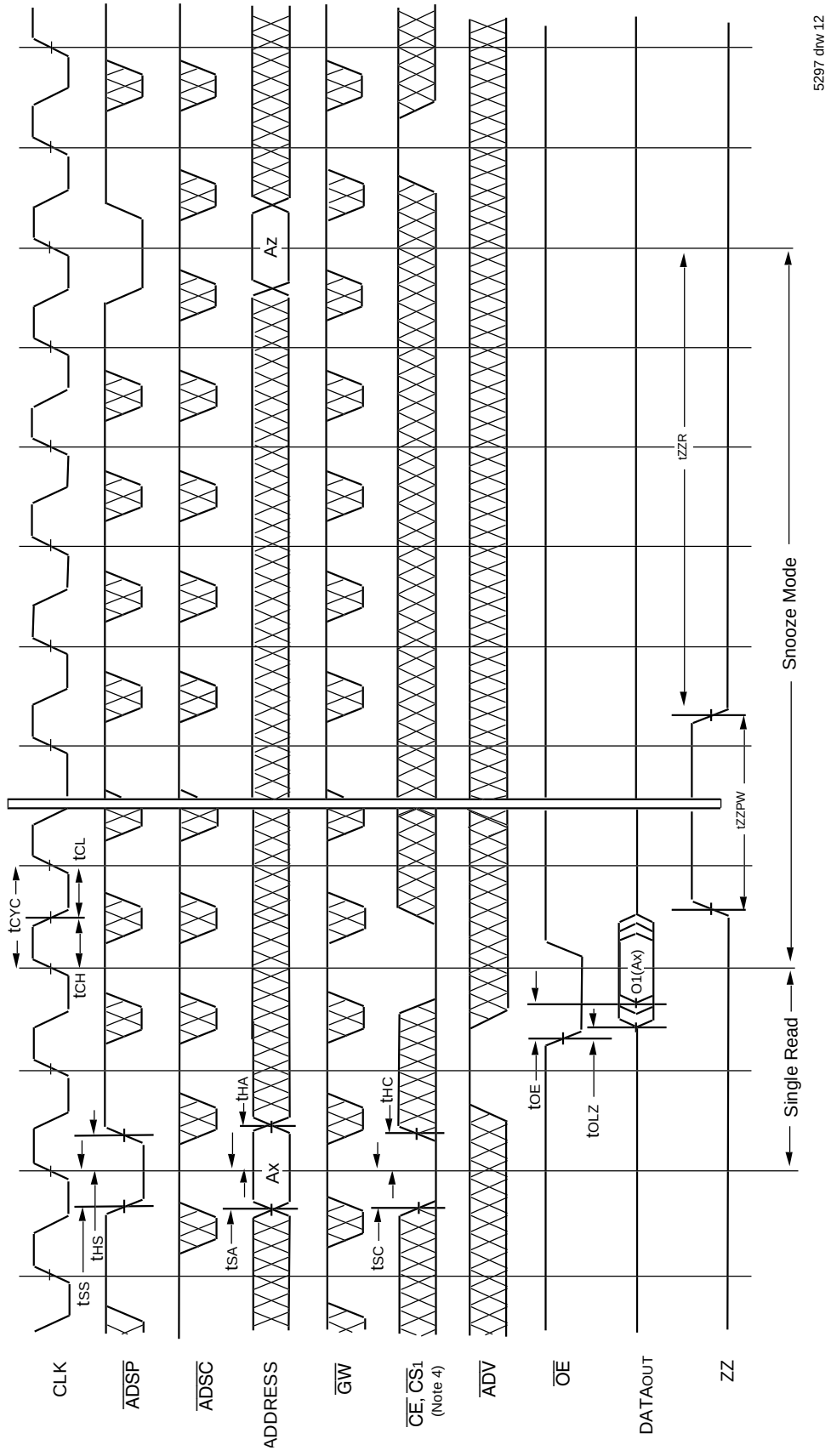
NOTES:
1. ZZ input is LOW, $\overline{BWE}$ is HIGH and $\overline{LBO}$ is Don't Care for this cycle.
2. O4 (Aw) represents the final output data in the burst sequence of the base address Aw. I1 (Ax) represents the first input from the external address Ax. I1 (Ay) represents the first input from the external address Ay; I2 (Ay) represents the next input data in the burst sequence of the base address Ay, etc. where A0 and A1 are advancing for the four word burst in the sequence defined by the state of the $\overline{LBO}$ input. In the case of input I2 (Ay) this data is valid for two cycles because $\overline{ADV}$ is high and has suspended the burst.
3. CS0 timing transitions are identical but inverted to the $\overline{CE}$ and $\overline{CS}_1$ signals. For example, when $\overline{CE}$ and $\overline{CS}_1$ are LOW on this waveform, CS0 is HIGH.

Timing Waveform of Write Cycle No. 2 — Byte Controlled(1,2,3)



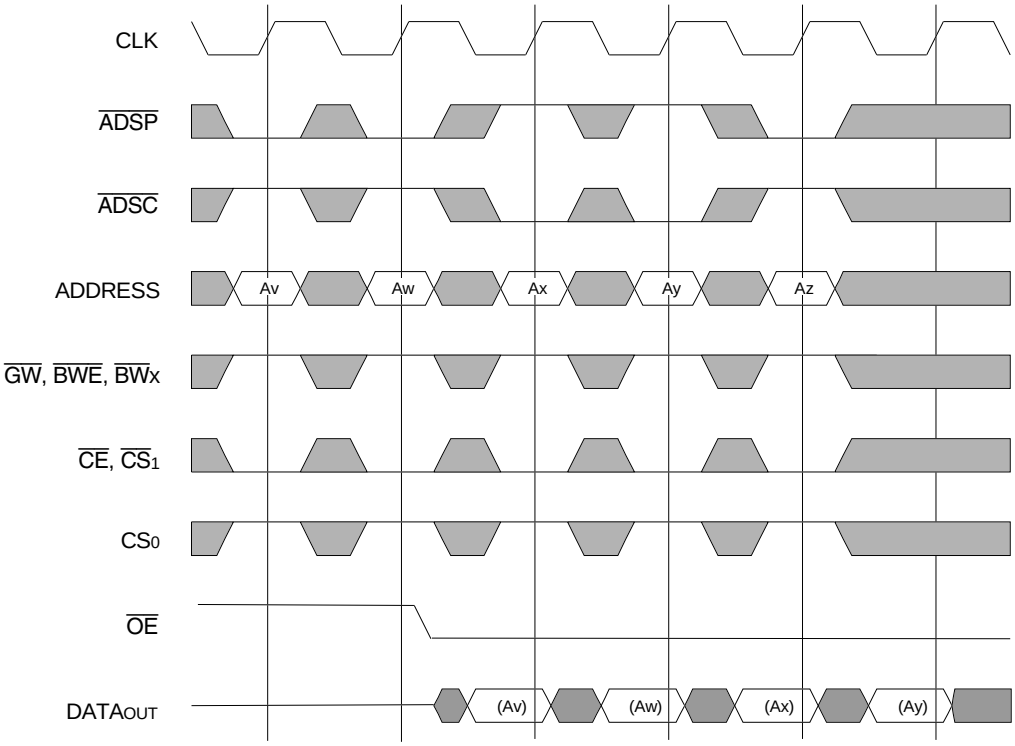
NOTES:
1. ZZ input is LOW, $\overline{GW}$ is HIGH and $\overline{LBO}$ is Don't Care for this cycle.
2. O4 (Aw) represents the final output data in the burst sequence of the base address Aw. I1 (Ax) represents the first input from the external address Ax. I1 (Ay) represents the first input from the external address Ay; I2 (Ay) represent the next input data in the burst sequence of the base address Ay, etc. where A0 and A1 are advancing for the four word burst in the sequence defined by the state of the $\overline{LBO}$ input. In the case of input I2 (Ay) this data is valid for two cycles because $\overline{ADV}$ is high and has suspended the burst.
3. CS0 timing transitions are identical but inverted to the $\overline{CE}$ and $\overline{CS1}$ signals. For example, when $\overline{CE}$ and $\overline{CS1}$ are LOW on this waveform, CS0 is HIGH.

Timing Waveform of Sleep (ZZ) and Power-Down Modes(1,2,3)



NOTES:
1. Device must power up in deselected Mode.
2. $\overline{LBO}$ is Don't Care for this cycle.
3. It is not necessary to retain the state of the input registers throughout the Power-down cycle.
4. CS_0 timing transitions are identical but inverted to the $\overline{CE}$ and $\overline{CS}_1$ signals. For example, when $\overline{CE}$ and CS_1 are LOW on this waveform, CS_0 is HIGH.

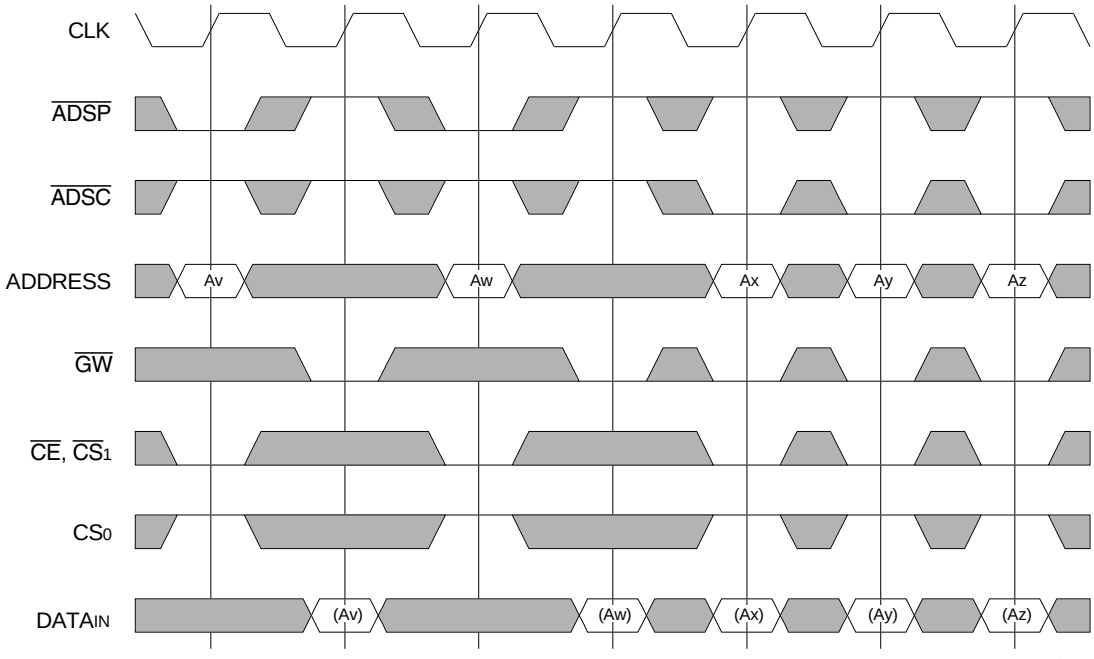
Non-Burst Read Cycle Timing Waveform



5297 drw 14

NOTES:
1. ZZ input is LOW, ADV is HIGH and LBO is Don't Care for this cycle.
2. (Ax) represents the data for address Ax, etc.
3. For read cycles, ADSP and ADSC function identically and are therefore interchangable.

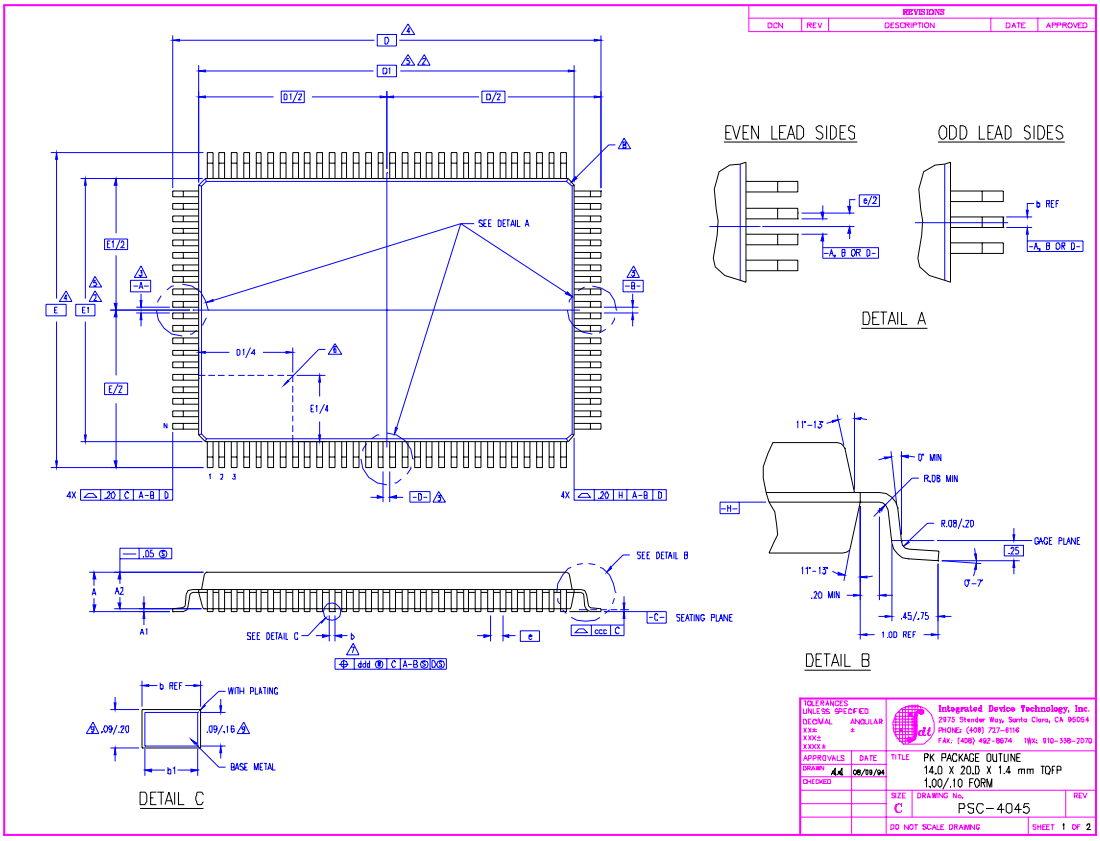
Non-Burst Write Cycle Timing Waveform



5297 drw 15

NOTES:
1. ZZ input is LOW, ADV and OE are HIGH, and LBO is Don't Care for this cycle.
2. (Ax) represents the data for address Ax, etc.
3. Although only GW writes are shown, the functionality of BWE and BWx together is the same as GW.
4. For write cycles, ADSP and ADSC have different limitations.

100-Pin Plastic Thin Quad Flatpack(TQFP) Package Diagram Outline

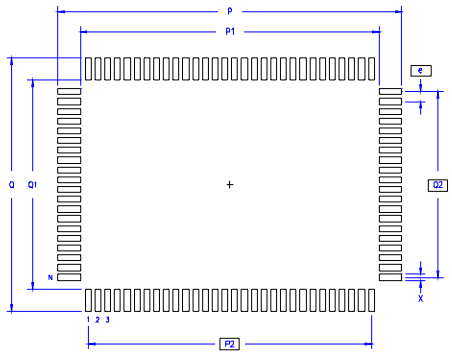


SYMBOL	JEDEC VARIATION DJ MIN	NOM	MAX	NOTE
A	–	–	1.60	
A1	.05	.10	.15	
A2	1.35	1.40	1.45	
D		22.00 BSC		4
D1		20.00 BSC		5,2
E		16.00 BSC		4
E1		14.00 BSC		5,2
N		100		
ND		30		
NE		20		
e		.65 BSC		
b	.22	.32	.38	7
b1	.22	.30	.33	
ccc	–	–	.10	
ddd	–	–	.13	

NOTES:

1. ALL DIMENSIONING AND TOLERANCING CONFORM TO ANSI Y14.5M-1982
2. TOP PACKAGE MAY BE SMALLER THAN BOTTOM PACKAGE BY .15 mm
3. DATUMS [A-B] AND [-D-] TO BE DETERMINED AT DATUM PLANE [-H-]
4. DIMENSIONS D AND E ARE TO BE DETERMINED AT SEATING PLANE [-C-]
5. DIMENSIONS D1 AND E1 DO NOT INCLUDE MOLD PROTRUSION. ALLOWABLE MOLD PROTRUSION IS .25 mm PER SIDE. D1 AND E1 ARE MAXIMUM BODY SIZE DIMENSIONS INCLUDING MOLD MISMATCH
6. DETAILS OF PIN 1 IDENTIFIER IS OPTIONAL BUT MUST BE LOCATED WITHIN THE ZONE INDICATED
7. DIMENSION b DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION IS .08 mm IN EXCESS OF THE b DIMENSION AT MAXIMUM MATERIAL CONDITION. DAMBAR CANNOT BE LOCATED ON THE LOWER RADIUS OR THE FOOT.
8. EXACT SHAPE OF EACH CORNER IS OPTIONAL
9. THESE DIMENSIONS APPLY TO THE FLAT SECTION OF THE LEAD BETWEEN .10 AND .25 mm FROM THE LEAD TIP
10. ALL DIMENSIONS ARE IN MILLIMETERS
11. THIS OUTLINE CONFORMS TO JEDEC PUBLICATION 95 REGISTRATION MO-136, VARIATION DJ AND BX

LAND PATTERN DIMENSIONS

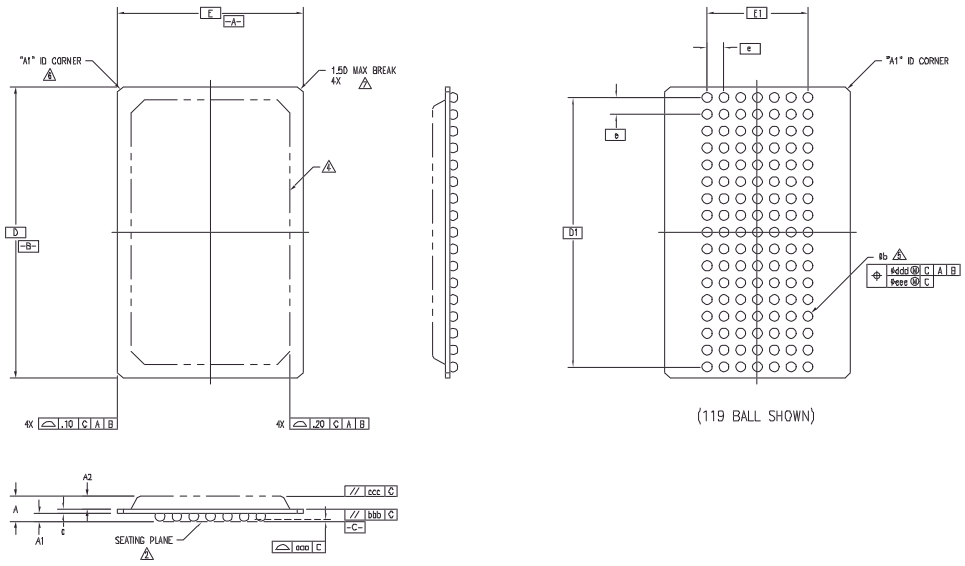


	MIN	MAX
P	22.80	23.00
P1	19.80	20.00
P2	18.85 BSC	
Q	16.80	17.00
Q1	13.80	14.00
Q2	12.35 BSC	
X	.30	.50
e	.65 BSC	
N	100	

Integrated Device Technology, Inc.
2975 Stender Way, Santa Clara, CA 95054
PHONE: (408) 727-6116
FAX: (408) 492-8674
TITLE PK PACKAGE OUTLINE
14.0 X 20.0 X 1.4 mm TQFP
1.00/.10 FORM
SIZE C
DRAWING No. PSC-4045
REV
DO NOT SCALE DRAWING
SHEET 2 OF 2

119 Ball Grid Array (BGA) Package Diagram Outline

REVISIONS				
DCN	REV	DESCRIPTION	DATE	APPROVED
60626	00	INITIAL RELEASE	10/15/97	T. VU
	01	SWITCH E & D DIMENSIONS	04/25/00	T. VU
	02	CHANGE PACKAGE THICKNESS	08/05/00	



(119 BALL SHOWN)

TOLERANCES UNLESS SPECIFIED
DECIMAL ANGULAR
XX± ±
XXX±
XXXX±

Integrated Device Technology, Inc.
2975 Stender Way, Santa Clara, CA 95054
PHONE: (408) 727-6116
FAX: (408) 492-8674 TWX: 910-338-2070

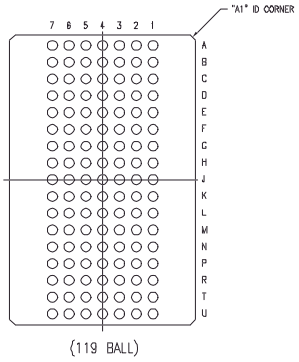
APPROVALS	DATE
DRAWN JV	10/15/97
CHECKED	

TITLE BG PACKAGE OUTLINE
14.0 X 22.0 mm BODY
PBGA

SIZE C | DRAWING No. PSC-4063 | REV 02

DO NOT SCALE DRAWING | SHEET 1 OF 2

REVISIONS				
DCN	REV	DESCRIPTION	DATE	APPROVED
60626	00	INITIAL RELEASE	10/15/97	T. VU
	01	SWITCH E & D DIMENSIONS	04/25/00	T. VU
	02	CHANGE PACKAGE THICKNESS	08/05/00	



(119 BALL)

SYMBOL	JEDEC VARIATION AA MIN	NOM	MAX	NOTE
A	–	2.15	2.36	
A1	.50	.60	.70	
A2	–	–	1.20	
D	22.00 BSC			
D1	20.32 BSC			
E	14.00 BSC			
E1	7.62 BSC			
MD	17			3
ME	7			3
N	119			3
e	1.27 BSC			
b	.60	.75	.90	5
c	.51	.56	.61	
aaa	–	–	.15	
bbb	–	–	.25	
ccc	–	–	.35	
ddd	–	–	.30	
eee	–	–	.10	

NOTES:

1 ALL DIMENSIONING AND TOLERANCING CONFORM TO ANSI Y14.5M-1982

2 SEATING PLANE AND PRIMARY DATUM -C- ARE DEFINED BY THE SPHERICAL CROWNS OF THE SOLDER BALLS

3 "MD" IS THE BALL MATRIX SIZE IN THE "D" DIRECTION
"ME" IS THE BALL MATRIX SIZE IN THE "E" DIRECTION
"N" IS THE MAXIMUM ALLOWABLE NUMBER OF SOLDER BALLS

4 PACKAGE MAY EXTEND TO EDGE PERIPHERY AND MAY CONSIST OF MOLDING COMPOUND, EPOXY, METAL, CERAMIC OR OTHER MATERIAL

5 DIMENSION "b" IS MEASURED AT THE MAXIMUM SOLDER BALL DIAMETER, PARALLEL TO PRIMARY DATUM -C-

6 "A1" ID CORNER MUST BE IDENTIFIED. IDENTIFICATION MAY BE BY MEANS OF CHAMFER, METALLIZED OR INK MARK, INDENTATION OR OTHER FEATURE OF THE PACKAGE BODY. MARK MUST BE VISIBLE FROM TOP SURFACE

7 ACTUAL SHAPE OF THIS FEATURE IS OPTIONAL

8 ALL DIMENSIONS ARE IN MILLIMETERS

9 THIS DRAWING CONFORMS TO JEDEC PUBLICATION 95 REGISTRATION MS-028, VARIATION AA

TOLERANCES UNLESS SPECIFIED
DECIMAL ANGULAR
XX± ±
XXX±
XXXX±

Integrated Device Technology, Inc.
2975 Stender Way, Santa Clara, CA 95054
PHONE: (408) 727-6116
FAX: (408) 492-8674 TWX: 910-338-2070

APPROVALS	DATE
DRAWN JV	10/15/97
CHECKED	

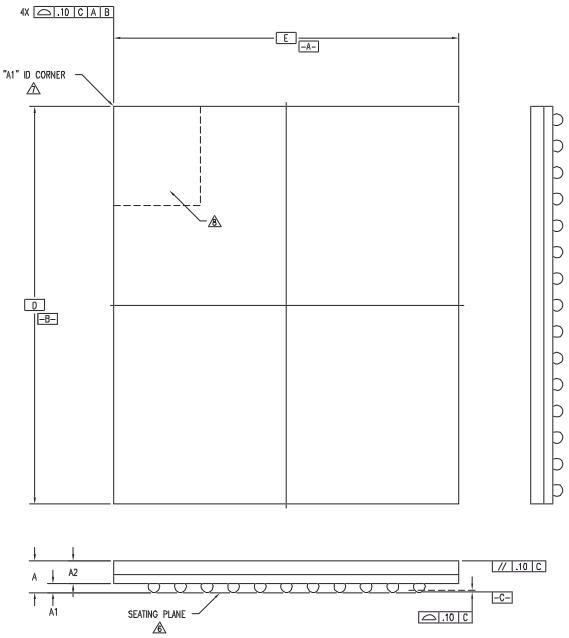
TITLE BG PACKAGE OUTLINE
14.0 X 22.0 mm BODY
PBGA

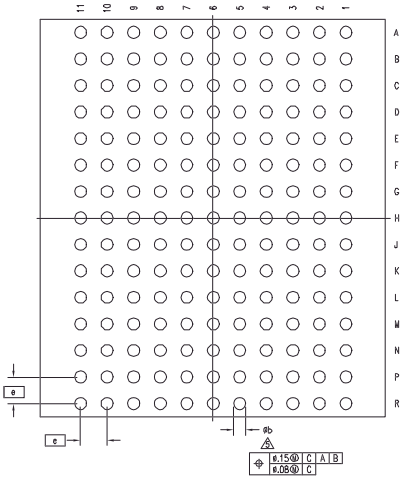
SIZE C | DRAWING No. PSC-4063 | REV 02

DO NOT SCALE DRAWING | SHEET 2 OF 2

165 Fine Pitch Ball Grid Array (fBGA) Package Diagram Outline

REVISIONS				
DCN	REV	DESCRIPTION	DATE	APPROVED
	00	INITIAL RELEASE	05/01/00	

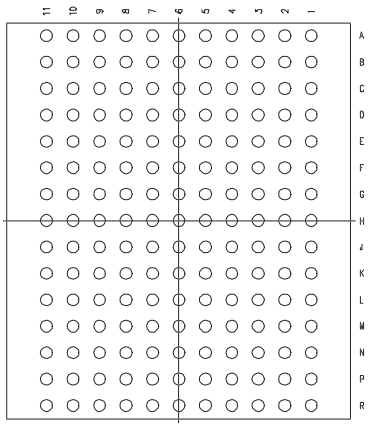




(165 BALL SHOWN)

TOLERANCES UNLESS SPECIFIED		Integrated Device Technology, Inc. 2975 Stender Way, Santa Clara, CA 95054 PHONE: (408) 727-6116 FAX: (408) 492-8674 TWX: 910-338-2070	
DECIMAL ANGULAR			
XX± ±			
XXX±			
XXXX±			
APPROVALS	DATE	TITLE BQ PACKAGE OUTLINE 13.0 X 15.0 mm BODY FPBGA	
DRAWN JTP	05/01/00		
CHECKED		SIZE C	DRAWING No. PSC-4086 REV 00
		DO NOT SCALE DRAWING	SHEET 1 OF 2

REVISIONS				
DCN	REV	DESCRIPTION	DATE	APPROVED
	00	INITIAL RELEASE	05/01/00	



(165 BALL)

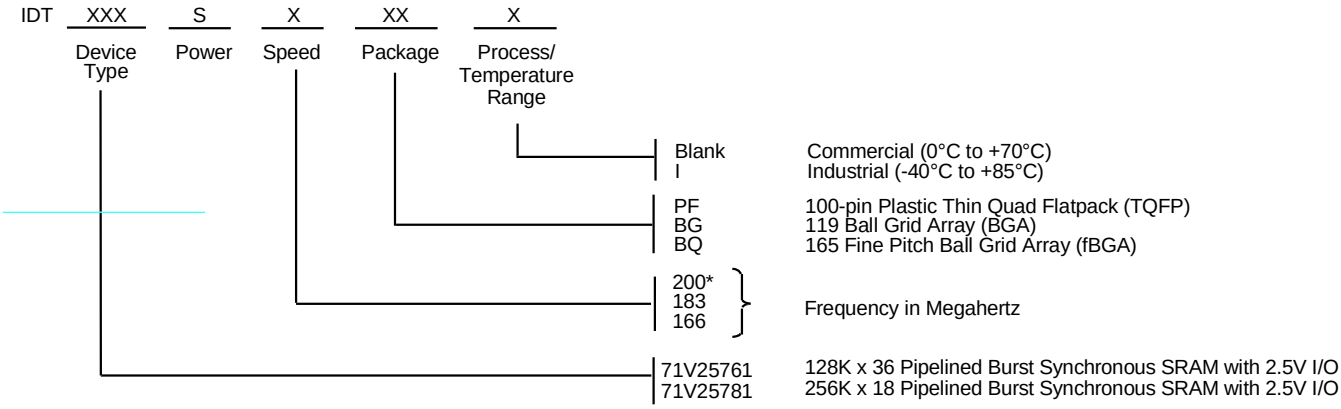
NOTES:

1. ALL DIMENSIONING AND TOLERANCING CONFORM TO ASME Y14.5M-1994
2. "e" REPRESENTS THE BASIC SOLDER BALL GRID PITCH
3. "M" REPRESENTS THE MAXIMUM SOLDER BALL MATRIX SIZE
4. "N" REPRESENTS THE BALLCOUNT NUMBER
5. DIMENSION "b" IS MEASURED AT THE MAXIMUM SOLDER BALL DIAMETER, PARALLEL TO PRIMARY DATUM -C-
6. SEATING PLANE AND PRIMARY DATUM -C- ARE DEFINED BY THE SPHERICAL CROWNS OF THE SOLDER BALLS
7. "A1" ID CORNER MUST BE IDENTIFIED BY CHAMFER, INK MARK, METALLIZED MARKING, INDENTATION OR OTHER FEATURE ON PACKAGE BODY
8. IF "A1" ID CORNER IS ON PACKAGE BODY, IT MUST BE LOCATED WITHIN THE ZONE INDICATED
9. ALL DIMENSIONS ARE IN MILLIMETERS

SYMBOL	JEDEC VARIATION NOT YET REGISTERED MIN	NOM	MAX	NOTE
A	–	–	1.20	
A1	.30	.35	.40	
A2	.78	.85	.92	
D	15.00 BSC			
E	13.00 BSC			
M	11 X 15			3
N	165			4
e	1.00 BSC			
b	.35	.45	.50	5
CENTER BALL MATRIX	N/A			

TOLERANCES UNLESS SPECIFIED		Integrated Device Technology, Inc. 2975 Stender Way, Santa Clara, CA 95054 PHONE: (408) 727-6116 FAX: (408) 492-8674 TWX: 910-338-2070	
DECIMAL ANGULAR			
XX± ±			
XXX±			
XXXX±			
APPROVALS	DATE	TITLE BQ PACKAGE OUTLINE 13.0 X 15.0 mm BODY FPBGA	
DRAWN JTP	05/01/00		
CHECKED		SIZE C	DRAWING No. PSC-4086 REV 00
		DO NOT SCALE DRAWING	SHEET 2 OF 2

Ordering Information



*Commercial temperature range only.

5297 drw 13

Datasheet Document History

12/31/99		Created new datasheet from 71V2576 and 71V2578 datasheets
	Pg. 1, 4, 8, 19	Added Industrial Temperature range offerings
04/04/00	Pg. 18	Added 100pin TQFP Package Diagram Outline
	Pg. 4	Add capacitance table for BGA package; Add Industrial temperature to table; Insert note to Absolute Max Ratings and Recommended Operating Temprature tables
06/01/00		Add new package offering, 13 x 15mm 165 fBGA
	Pg. 20	Correct BG119 Package Diagram Outline
07/15/00	Pg. 7	Add note reference to BG119 pinout
	Pg. 8	Add DNU note to BQ165 pinout
	Pg. 20	Update BG119 Package Diagram Outline Dimensions
10/25/00		Remove Preliminary from datasheet
	Pg. 8	Add reference note to pin N5 in BQ165 pinout, reserved for JTAG, $\overline{\text{TRST}}$

CORPORATE HEADQUARTERS
2975 Stender Way
Santa Clara, CA 95054

for SALES:
800-345-7015 or 408-727-6116
fax: 408-492-8674
www.idt.com

for Tech Support:
sramhelp@idt.com
800-544-7726, x4033

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