Edge720
500 MHz Pin Electronics Driver, Window Comparator, and Load

TEST AND MEASUREMENT PRODUCTS

Description

The Edge720 is a totally monolithic ATE pin electronics solution manufactured in a high-performance complementary bipolar process.

The three-statable driver is capable of generating 9V swings over a –1V to +12V range. In addition, 13V super voltage may be obtained under certain operating conditions. An input power down mode allows extremely low leakage current in HiZ. Thus, the Edge720 can help to eliminate relays that are typically used to isolate devices such as per pin measurement units from the driver/comparator/load.

The load supports programmable source and sink currents of ± 35 mA over a –1V to +12V range, or it can be completely disabled. In addition, the load is configurable and may be used as a programmable voltage clamp.

The window comparator spans a 13V common mode range, tracks input signals with edge rates greater than 6 V/ns and passes sub-ns pulses. An input power down mode allows for extremely low leakage measurements.

The inclusion of all pin electronics building blocks into a 52 lead QFP (10 mm body w/ exposed heat sink) offers a highly integrated solution that is traditionally implemented with multiple integrated circuits or discretes.

The Edge720 is a variant of the Edge710, with the following improvements:

- Reduced D+C+L Leakage Current
- Increased Super Voltage Range
- Additional VCM_IN buffer reduces the need for an external buffer when using the load circuit as a programmable clamp.

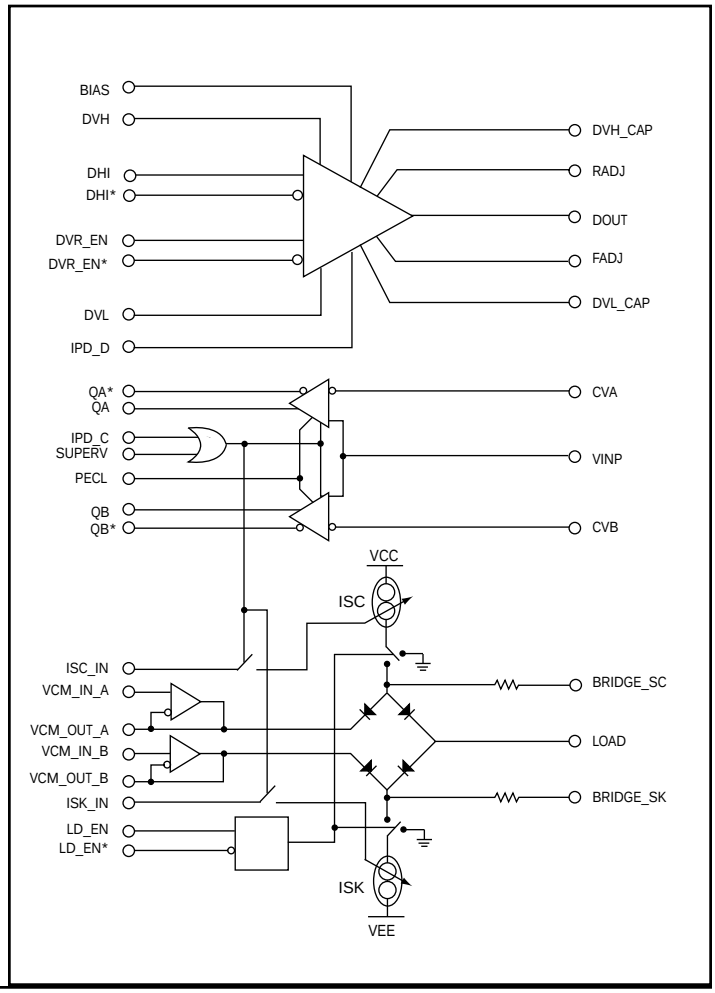
Features

- Fully Integrated Three-Statable Driver, Window Comparator, and Dynamic Active Load
- 13V Driver, Load, Compare Range
- +13V Super Voltage Capable
- ± 35 mA Programmable Load
- Comparator Input Tracking >6V/ns
- Leakage (L+D+C) < 2 µA (normal mode, typical)
- Leakage (L+D+C) < 30 nA (power-down mode, guaranteed)
- Small footprint (52 lead Exposed Pad QFP)

Applications

- Flash Memory Test
- VLSI Test Equipment
- Mixed-Signal Test Equipment
- Memory Testers (Bidirectional Channels)
- ASIC Verifiers

Functional Block Diagram



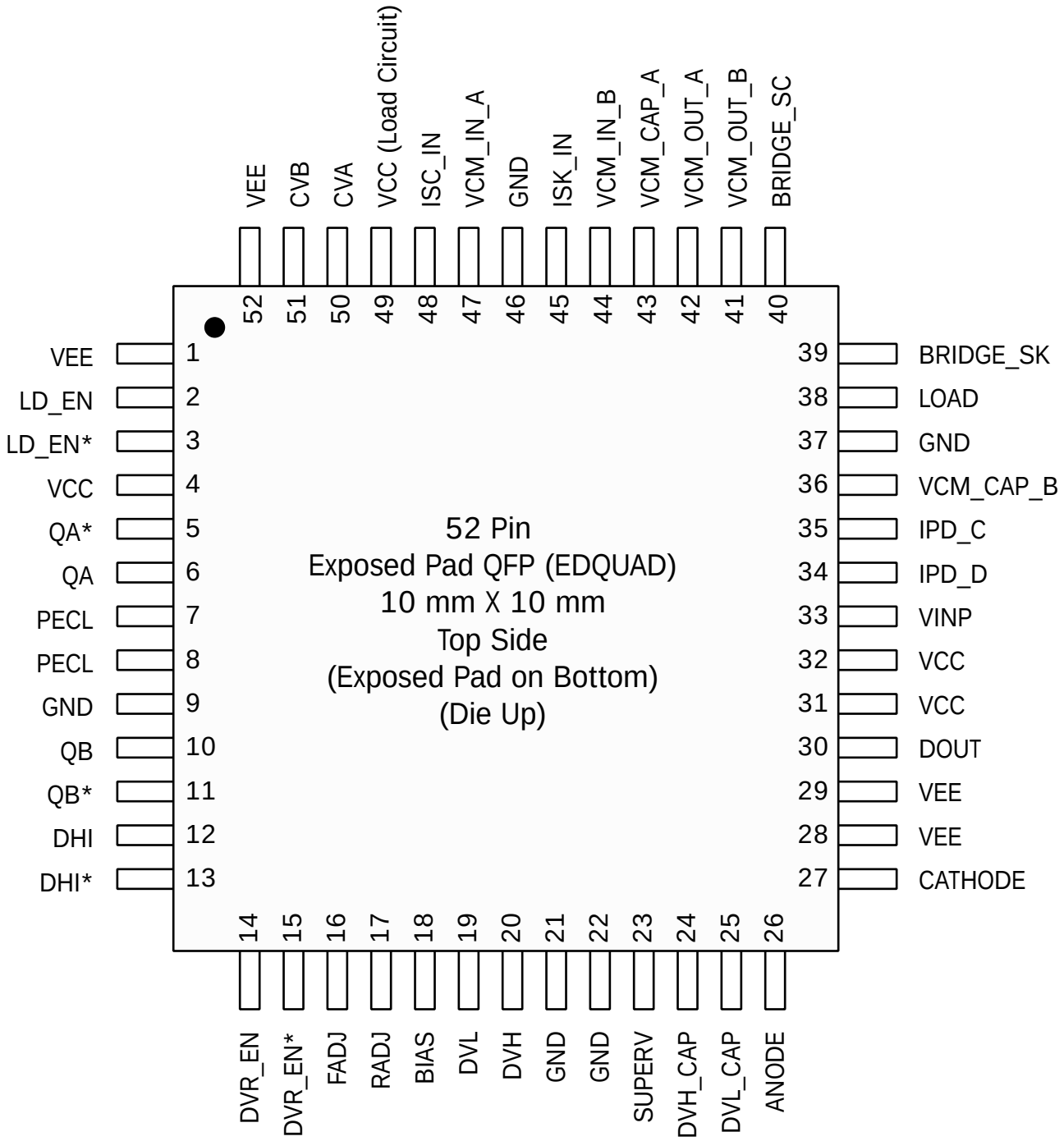
PIN Description

Pin #	Pin Name	Description
Driver		
30	DOUT	Driver Output.
12, 13	DHI / DHI*	Wide voltage differential input digital pins which determine the driver high or low level.
14, 15	DVR_EN / DVR_EN*	Wide voltage differential input digital pins which control the driver being active or in a high impedance state.
20, 19	DVH, DVL	High impedance analog voltage inputs which determine the driver high and low level.
24	DVH_CAP	Op amp compensation pin. A 100 pF capacitor should be connected to DVH.
25	DVL_CAP	Op amp compensation pin. A 100 pF capacitor should be connected to DVL.
17, 16	RADJ, FADJ	Input currents which determine the driver transition times.
18	BIAS	Analog current input which sets an internal bias current for the driver only.
34	IPD_D	TTL Driver Input Power Down control which slows the driver down and reduces the driver HiZ leakage current.
Comparator		
33	VINP	Analog voltage input to the positive input of comparators.
50, 51	CVA, CVB	Analog inputs which set the comparator thresholds.
6, 5 10, 11	QA / QA* QB / QB*	Differential ECL (or PECL) digital outputs of comparators A and B.
7, 8	PECL	Unbuffered power supply level for the comparator output stages which establishes either ECL or PECL digital levels.
35	IPD_C	TTL input that puts comparator and load in a power-down, non-functional mode.
23	SUPERV	TTL input that puts comparator and load in a power-down, non-functional mode.

PIN Description *(continued)*

Pln #	Pin Name	Description
Load		
38	LOAD	Load Output.
2, 3	LD_EN / LD_EN*	Wide voltage differential digital inputs which activate and disable the load.
47 44	VCM_IN_A VCM_IN_B	High impedance analog voltage inputs that program the commutating voltages.
48, 45	ISC_IN, ISK_IN	Analog current inputs which program the load source and sink currents.
43 36	VCM_CAP_A VCM_CAP_B	Commutating buffer op amp compensation pin (a .01 µF capacitor to ground is recommended).
42 41	VCM_OUT_A VCM_OUT_B	Commutating voltage pins (a .01 µF capacitor to ground is recommended).
40 39	BRIDGE_SC BRIDGE_SK	Diode bridge connections to the output bridge that bypass the internal current sources.
Power Supplies/ Miscellaneous		
27 26	CATHODE ANODE	Terminals of the on-chip thermal diode string.
4, 31, 32, 49	VCC	Positive power supply level. (Pin 49 is the designated VCC for the load circuit.)
1, 28, 29, 52	VEE	Negative power supply level.
9, 21, 22, 37, 46	GND	Device Ground.

PIN Description *(continued)*



Driver Circuit Description

Introduction

The Edge720 features a driver circuit that can be used to drive voltage levels over a –1V to +12V range at frequencies of up to 500 MHz at the DOUT pin. In addition, the driver can be used to force a super voltage level of up to 13V and can also be placed in a high impedance state. The driver circuit of the Edge720 is a variant of the driver circuit of the Edge710, and was specifically designed to offer a low leakage solution to FLASH™ memory testing.. A block diagram of the driver can be seen in Figure 1.

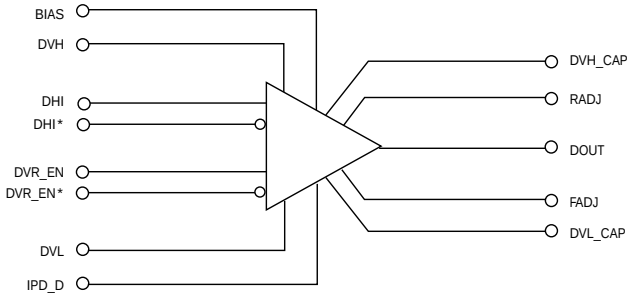


Figure 1. Block Diagram of the Edge720 Driver

Driver Digital "Flex-In" Inputs

The Edge720 driver circuit features "Flex-In" control inputs for the driver enable (DRV-EN(*)) and driver data (DHI(*)) inputs that allow the driver to receive ECL, TTL, CMOS, or custom signal levels. These "Flex-In" inputs are wide voltage differential inputs whose operation is described in Table 1.

	Min	Max	Units
Common Mode Input Range	VEE + 2.75	5.0	V
Differential Input Range	±0.25	±4.0	V

Table 1. "Flex-In" Input Characteristics

Single-ended operation of these inputs can be accomplished by connecting the inverting input (DHI* or DRV_EN*) to the desired DC threshold level.

Driver Enable Inputs (DRV_EN(*))

The driver enable inputs, DRV_EN(*), control whether the driver is forcing a voltage at DOUT, or is placed in a high impedance state. If the voltage applied to DRV_EN is more positive than that applied to DRV_EN*, the driver, will force the DOUT voltage to either DVH or DVL (determined by DHI(*)). If the voltage applied to DRV_EN is less than that applied to DRV_EN*, the driver will force the DOUT pin to a high impedance state (see Table 2 for DRV_EN(*) functionality). It is important to note that for predictable operation, DRV_EN(*) pins must not be left floating.

Driver Enable	Driver Data	DOUT
DRV_EN > DRV_EN*	DHI > DHI*	DVH
DRV_EN > DRV_EN*	DHI < DHI*	DVL
DRV_EN < DRV_EN*	X	HiZ

Table 2. DRV_EN(*) and DHI(*) Control Input Functionality

Input Power Down

The driver input power down pin, IPD_D, is a TTL compatible input that can be used to place the driver in input power down (IPD) mode. IPD_D functionality is described below in Table 3.

IPD_D	Operation
0	Normal
1	IPD Mode

Table 3. IPD_D Functionality

IPD mode should be invoked when the driver is in high impedance mode (DRV_EN < DRV_EN*). When in IPD mode, the driver output leakage will be minimized. It is important to note that IPD_D should not be left floating. If IPD_D is not being used, it should be connected to GND.

Circuit Description *(continued)*

Driver Level Inputs

The DVL and DVH pins are high impedance analog voltage inputs that establish the driver output levels of a logical "1" or "0" at DOUT. Due to possible offsets inherent in the driver, it may be necessary to apply a voltage to DVH or DVL that is slightly larger in magnitude than the desired DOUT voltage.

Driver Stability/Compensation

In order to ensure stability, 100 pF chip capacitors (with good high frequency characteristics) should be connected between the DVH and DVH_CAP, as well as between DVL and DVL_CAP pins. The connectivity of these external components can be seen in Figure 2.

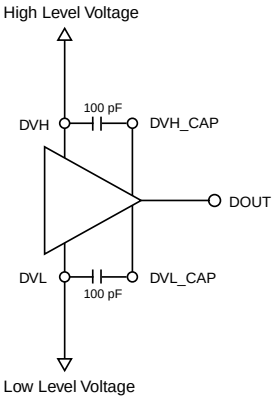


Figure 2. Driver External Compensation Component Connectivity

These capacitors are intended to improve the driver output response to fast changes in the DVL(H) input voltage levels. Using 100 pF capacitors will allow the DOUT voltage to track DVL(H) level changes at slew rates up to 400V/µs. If it is desired to operate the Edge720 in an application that can tolerate DVL(H) level changes (with the driver circuit enabled) of less than 100V/µs, these capacitors can be omitted without any reduction in part performance.

Super Voltage Operation

The Edge720 may be used to drive a super voltage level of up to 13V at the driver output, DOUT. In order to ensure that the desired super voltage level is driven, a slightly higher voltage will need to be switched onto the DVH or DVL pins to account for possible offsets in the driver.

One Solution that can be used to implement super voltage functionality is included as a feature on the Edge4707. The Edge4707B features an analog MUX, which was designed to switch the driver input voltages between super voltage and standard levels. Analog MUX connectivity can be seen below in Figure 3.

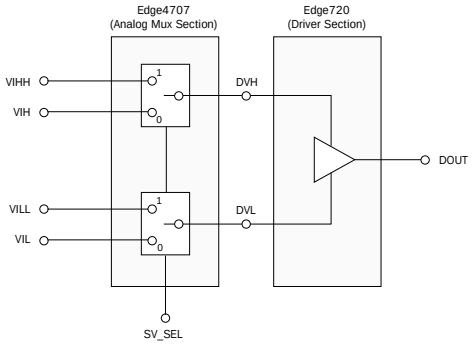


Figure 3. Analog MUX Connectivity for Super Voltage Operation

It is important to note that when driving a super voltage level, the driver differential input voltage (DVH – DVL) must be in compliance with the specified range. Connecting the super voltage inputs (VIHH and VILL) of each analog MUX to the same super voltage source will ensure this. In addition, if the Edge720's comparator and load are connected to the driver output, as in typical relay-less test system architecture, they will need to be protected during super voltage operation as follows:

1. Comparator must be placed in input power down mode (IPD_C = 1 or SUPERV = 1)
2. Differential load voltage specification (VLOAD – VCM_IN_A(B)) must be met
3. Load should be disabled (ISK_IN, ISC_IN = 0 mA, LD_EN < LD_EN*)

Compliance with the precautions above will ensure that the Edge720 is not inadvertently damaged during super voltage operation.

Driver Current Inputs

The Edge720 driver also features a trio of current controlled inputs (BIAS, RADJ, and FADJ) that can be used to optimize the driver circuit's power consumption and AC characteristics to allow the Edge720 to be custom tailored to a broad spectrum of applications.

Driver Bias Input

The BIAS pin is an analog current input that establishes the internal driver bias current. This current, to some degree, also establishes the overall power consumption and AC performance of the driver. An external current source, such as a group F DAC on the Edge6420, can be used to provide a programmable current supply as well as minimize part-to-part performance variation within a test system to optimize performance. In lieu of using an Edge6420 Group F DAC for a programmable current source, a precision external resistor can be used to set the BIAS current as seen in Figure 4.

BIAS input current can range from 0.5 mA to 1.25 mA. In general, increasing the BIAS input current will result in faster AC swings and increased power consumption. However, optimum BIAS input current will be a function of RADJ and FADJ input currents and thus BIAS cannot be set independently.

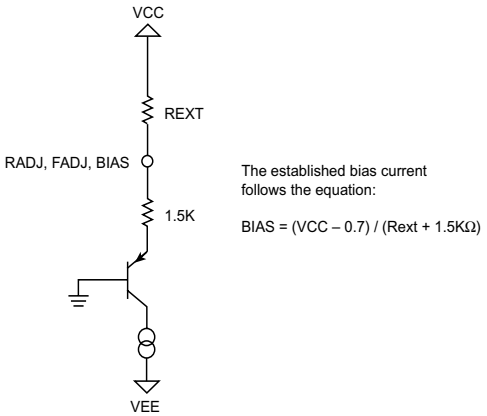


Figure 4. Using an External Resistor to Establish the Input Current at BIAS, RADJ, and FADJ

Driver Slew Rate Adjustment

The RADJ and FADJ pins are current input pins that can be used to adjust the driver rising edge and falling edge slew rates, thus determining driver rise and fall times. The rising edge adjust pin, RADJ, controls the rate at which an output signal at DOUT transitions from low to high while the falling edge adjust pin, FADJ, controls the rate at which an output signal transitions from high to low. Similar to the BIAS input, it is recommended that an Edge6420 group F DAC provide these inputs. The Edge6420 is designed to facilitate all of the necessary inputs to operate the Edge720. However, in lieu of using the Edge6420, an external precision resistor can be connected as shown in Figure 4 to provide the RADJ and FADJ input currents.

Driver DC Accuracy

In the ideal case, the voltages applied to the driver level inputs (DVL and DVH) will correspond 1:1 with the driver output voltage appearing at DOUT as can be seen in Figure 5.

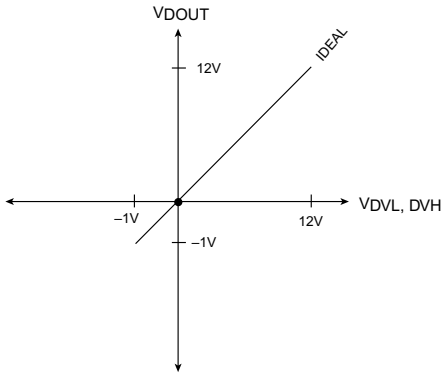


Figure 5. Ideal Driver DC Transfer Characteristic

In reality, the transfer characteristic of the driver circuit is non-ideal and thus the driver level input voltages do not correspond 1:1 with the driver output voltage. There are three parameters that can be used to quantify the deviation of the non-ideal driver transfer characteristic from the ideal one. These parameters are all specified in the "Driver DC Accuracy" section of the datasheet and are as follows:

1. Offset Voltage
2. Gain Error
3. Linearity Error

Circuit Description *(continued)*

The first parameter that will be discussed is offset voltage. Offset voltage is defined as the difference between the driver level input voltage and the driver output voltage when the input is programmed to 0V. Offset voltage manifests itself as a DC shift of the ideal driver transfer characteristic as can be seen in Figure 6.

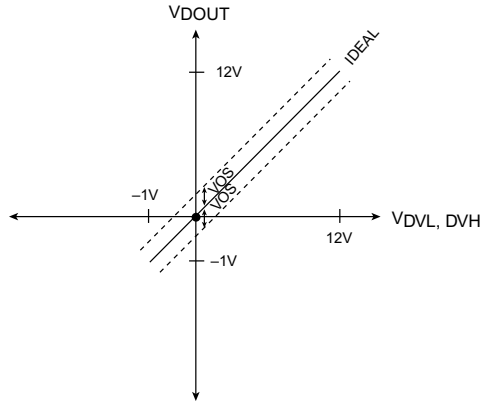


Figure 6. The Effect of Offset Voltage on the Ideal Driver DC Transfer Characteristic

The second parameter that will be discussed is gain error. Gain error is due to the fact that the gain of the driver circuit may not be unity (constant) as in the ideal case. This can have an effect on the slope of the ideal driver DC transfer characteristic as can be seen in Figure 7.

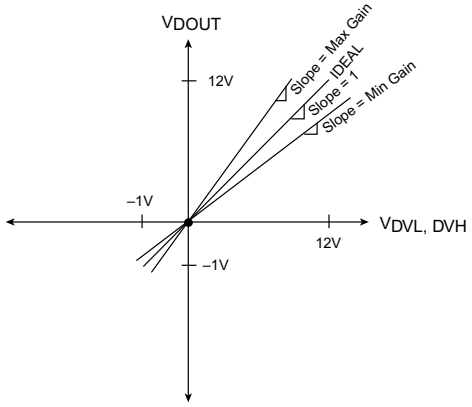


Figure 7. The Effect of Gain Error on the Ideal Driver DC Transfer Characteristic

The final parameter that is used when quantifying the deviation of the non-ideal transfer characteristic from the ideal one is linearity error. Linearity error is used to account for the fact that the driver DC transfer characteristic may not be completely linear, but guaranteed to fall within a window defined by the driver linearity specification (see Figure 8).

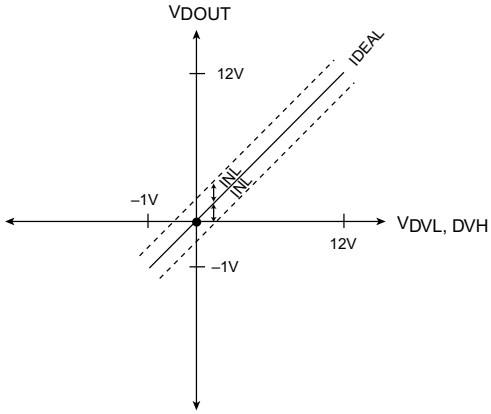


Figure 8. The Effect of Linearity Error on the Ideal Driver DC Transfer Characteristic

Of the three parameters that quantify the non-ideal behavior of the driver DC transfer characteristic, both offset voltage and gain error can be accounted for in software calibration and thus overall driver DC accuracy is governed by the linearity error of the device.

Comparator Circuit Description

Introduction

The Edge720 features two on-chip comparators that are connected to form a window comparator. This window comparator can be used to determine whether an input signal at VINP is within a threshold window determined by the CVA and CVB pins. The comparator on the Edge720 is a variant of the comparator on the Edge710 and has been specifically designed to improve resistance to breakdown at super voltage levels. A block diagram of the Edge720's window comparator circuit can be seen in Figure 9.

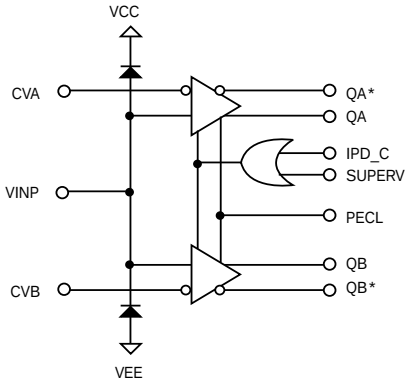


Figure 9. Block Diagram of the Edge720's Window Comparator

Comparator Inputs

The comparator circuit features two digital, three analog, and three power supply inputs. The digital inputs, IPD_C and SUPERV, can be used to place the comparator into input power down mode. The analog inputs are CVA, CVB, and VINP. CVA and CVB set the comparator thresholds, while VINP is the comparator input voltage signal. The comparator output power supply input is PECL. The functionality of all of these inputs is described later in this section.

Comparator Input Power Down

The IPD_C and SUPERV pins are TTL compatible inputs that can be used to place the Edge720's window comparator circuit into "Input Power Down" mode. IPD_C and SUPERV functionality is described in Table 4.

SUPERV	IPD_C	Operation
0	0	Normal
0	1	IPD mode
1	0	IPD mode
1	1	IPD mode

Table 4. IPD_C Functionality

When the comparator is placed in IPD mode, the comparator input, VINP, can be safely exposed to super voltage levels. Since the comparator circuit is not functional in this mode, it is recommended that IPD_C be connected to GND when not in use. In addition to the input power down characteristics of VINP, SUPERV and IPD_C control switches that internally connect the ISK_IN and ISC_IN inputs to protect the load circuit.

Comparator Analog Inputs

VINP is a high impedance analog voltage input pin that is used to read a desired voltage signal. VINP is internally connected to the non-inverting inputs of both on-chip comparators (as seen in Figure 9). VINP is also connected to two internal over-voltage diodes that are connected to VCC and VEE. These diodes are sized to handle up to 100 mA of current. CVA and CVB are high impedance analog voltage inputs that are used to set the threshold levels of the window comparator. Although CVA(B) are high speed inputs, they do not require bypassing as long as the source impedance is not inductive (which can happen with a long, narrow PCB trace). If needed, small (≈100 pF) capacitors can be connected between the CVA(B) pins and GND to ensure stability and low noise.

Circuit Description *(continued)*

Comparator Outputs

The comparator outputs QA(*) and QB(*) are open emitter outputs that can be used to determine where the input voltage measured at the VINP input is located in relation to the comparator thresholds, CVA and CVB. These outputs are normally terminated through a 50Ω resistor connected to PECL – 2V. Other possible termination schemes are discussed in "AN1003-ECL Output Termination Techniques." Comparator output functinality is described in Table 5.

VINP (V)	QA	QB
VINP < CVA(B)	0	0
VINP > CVA(B)	1	1
CVA < VINP < CVB	1	0
CVA > VINP > CVB	0	1

Table 5. Window Comparator Truth Table

Comparator Power Supplies

PECL is the comparator output power supply input that determines the logic levels of the comparator circuit's differential outputs QA(*) and QB(*). When connected to GND, the comparator outputs will function as standard ECL outputs. However, by increasing the value of the PECL input voltage, QA(*) and QB(*) will track the PECL input voltage and also increase as shown below in Figure 10.

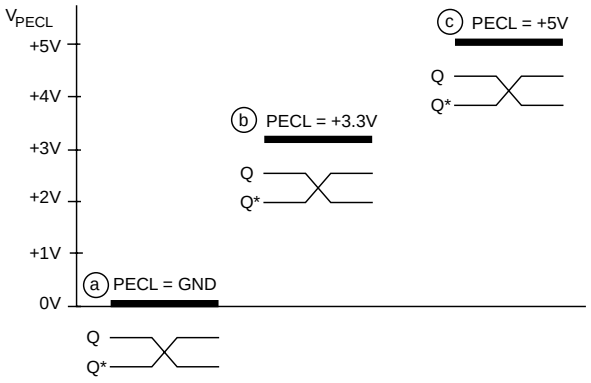


Figure 10. The Influence of the PECL Input on Comparator Outputs

When operating PECL at voltage levels above GND, pins 7 and 8 should be bypassed with 0.1 µF capacitors to GND to ensure stability of the comparator inputs.

Comparator DC Accuracy

The DC accuracy of the Edge720's comparator circuitry is quantified by the following datasheet specified parameters:

1. Comparator input offset voltage
2. Comparator hysteresis

Comparator input offset voltage quantifies the region around the programmed threshold voltage applied to CVA(B) at which the voltage applied to VINP will cause the comparator output to transition states. Or more simply, it describes how far the actual threshold voltage of the comparator may deviate from the value which has been programmed at CVA(B).

Comparator hysteresis quantifies the difference in the comparator threshold level when the comparator is triggered by a signal with a positive slope as opposed to one with a negative slope when the programmed threshold voltage at CVA(B) is held constant. In order words, hysteresis is a measure of the change in threshold voltage as a function of the comparator output state (see Figure 11). Typically, hysteresis is used to prevent multiple comparator output transitions due to slow input slew rates in a noisy environment. These slower inputs remain in the transition region for longer periods of time, allowing noise present to cause repeated threshold crossings.

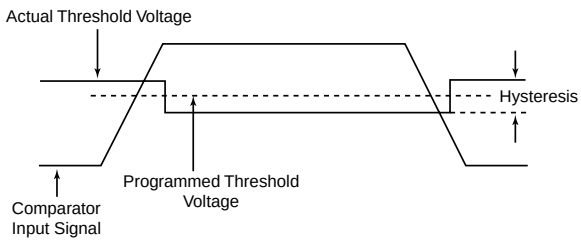


Figure 11. Hysteresis

Circuit Description *(continued)*

Load Circuit Description

Introduction

The Edge720 features a programmable load circuit which is capable of sourcing or sinking up to 35 mA over a –1V to +12V range, or being placed in a high impedance state. This circuit also features "split" commutating voltage inputs that allow it to be configured as a programmable voltage clamp. In addition, the BRIDGE_SC and BRIDGE_SK pins allow the load circuit's diode bridge to be connected to external current sources for increased low current accuracy. A functional schematic of the Edge720's load circuit can be seen below in Figure 12.

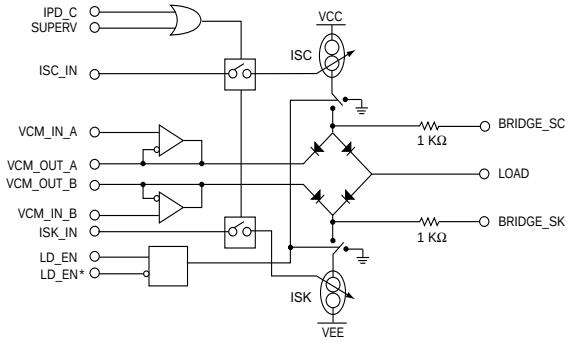


Figure 12. Functional Schematic of the Edge720's Load Circuit

Load Enable

The Edge720 load circuit features a differential "Flex In" input labeled LD_EN(*). This input can be used to isolate the diode bridge from the on-chip current supplies, leaving the LOAD pin in a high impedance state. "Flex In" inputs are wide voltage inputs which allow the LD_EN(*) pin to be used with ECL, TTL, CMOS, or custom level inputs, and whose characteristics are described in Table 1. LD_EN(*) functionality is described in Table 6.

Load Enable Input	Operation
LD_EN < LD_EN*	High Impedance
LD_EN > LD_EN*	Active

Table 6. Load Enable Input Functionality

Single-ended operation can be attained by connecting the inverting input, LD_EN* to the desired DC threshold level.

Current Programming Inputs

ISC_IN and ISK_IN are independently adjustable analog current inputs that control the amount of current being supplied to the diode bridge by the on-chip current supplies (see Figure 12). Consequently, these inputs can be used to program the amount of current being sourced (ISC_IN) or sunk (ISK_IN) at the load circuit output pin (LOAD). The on-chip current supplies have been designed to have a nominal gain of 20. Therefore, the magnitude of current sourced or sunk is equal to the magnitude of the control current scaled by a factor of 20. The ISK_IN and ISC_IN current programming inputs should be routed on a PCB such that coupling between the control inputs and the LOAD, VCM_OUT_A and VCM_OUT_B pins is minimized. Finally, it is also recommended that 1 kΩ of external series resistance be connected between these inputs and the source controlling them. A group E DAC on the Edge6420 offers a nice solution to controlling these inputs.

Commutating Voltage Inputs

VCM_IN_A(B) are high impedance analog voltage inputs to on-chip buffers that are used to set the voltage level at which the diode bridge switches from sourcing to sinking current when the load is connected as a standard active load (see Figure 15). If the voltages applied to VCM_IN_A(B) are more positive than that on the LOAD pin, the bridge will source current from the LOAD pin (see Figure 13). If the voltage applied to VCM_IN_A(B) is less than that at the LOAD pin, the bridge will sink current through the LOAD pin (see Figure 14).

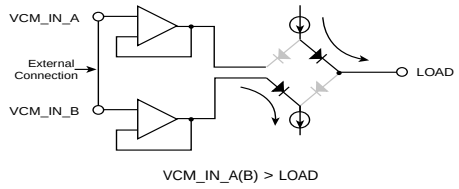


Figure 13. Edge720 Load Circuit Sources Current

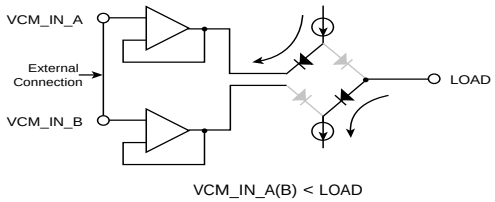


Figure 14. Edge720 Load Circuit Sinks Current

Circuit Description *(continued)*

Commutating Voltage Compensation

The VCM_CAP_A(B) pins are internal commutating buffer compensation pins that require a fixed 0.01 µF chip capacitor (with good high frequency characteristics) connected to GND.

Commutating Buffer Outputs

VCM_OUT_A(B) are connected to the outputs of the on-chip commutating buffer, whose output voltages are determined by VCM_IN_A(B) (see Figure 12). The connection scheme of these pins will determine the configuration of the Edge720 load circuit. This allows the Edge720's load circuit to be quite versatile in that it can be configured in multiple ways.

Standard Active Load Configuration

One way to configure the load circuit of the Edge720 is as a standard active load. In order to operate the load as a standard active load, VCM_IN_A can be connected to VCM_IN_B and driven with the same source as shown in Figure 15. The 0.01 µF bypass capacitors shown in Figure 15 are needed to supply current to the diode bridge during fast transients. These capacitors should be placed as close to the VCM_OUT_A(B) pins as possible to ensure stability and quick response to fast transitions on the LOAD output pin.

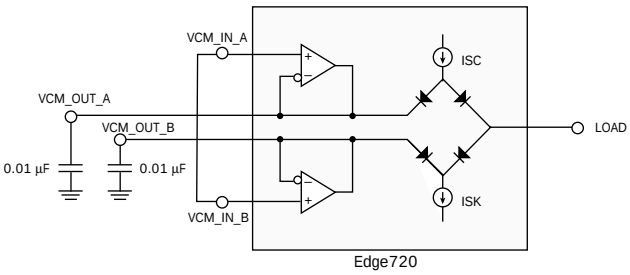


Figure 15. Edge720 Load Circuit Connected as a Standard Active Load

Programmable Clamp Configuration

Another way to configure the load circuit of the Edge720 is as a programmable voltage clamp. Using this configuration allows the Edge720 load circuitry to be used as a transmission line termination scheme to minimize the reflections caused by an unmatched line. Using the Edge720 load circuit in this configuration offers a superior clamping solution to the more traditional voltage controlled diode clamp method. To configure the Edge720 load circuit as a programmable clamp, the load circuit should be configured as in Figure 16. The 0.01 µF bypass capacitors shown in Figure 16 are needed to supply current to the diode bridge during fast transients. These capacitors should be placed as close to the VCM_OUT_A(B) pins as possible to ensure stability and quick response to fast transitions on the LOAD output pin.

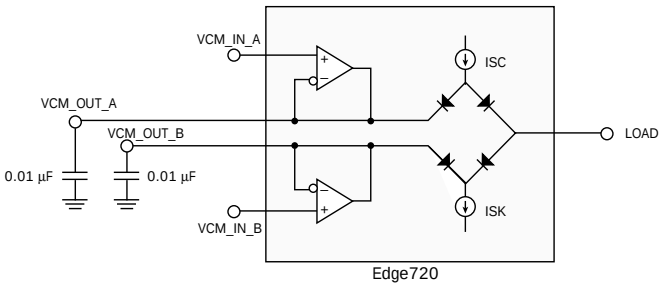


Figure 16. Edge720 Load Circuit Connected as a Programmable Voltage Clamp

With the load configured in this manner, the voltage at the LOAD pin will be clamped within a range determined by the voltage at VCM_OUT_A and VCM_OUT_B. The voltage at VCM_OUT_A determines the low voltage-clamping limit, while the voltage at VCM_OUT_B determines the high voltage-clamping limit. It is important to note that when using the load circuit in this manner, ISC_IN and ISK_IN should be set to their maximum values.

External Diode Bridge Connections

The Edge720 features two pins, BRIDGE_SC and BRIDGE_SK, which allow access to the top and bottom of the diode bridge through 1 kΩ series resistors (see Figure 12). These pins can be connected to external current sources whenever it is desired to use sources that are more accurate than the on-chip sources. Connecting these pins may degrade the high impedance characteristics of the load when it is not enabled unless isolation relays are used to isolate the external current sources from the diode bridge.

Circuit Description *(continued)*

Load Circuit Current Accuracy

In the ideal case, the current that the load circuit will source or sink at the load pin will be equal to the magnitude of the current input applied to the current programming input pin (ISC_IN, ISK_IN) scaled by a factor of 20. This results in the ideal load circuit transfer characteristic seen in Figure 17.

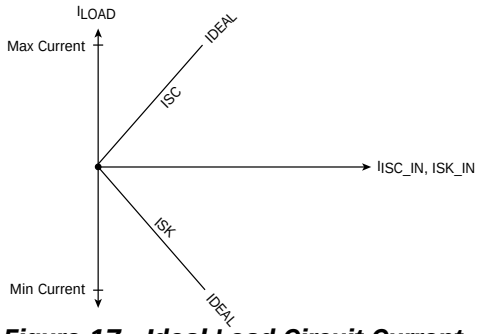


Figure 17. Ideal Load Circuit Current Transfer Characteristic

In reality, the transfer characteristic of the load circuit current is non-ideal and thus the current being sourced or sunk at the LOAD pin will not be equal to the magnitude of the programming input currents at ISC_IN or ISK_IN scaled by a factor of 20. To account for these non-ideal effects, the accuracy of the on-chip current sources (ISC, ISK) is quantified by three parameters. These parameters are all specified in the "Programmable Load Current Accuracy" section of the datasheet and are as follows:

1. Source/Sink Current Offset
2. Source/Sink Current Gain
3. Source/Sink Current Linearity Error

The Source/Sink offset current specification quantifies the amount of current that may be needed at the programming inputs (ISC_IN and ISK_IN) before the current being sourced or sunk at the LOAD pin will actually turn on (see Figure 18). This allows for the offset to be calibrated to ensure that zero input current results in zero output current.

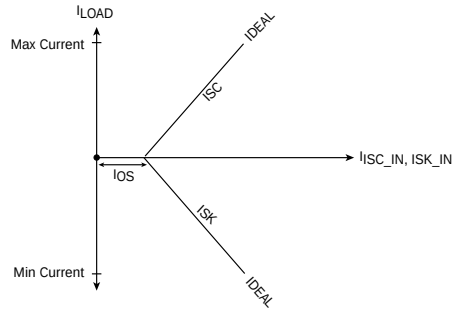


Figure 18. Source/Sink Current Offset

The Source/Sink current gain specification accounts for the fact that the gain of the actual on-chip current source (ISC, ISK) may not be 20 as in the ideal case. This may result in the possibility of a deviation in the slope of the load circuit transfer characteristic when it is in the linear region as shown in Figure19.

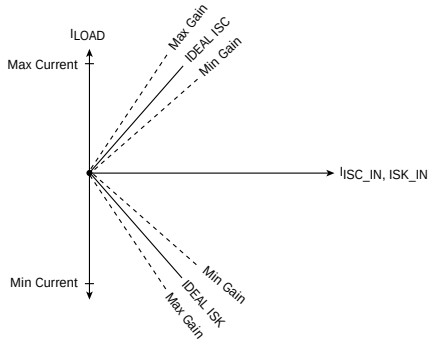


Figure 20. Source/Sink Current Gain

The Source/Sink current linearity specification quantifies the amount the load transfer characteristic deviates from a predicted ideal transfer characteristic in the linear region as shown in Figure 20.

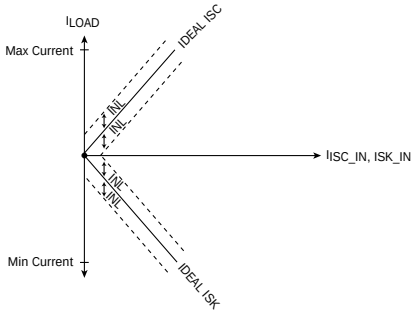


Figure 20. Source/Sink Current Linearity

Load Circuit Commutating Voltage Accuracy

The accuracy of the load circuit commutating voltage is dependent upon the commutating buffer. The accuracy of this buffer is quantified by three parameters. These parameters are all specified in the "Commutating Voltage Accuracy" section of the datasheet and are as follows:

1. Offset Voltage
2. Gain Error
3. Linearity Error

These parameters affect the ideal voltage transfer characteristic of the commutating buffer in the same manner as they affect the ideal transfer characteristic of the driver circuit. Please refer to the Driver DC Accuracy section for a detailed description of these effects.

Additional Features

Thermal Monitor

The Edge720 features an on-chip string of five thermal diodes that allow for a method of accurate die temperature measurement (see Figure 21). Using an external bias current of 100 µA injected through the string, the Edge720 junction temperature follows the equation:

$$Tj[^{\circ}C] = \{ANODE - CATHODE)/ 5 - .7752\} / (-.0018)$$

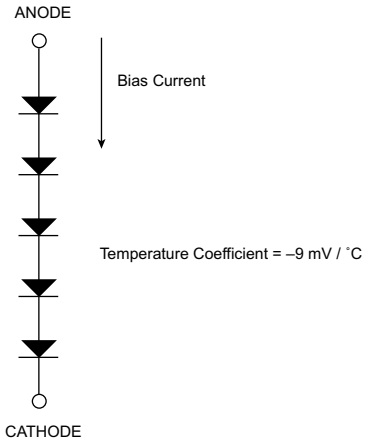


Figure 21. Edge720 Thermal Diode String

Low Leakage Pin Electronics Implementation

The Edge720 is capable of supporting a total DCL (driver + comparator + load) leakage of less than 100 nA. This extremely low leakage current capability enables the Edge720 to be ideally suited for relay-less ATE system architecture. In order to realize low leakage functionality, the following conditions must be met:

1. Driver circuit must be in IPD mode (IPD_D = 1)
2. Comparator circuit must be in IPD mode (IPD_C = 1)
3. Load circuit must be disabled (high impedance mode: LD_EN < LD_EN*, ISC_IN = ISK_IN = 0 mA)

Connectivity

The Edge720 can be easily combined with other Edge devices to create simple, yet high performance solutions to many challenges in ATE. One possible ATE solution that consists of the Edge6420 DAC, Edge4707B PMU, and Edge720 DCL is shown in Figure 24.

Power Sequencing

In order to avoid the possibility of latch-up, the following power-up requirements must be satisfied:

1. VEE ≤ GND ≤ VCC at all times
2. VEE ≤ All Inputs ≤ VCC

The following power sequencing can be used as a guideline when using the Edge720:

Power Up Sequence
1. VEE
2. VCC
3. Analog Inputs
4. Digital Inputs

Power Down Sequence
1. Digital Inputs
2. Analog Inputs
3. VCC
4. VEE

Driver/Comparator/Load Output Circuit

The recommended circuit for combining the driver, comparator, and load outputs to a single DUT pin is shown in Figure 1. The inductors in the circuit compensate for the parasitic capacitance of the load and comparator pins, minimizing the imaginary part of the impedance to both incoming and outbound signals. This yields the fastest driver rise times as well as the smallest amount of distortion of the signal going into the comparator. The amount of distortion caused by this compensation network is small compared to the other sources of distortion.

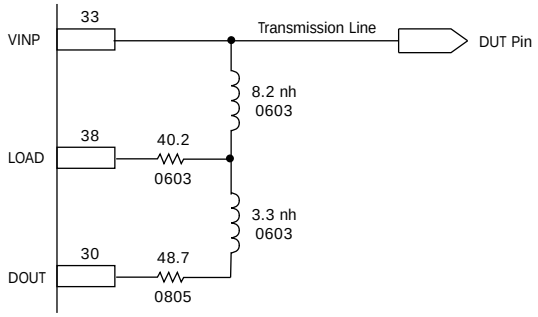


Figure 22. Optimum Circuit for Combined Edge720 Outputs

Computing Output Voltage Range

The output voltage range of the driver and load and the input range of the comparator are a function of VCC and VEE and their individual voltage overheads, offset, and gains specified for each.

For example, the driver's output high range (no load) is shown below.

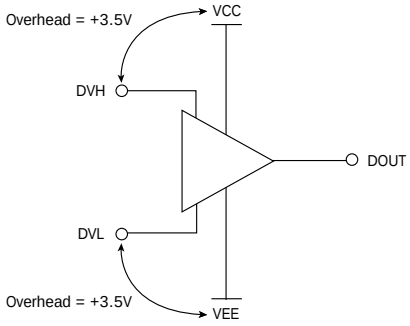


Figure 23. Driver Output High Range (no Load)

For DOUT(high) of +11.75V, DVH may need to be overdrived as follows:

$$\left(\frac{+11.75V}{GAIN}\right) + \text{Offset (of DOUT vs. DVH)}$$

$$\text{i.e. } \left(\frac{+11.75V}{0.985}\right) + 125\ mV = 12.05V = DVH$$

Hence, VCC(min) needs to be:

$$+12.05V + \text{Overhead}$$

$$\text{i.e. } +12.05 + 3.5V = 15.55V$$

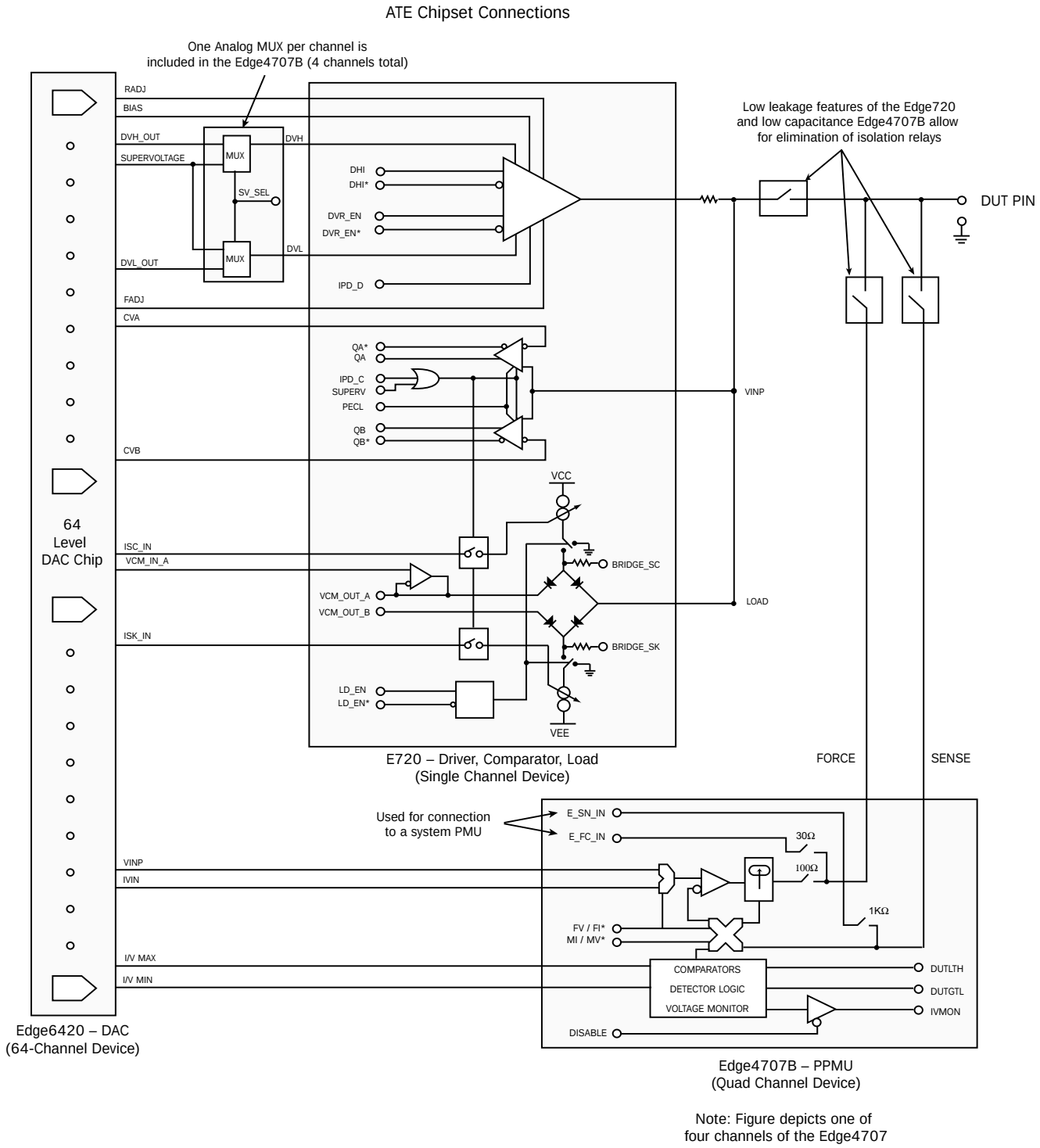
For the application of DOUTmax = +11.75V, VCC must be greater than 15.55V. Similar is true for all input/output ranges specified.

Power Supply Bypassing

Each section of the Edge720 has separate VCC and GND pins which are not connected to each other internally, so each ground pin must be connected to analog ground by the shortest possible path, and each of the VCC pins must have power and a bypass capacitor provided. These bypass capacitors should be placed as close to the power pin as possible for optimum filtering and stability. Pins 31 and 32 provide VCC to the driver circuit. Pins 21 and 22 connect the driver GND. Pin 4 is VCC, and pin 9 is GND for the comparator circuit. Pin 49 provides VCC and pins 37 and 46 provide GND to the load circuit.

All of the VEE pins are connected together via the exposed heat slug on the bottom of the part. Each of these go to separate sections of the part, so should be bypassed separately for best noise filtering and stability. Pin 21 and 22 provide VEE to the driver circuit, pin 1 provides it to the comparator, and pin 52 connects VEE to the load circuit.

Application Information *(continued)*

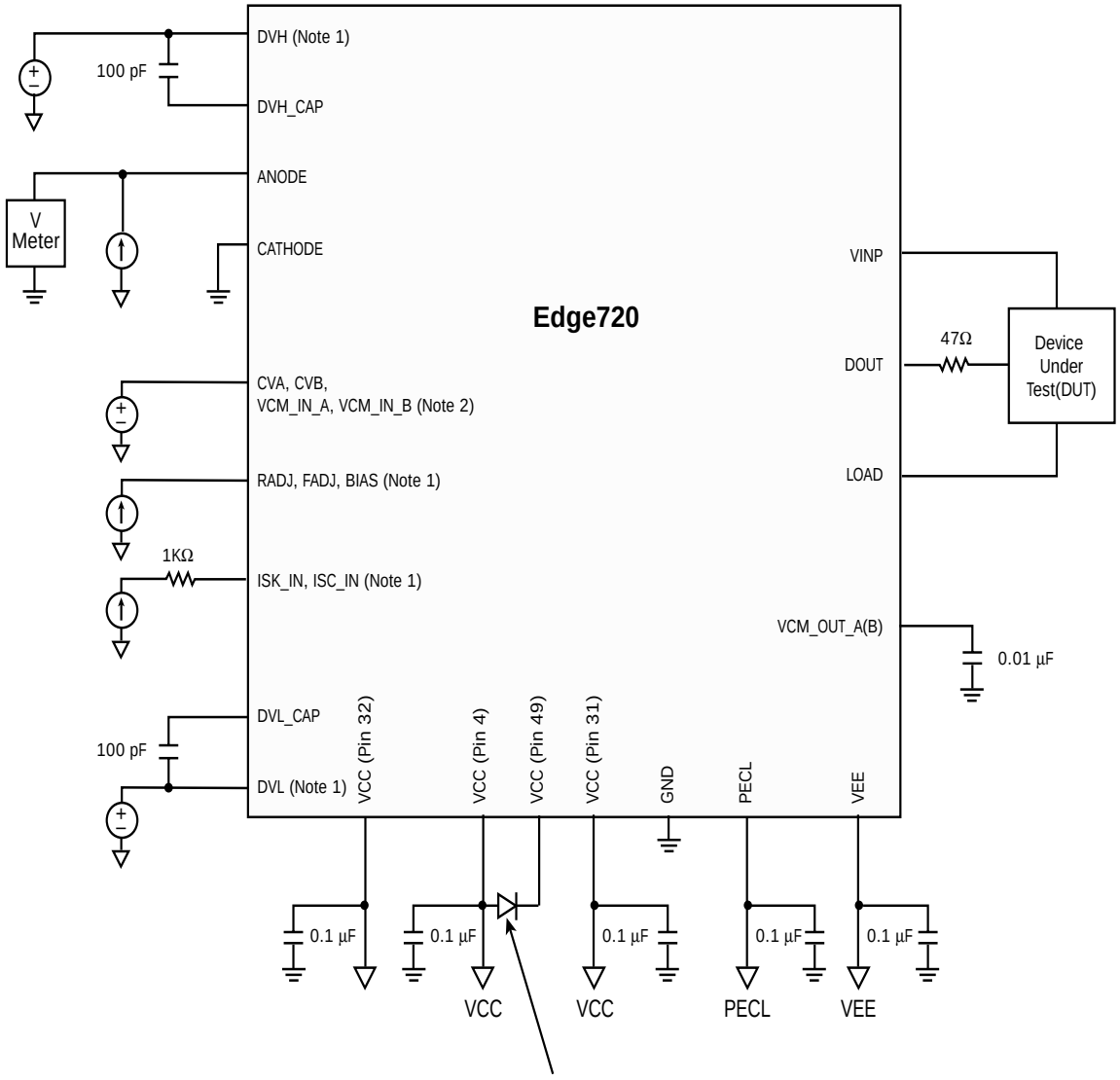


Actual implementation of chipset may differ. The diagram above is conceptual only.

Figure 24. Connectivity of Edge6420 DAC, Edge4707B PMU, and Edge720 DCL

Application Information *(continued)*

Required External Components

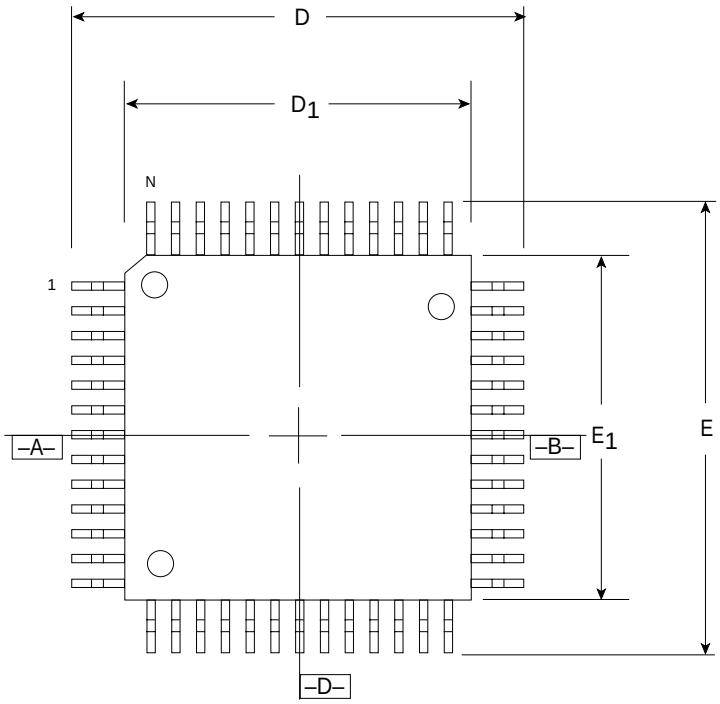


A silicon diode with 150 mA of forward current capability is used to limit the VCC power supply voltage to the load circuit. Its purpose is to ensure that the VCC – VCM_IN_A(B) breakdown voltage of 16V is not exceeded.

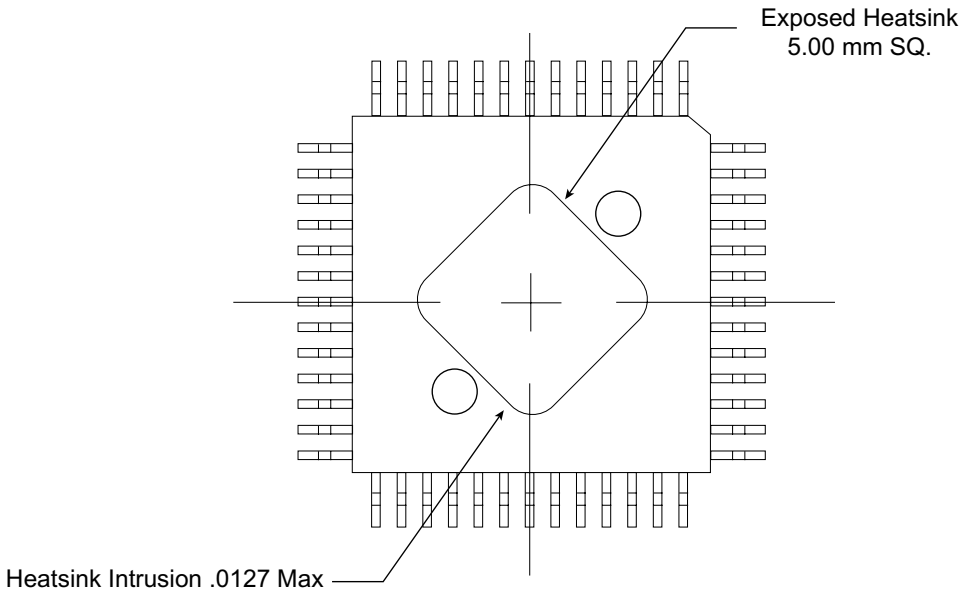
Note 1: The DVH, DVL, RADJ, FADJ, and BIAS inputs do not normally require bypass capacitors for the Edge720 to operate correctly. However, it is important that the signals supplied to these inputs be routed carefully to avoid noise pick-up or feedback from the driver output signal. If needed, bypass capacitors can be placed in front of these inputs to reduce the amount of pick-up.

Note 2: The ISKIN, ISCIN, VCM_IN_B and VCM_IN_A inputs do not require bypass capacitors if the input traces are routed to avoid noise pick-up and feedback from the output stage. It is especially important that the ISK input be routed away from the output stage since this signal is the inverse of the applied output signal and can feed back to itself, causing oscillations. If needed, bypass capacitors can be placed before any of these pins without degrading part performance.

Edge720BXF
10 mm X 10 mm x 1.4 mm Exposed Pad QFP



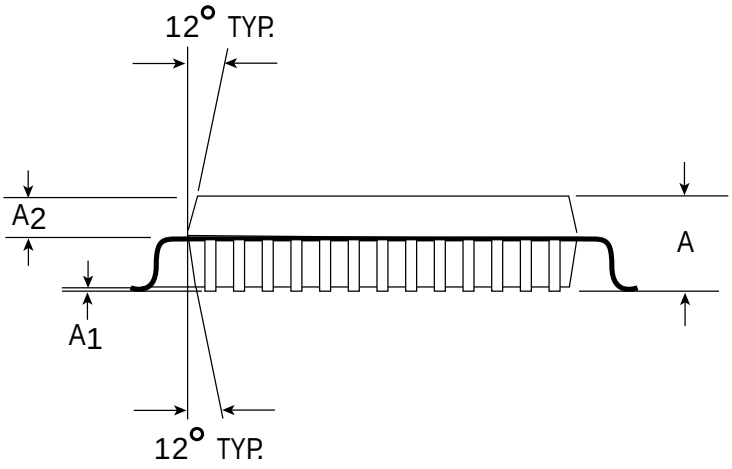
Top View



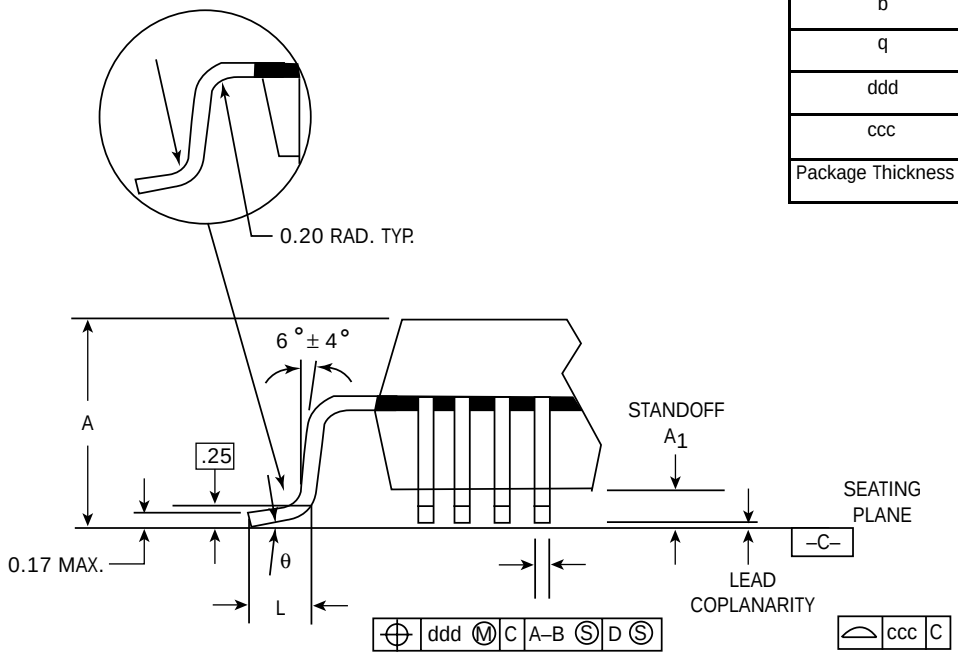
Bottom View

Package Information *(continued)*

Edge720BXF
10 mm X 10 mm x 1.4 mm Exposed Pad QFP



Footprint		
Dims.	**Tolerance**	**Body + 2.00 mm**
A	MAX.	1.60
A1		.05 min. / .15 max
A2	±.05	1.40
D	±.20	12.00
D1	±.10	10.00
E	±.20	12.00
E1	±.10	10.00
L	+.15 / –.10	.60
e	BASIC	.65
b	±.05	.30
q		0° - 7°
ddd	MAX.	.13
ccc	MAX.	.10
Package Thickness		1.40



Recommended Operating Conditions

Parameter	Symbol	Min	Typ	Max	Units
Positive Power Supply	VCC	+15.25	+15.5	+15.75	V
Negative Power Supply	VEE	–4.75	–4.5	–4.25	V
Total Analog Supply	VCC – VEE	19.5	20.0	20.5	V
Comparator Output Supply	PECL	0	3.3	5.0	V
Junction Temperature	T_J	60		80	˚C
Thermnal Resistance of Package (Junction to Case)	θ_{JC}		14.1		˚C/W

Absolute Maximum Ratings

Parameter	Symbol	Min	Max	Units
VCC (relative to GND)	VCC	0	16.5	V
VEE (relative to GND)	VEE	–10	0	V
Total Power Supply	VCC – VEE		21.0	V
PECL (relative to GND)	PECL	–0.1	5.5	V
Digital Input Voltages	DHI(*), DVR_EN(*), LD_EN(*)	VEE	+7.0	V
Digital TTL Input Voltages	IPD_D, IPD_C, SUPERV	–2.5	6.0	V
Analog Input Voltages	CVA, CVB, DVH, DVL, VINP, LOAD	VEE	VCC	V
Analog DOUT Voltage (DRV_EN < DRV_EN*)	DOUT	VEE + 2.0	VCC – 1.5	V
Analog Input Currents	ISC_IN, ISK_IN RADJ, FADJ BIAS	–0.125 0 0	2.25 1.45 1.45	mA mA mA
Digital Output Currents	QA/QA*; QB/QB*	0	50	mA
Static Driver Output Current	Iout	–40	+40	mA
Driver Swing	DVH – DVL	–0.5	13	V
Differential Comparator Voltage (SUPERV = 0 and IPD_C = 0)	VINP – CVA(B)	–13	+9	V
Differential Comparator Voltage (SUPERV = 1 or IPD_C = 1)	VINP – CVA(B)	–15	+15	V
Load Input Voltage	LOAD – VCM_IN_A(B)	–13	+13	V
Commutating Voltage Breakdown Limit	VCM_IN_A(B)	VCC – 16.25	VCC	V
Storage Temperature	TS	–65	+150	˚C
Junction Temperature (Note 1)	TJ		+125	˚C
Soldering Temperature (5 seconds, .25" from the pin)	TSOL		+260	˚C

Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only, and functional operation of the device at these, or any other conditions beyond those listed, is not implied. Exposure to absolute maximum conditions for extended periods may affect device reliability.

Note 1: This device does not contain internal thermal limiting; external cooling is required.

DC Characteristics

Power Supply Consumption

Parameter	Symbol	Min	Typ	Max	Units
Load + Comparator + Driver (Quiescent)					
Positive Supply	ICC		155	175	mA
Negative Supply	IEE	–190	–175		mA
PECL (Quiescent)	IPECL		25	30	mA
Quiescent Power Dissipation (per chip)	Pdiss		3.2		W

DC test conditions (unless otherwise specified): Over the full "Recommended Operating Conditions".

DC Characteristics *(continued)*

Driver Circuit

Parameter	Symbol	Min	Typ	Max	Units
Analog Input Voltages					
Driver Level Input Voltages					
DVH "High Level" Input Voltage Level	VDVH	VEE + 4.0		VCC – 3.5	V
DVL "Low Level" Input Voltage Level	VDVL	VEE + 3.5		VCC – 4.5	V
DVH "Super Voltage" Input Voltage Level	VDVHH	VEE + 4.0		VCC – 1.75	V
DVL "Super Voltage" Input Voltage Level	VDVLH	VEE + 3.5		VCC – 1.75	V
Differential Input Voltage Range	VDVH – VDVL	0		9	V
Analog Input Currents					
DVH, DVL Input Current	IDVH, IDVL	–50		50	µA
RADJ, FADJ Input Current	IRADJ, IFADJ	0.4		1.25	mA
BIAS Input Current	IBIAS	0.5		1.25	mA
Compliance Voltage Range for IRADJ, IFADJ, IBIAS ≤ 1.25 mA	VRADJ, VFADJ, VBIAS	0		3.0	V
Driver Output Characteristics					
DC Static Output Current (Non-Super Voltage)	I_{OUT}	–35		35	mA
DC Dynamic Output Current (Non-Super Voltage)	I_{OUT} Dynamic		±90		mA
DC Output Current (Super Voltage)	SV_{IOUT}	0		6	mA
Output Impedance (@ ±35 mA)	R_{OUT}	0.5	1.3	3.5	Ω
DOUT Leakage					
HiZ Mode (–8V ≤DOUT – CVA(B) ≤ 8V)	I_LEAK	–1		1	µA
@ (VEE + 3.5) < DOUT < 12V					
IPD Mode (VEE + 3.5 ≤ CVA(B) ≤ 8V, IPDD = IPDC = 1)					
@ (VEE + 3.5V) ≤ DOUT < 0V	I_LEAK	–300		300	nA
@ 0V ≤DOUT ≤+8V	I_LEAK	–15		15	nA
@ 8V < DOUT ≤ 12V	I_LEAK	–30		30	nA
@ 12V < DOUT ≤ 13V	I_LEAK	–100		100	nA
Driver DC Accuracy					
Driver High (DVH Range: VEE + 4.0V to VCC – 3.5V)					
Offset Voltage (DVH = 0V)	VDVH – VDOUT	–125		125	mV
Gain	VDOUT/VDVH	0.98		1	V/V
Linearity	DVHINL				
DVH = VEE + 4.0V TO VCC – 3.5V		–20		20	mV
DVH = –0.25V TO 10V		–10		10	mV
Super Voltage Offset (DVH = VCC – 1.75V)	VDVHH – VDOUT			750	mV
Offset Voltage Temperature Coefficient	ΔVDOUT / ΔT		0.25		mV/°C
Driver Low (DVL Range: VEE + 3.5V to VCC – 4.5V)					
Offset Voltage (DVL = 0V)	DVL – VDOUT	–125		125	mV
Gain	VDOUT/VDVL	0.98		1	V/V
Linearity	DVLINL				
DVL = VEE + 3.5V to VCC – 4.5V		–20		20	mV
DVL = –0.75V to 10V		–10		10	mV
Super Voltage Offset (DVL = VCC – 1.75V)	VDVLH – VDOUT			2000	mV
Offset Voltage Temperature Coefficient	ΔVDOUT / ΔT		0.25		mV°C
Digital Input Voltages					
DHI(*), DVR_EN(*) Input Voltage Range	$V_{FLEXINPUT}$	VEE + 2.75		5	V
Differential Input Swing	Input – Input*	±0.25		±4.0	V
IPD_D, SUPERV Input Low Voltage	VIL			0.5	V
IPD_D, SUPERV Input High Voltage	VIH	2.0			V
Digital Input Current DHI(*), DVR_EN(*), IPD_D					
DHI(*), DVR_EN(*)	$I_{FLEXINPUT}$	–350		350	µA
IPD_D, SUPERV	I_{IPD_D}	–100		100	µA

DC test conditions (unless otherwise specified): Over the full “Recommended Operating Conditions".

DC Characteristics *(continued)*

Comparator Circuit

Parameter	Symbol	Min	Typ	Max	Units
Analog Input Voltages					
Comparator Input Voltage Range	VINP	VEE + 3.5		VCC – 3.5	V
Comparator Threshold Voltage Range	CVA, CVB	VEE + 3.5		VCC – 3.5	V
Differential Comparator Voltage Range	VINP – CVA(B)	–8		8	V
Analog Input Currents					
Threshold Input Current					
VINP Input Current	I_CVA(B)	–50		50	µA
Normal Mode					
(IPD_D = IPD_C = 0, SUPERV = 0)					
@ (VEE + 3.5) ≤ VINP < 12V	IVINP	–3		3	µA
IPD Mode					
(IPD_D = IPD_C = 1 or SUPERV = 1,					
VEE + 3.5 ≤ CVA(B) ≤ +8V)					
@ (VEE + 3.5) ≤ VINP < 0V	IVINP	–100		100	nA
@ 0V ≤ VINP ≤ 8V	IVINP	–25		25	nA
@ 8V < VINP ≤ 12V	IVINP	–50		50	nA
@ 12V < VINP ≤ 13V	IVINP	–50		50	nA
DC Accuracy					
Comparator Hysteresis	V(hys)		10		mV
Comparator Offset	Vos	–20		20	mV
Comparator Offset Temperature Coefficient	ΔVos / ΔT		0.04		mV/°C
VINP Input Impedance (Note 1)	R_{IN}	2			MΩ
Digital Input Voltage					
IPD_C Input Low Voltage	VIL			0.5	V
IPD_C Input High Voltage	VIH	2.0			V
Digital Input Current	I_IPD_C	–100		100	µA
IPD_C Input Current Range					
Digital Output Voltage					
Differential Output Swing	|VQA–VQA*|, |VQB–VQB*|	400			mV
Output Common Mode Range	|VQA+VQA*|/2, |VQB+VQB*|/2	PECL – 1.5		PECL – 1.2	V

DC test conditions (unless otherwise specified): Over the full “Recommended Operating Conditions".

DC Characteristics *(continued)*

Load Circuit

Parameter	Symbol	Min	Typ	Max	Units
Programmable Load Analog Inputs					
Current Programming Inputs (ISC_IN, ISK_IN)					
Input Compliance Voltage Range	VISC_IN, VISK_IN	–0.1		2.5	V
Input Current Range	IISC_IN, IISK_IN	0		1.93	mA
Commutating Buffer Input (VCM_IN)					
Commutating Buffer Input Voltage Range	VVCM_IN_A(B)	VCC – 16		VCC – 7.5	V
Commutating Buffer Input Current Range	IVCM_IN_A(B)	–100		100	µA
Auxilliary Current Source Inputs					
BRIDGE_SC, BRIDGE_SK Input Resistance	Rin		1		kΩ
Programmable Load Digital Inputs					
LOAD Enable Inputs (LD_EN(*))					
Digital Input Voltage Range	VLD_EN(*)	VEE + 2.75		5	V
Differential Input Swing	VLD_EN – VLD_EN*	±0.25		±4.0	V
Digital Input Current	ILDEN(*)	–350		350	µA
Programmable Load Output					
LOAD Output Voltage Range	VLOAD	VEE + 3.5		VCC – 3.5	V
LOAD Output Current Range	ILOAD	–35		35	mA
Differential Load Voltage	VLOAD – VCM_IN	–11		11	V
LOAD Output Impedance	Zout	5		8	Ω
On-Chip Current Source Leakage					
Load Circuit Enabled (–8V ≤ LOAD – CVA(B) ≤ 8V, ISK_IN = ISC_IN = 0 mA)	ILOAD	–300		300	nA
HiZ Mode (IPD_D = IPD_C = 0, SUPERV = 0, LD_EN < LD_EN*, –8V ≤ LOAD – CVA(B) ≤ 8V) @ VEE + 3.5 ≤ LOAD ≤ 12V	ILOAD	–1		1	µA
IPD Mode (IPD_C = 1 or SUPERV = 1, IPD_D = 1, LD_EN < LD_EN*, VEE + 3.5 ≤ CVA(B) ≤ 8V)					
@ VEE + 3.5 < LOAD < 0V	ILOAD	–250		250	nA
@ 0V ≤ LOAD ≤ 8V	ILOAD	–15		15	nA
@ 8V < LOAD < 12V	ILOAD	–30		30	nA
@ 12V < LOAD ≤ 13V	ILOAD	–100		100	nA

DC test conditions (unless otherwise specified): Over the full “Recommended Operating Conditions".

DC Characteristics *(continued)*

Load Circuit (continued)

Parameter		Symbol	Min	Typ	Max	Units
Programmable Load Current Accuracy						
Source/Sink Current Offset		Ios	1		14	µA
Source/Sink Current Gain		Ai	18		22	mA/mA
Source/Sink Current Linearity Error						
ISC_IN, ISK_IN						
Calibration Points	*Test Point*	Actual–Programmed				
15 µA, 30 µA	22.5 µA		–5		5	µA
30 µA, 130 µA	80 µA		–15		15	µA
130 µA, 500 µA	315 µA		–50		50	µA
500 µA, 750 µA	625 µA		–50		50	µA
750 µA, 1 mA	875 µA		–50		50	µA
1 mA, 1.2 mA	1.1 mA		–50		50	µA
1.2 mA, 1.4 mA	1.3 mA		–50		50	µA
1.4 mA, 1.6 mA	1.5 mA		–50		50	µA
1.6 mA, 1.93 mA	1.7 mA		–100		100	µa
TempCo of Load Current		ΔILOAD / ΔT		±(0.1%+1)		µA/˚C
Commutating Voltage Accuracy						
Commutating Buffer Offset Voltage @ VCM_IN = 0V)		VOS	–100		100	mV
TempCo of Buffer Output Voltage		ΔVCMOUT_A(B) / ΔT		0.02		mV/˚C

Driver + Comparator + Load Combined Leakage – IPD Mode
(IPD_D = 1, IPD_C = 1 or SUPERV = 1, DRV_EN < DRV_EN*, LD_EN < LD_EN*,
VEE + 3.5 ≤ CVA(B) ≤ +8V)

Parameter	Symbol	Min	Typ	Max	Units
Leakage Current					
@ VEE + 3.5 ≤ DOUT + VINP + LOAD < 0V	ILEAK	–450		450	nA
@ 0V ≤ DOUT + VINP + LOAD ≤ 8V	ILEAK	–30		30	nA
@ 8V < DOUT + VINP + LOAD ≤ 12V	ILEAK	–50		50	nA
@ 12V < DOUT + VINP + LOAD ≤ 13V	ILEAK	–300		300	nA

DC conditions (unless otherwise specified): Over the full "Recommended Operating Conditions".

Note 1: Not production tested. Guaranteed by design and characterization.

AC Characteristics

Driver Circuit

Parameter	Symbol	Min	Typ	Max	Units
Driver Propagation Delay					
Data to Output	Tpd		1.5	3.0	ns
Enable to HiZ (Note 2)	Tpd		1.5	3.0	ns
Enable to Output Active (Note 2)	Tpd		1.5	3.0	ns
Propagation Delay to TEMPCO (Note 1)	ΔTPD/ΔT		1.0		ps/˚C
Driver Rise/Fall Times (Note 1)					
800 mV (20% - 80%)	Tr/Tf		800	1000	ps
3V (10% - 90%)	Tr/Tf		1.2	1.3	ns
5V (10% - 90%)	Tr/Tf		2.0	2.1	ns
Driver Rise/Fall Time Variation (Note 1)	|Tr – Tf|		±50		ps
Fmax (10% Amplitude Reduction) (Note 1)					
800 mV	Fmax	500			MHz
3V	Fmax	350			MHz
5V	Fmax	150			MHz
Driver Minimum Pulse Width (10% Amplitude Reduction) (Note 1)					
800 mV			1		ns
3V			2		ns
5V			3		ns
Driver Output Capacitance (Note 1)	Cout		2		pF

Comparator Circuit

Parameter	Symbol	Min	Typ	Max	Units
Comparator Propagation Delay	Tpd		1.5	3.0	ns
TempCo of Propagation Delay (Note 1)	ΔTpd / ΔT		7.0		ps/˚C
Comparator Input Slew Rate Tracking (Note 1)	SRT	4.0			V/ns
Comparator Input Capacitance (Note 1)	Cin		2.0		pF
Digital Output Rise and Fall Times (20% - 80%) (Note 1)	Tr, Tf		500		ps
Comparator Minimum Pulse Width (Note 1)	MPW	1.2			ns

AC test conditions (unless otherwise specified): "Recommended Operating Conditions". IRADJ = IFADJ = 1.1 mA. IBIAS = 0.8 mA, VINP terminated with 50Ω to GND, QA(*), QB(*) terminated with 50Ω to PECL –2V, ISC_IN - ISK_IN = 1.93 mA.

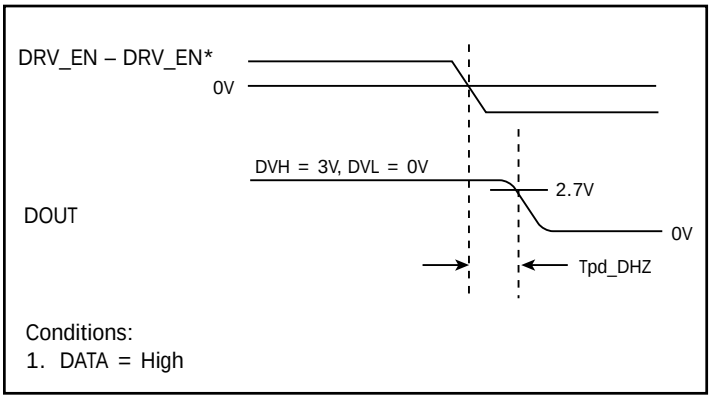
AC Characteristics *(continued)*

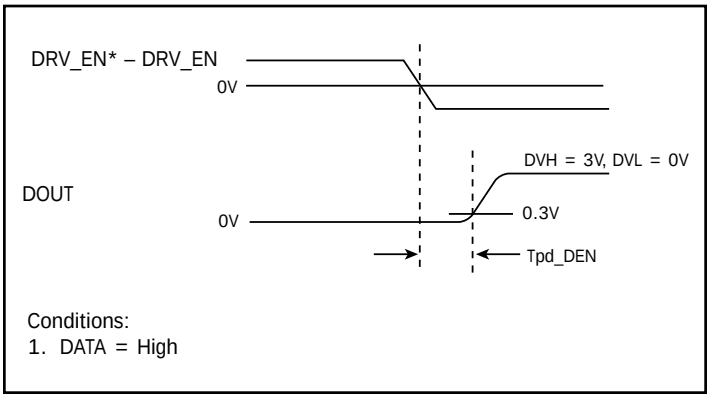
Load Circuit

Parameter	Symbol	Min	Typ	Max	Units
Load Propagation Delay (Note 3)					
Inhibit to Iout	Tpd_on		3.8	5.0	ns
Iout to Inhibit	Tpd_off		3.8	6.0	ns
Load Output Capacitance (Note 1)					
Load Active	Cout		3.5		pF
Load Off	Cout		2.0		pF

AC test conditions (unless otherwise specified): "Recommended Operating Conditions". IRADJ = IFADJ = 1.1 mA. IBIAS = 0.8 mA, VINP terminated with 50Ω to GND, QA(*), QB(*) terminated with 50Ω to PECL –2V, ISC_IN - ISK_IN = 1.93 mA.

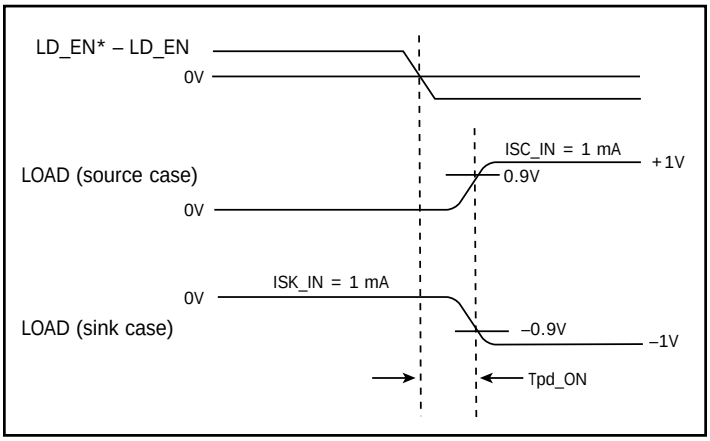
Note 1: Not production tested. Guaranteed by design and characterization.
Note 2: Driver Enable/Disable Tpd is depicted below:

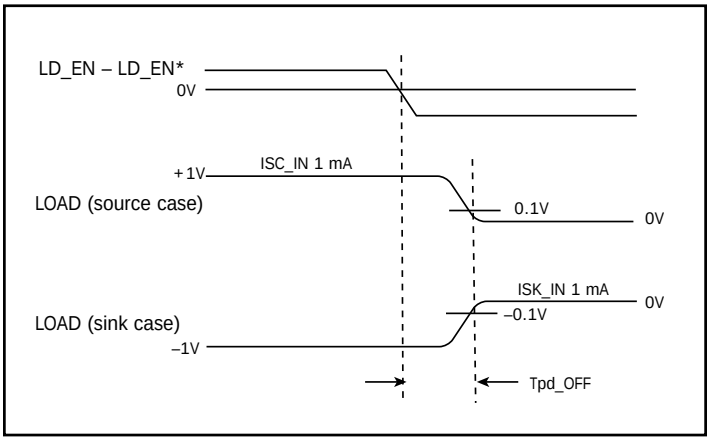




Driver Enable/Disable Tpd

Note 3: Load propagation delay is defined below:





Load Propagation Delay

Ordering Information

Model Number	Package
E720BXF	52 Lead Exposed Pad QFP (5 x 5 mm heat slug)
EVM720BXF	Edge720 Evaluation Board

Contact Information

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Revision History

Current Revision Date: September 24, 2002
Previous Revision Date: July 25, 2002

Page #	Section Name	Previous Revision	Current Revision
all			Remove "Preliminary" Status changed from "Preliminary" to "Final"
6	Driver Stability/Compenstaion		*Add:* 2nd paragraph
9	Comparator Analog Inputs		*Add:* 2 sentences to end of 1st paragraph.
10	Comparator Power Supplies		*Add:* 2nd paragraph
12	Commutating Voltage Compensation	The VCM_CAP pin is an internal commutating buffer compensation pin that requires a fixed ...	The VCM_CAP_A(B) pins are internal commutating buffer compensation pins that require a fixed ...
12	Standard Active Load Configuration		*Add:* 1 sentences to end of paragraph 1.
12	Programmable Clamp Configuration		*Add:* 1 sentences to end of paragraph 1.
14	Connectivity	... Edge720 DCL is shown in Figure 22.	... Edge720 DCL is shown in Figure 24.
15	Application Information		*Add:* Driver/Comparator/Load Output Circuit Section *Add:* Power Supply Bypassing Section
16	Figure 24	Quad Channel Device	64-Channel Device
17	Application Information		Update figure, add notes.
23	DC Characteristics	DOUT Leakage (-8V ≤ DOUT – CVA(B) ≤ 8V) HiZ Mode	DOUT Leakage HiZ Mode (-8V ≤ DOUT – CVA(B) ≤ 8V)
25	DC Characteristics	On-Chip Current Source Leakage	All Parameters rewritten

Revision History

Current Revision Date: July 25, 2002
Previous Revision Date: April 24, 2002

Page #	Section Name	Previous Revision	Current Revision
1	Description	2nd para: In addition, 13.75V super voltage ...	2nd para: In addition, 13V super voltage ...
1	Features	+13.75V Super Voltage Capable	+13V Super Voltage Capable
5	Introduction	... super voltage level of up to 13.75V ...	... super voltage level of up to 13V ...
6	Super Voltage Operation	... super voltage level of up to 13.75V ...	... super voltage level of up to 13V ...
8	Circuit Description	1st para, 2nd sentence: ... output voltage at DOUT = 0V.	... output voltage when the input is programmed to 0V.
16	Apps Information		*Add:* VCM_OUT_A(B) to figure
17	Package Information		Update drawings
18	Recommended Operation Conditions	Junction Temperature, Min: 50	Junction Temperature, Min: 60
21	Power Supply Consumption	Negative Supply, Min: –210	Negative Supply, Min: –190
22	Driver Circuit	Output Impedance (@ ±25 mA), Typ: 2, Max: 4.5 Linearity IPD_D DOUT Range Super Voltage Offset (DOUT = VCC – 2.5), Max: 500	Output Impedance (@ ±35 mA), Typ: 1.3, Max: 3.5 Break into DOUT Ranges IPD_D/SUPERV Change to "DVH = " Super Voltage Offset (DVH = VCC – 1.75V), Max: 750
23	Comparator Circuit	IPD_C = 0, SUPERV = 0 IPD_C = 1 or SUPERV = 1 Output Common Mode Range, Max: PECL –1.1	IPD_D = IPD_C = 0, SUPERV = 0 IPD_D = IPD_C = 1 or SUPERV = 1 Output Common Mode Range, Max: PECL –1.2
24	Load Circuit	Sym: VVCM_IN, IVCM_IN HiZ Mode (IPD_C = 0, ... IPD Mode (IPD_C = 1 or SUPERV = 1, LD_EN < LD_EN*	VVCM_IN_A(B), IVCM_IN_A(B) HiZ Mode (IPD_D = IPD_C = 0, ... IPD Mode (IPD_C = 1 or SUPERV = 1, IPD_D = 1, LD_EN < LD_EN*
25	Load Circuit		Update Source/Sink Current Linearity Error specs

Current Revision Date: April 24, 2002
Previous Revision Date: August 13, 2002

Page #	Section Name	Previous Revision	Current Revision
all	All Sections		All Sections Rewritten Status changed from "Target" to "Preliminary"