DS1645/DS3645, DS1675/DS3675

National Semiconductor

Memory Support

T-52-15

DS1645/DS3645, DS1675/DS3675 Hex TRI-STATE® TTL to MOS Latches/Drivers

General Description

The DS1645/DS3645 and DS1675/DS3675 are hex MOS latches/drivers with outputs designed to drive large capacitive loads up to 500 pF associated with MOS memory systems. PNP input transistors are used to reduce input currents, allowing the large fan-out to these drivers needed in memory systems. The circuit has Schottky-clamped transistor logic for minimum propagation delay, and TRI-STATE® outputs which allow bus operation.

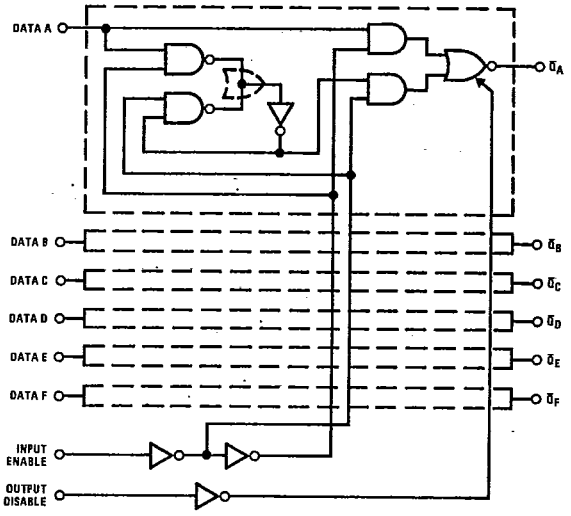
The DS1645/DS3645 has a 15 Ω resistor in series with the outputs to dampen transients caused by the fast switching output circuit. The DS1675/DS3675 has a direct, low impedance output for use with or without an external resistor.

The circuit employs a fall-through-latch which captures the data in parallel with the output, thereby eliminating the delay normally encountered in other latch circuits. The DS1645/DS3645 and DS1675/DS3675 may be used for input address lines or input/output data lines of a MOS memory system.

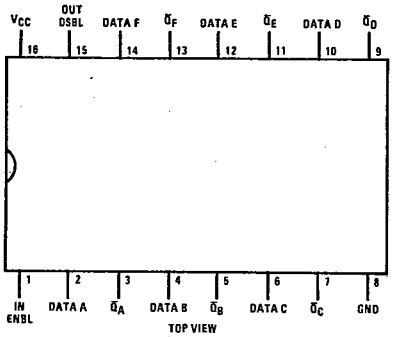
Features

- TTL compatible inputs
- PNP inputs minimize loading
- Capacitance-driving outputs
- TRI-STATE outputs
- Built-in damping resistor (DS1645/DS3645)

Logic and Connection Diagrams



Dual-In-Line Package



Order Number DS1645J, DS1675J, DS3645J, DS3675J, DS3645N or DS3675N
See NS Package J16A or N16A

Truth Table

INPUT ENABLE	OUTPUT DISABLE	DATA	OUTPUT	OPERATION
1	0	1	0	Data Feed-Through
1	0	0	1	Data Feed-Through
0	0	X	Q	Latched to Data Present when Enable Went Low
X	1	X	Hi-Z	High Impedance Output

X = Don't care
Hi-Z = TRI-STATE mode

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Absolute Maximum Ratings (Note 1)

Supply Voltage, V_{CC}	7V
Logical "1" Input Voltage	7V
Logical "0" Input Voltage	−1.5V
Storage Temperature Range	−65°C to +150°C
Maximum Power Dissipation* at 25°C	
Cavity Package	1433 mW
Molded Package	1362 mW
Lead Temperature (Soldering, 10 seconds)	300°C

*Derate cavity package 9.6 mW/°C above 25°C; derate molded package 10.9 mW/°C above 25°C.

Operating Conditions

	MIN	MAX	UNITS
Supply Voltage (V_{CC})	4.5	5.5	V
Temperature (T_A)			
DS1645, DS1675	−55	+125	°C
DS3645, DS3675	0	+70	°C

Electrical Characteristics (Notes 2 and 3)

	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
$V_{IN(1)}$	Logical "1" Input Voltage			2.0			V
$V_{IN(0)}$	Logical "0" Input Voltage					0.8	V
$I_{IN(1)}$	Logical "1" Input Current	V_{IN} = 5.5V, V_{CC} = 5.5V	Enable Inputs		0.1	40	μA
			Data Inputs		0.2	80	μA
$I_{IN(0)}$	Logical "0" Input Current	V_{IN} = 0.5V, V_{CC} = 5.5V	Enable Inputs		−50	−250	μA
			Data Inputs		−100	−500	μA
V_{CLAMP}	Input Clamp Voltage	V_{CC} = 4.5V, I_{IN} = −18 mA			−0.75	−1.2	V
V_{OH}	Logical "1" Output Voltage (No Load)	V_{CC} = 4.5V, I_{OH} = −10 μA	DS1645, DS1675	2.7	3.6		V
			DS3645, DS3675	2.8	3.6		V
V_{OL}	Logical "0" Output Voltage (No Load)	V_{CC} = 4.5V, I_{OL} = 10 μA	DS1645, DS1675		0.25	0.4	V
			DS3645, DS3675		0.25	0.35	V
V_{OH}	Logical "1" Output Voltage (With Load)	V_{CC} = 4.5V, I_{OH} = −1.0 mA	DS1645	2.4	3.5		V
			DS1675	2.5	3.5		V
			DS3645	2.6	3.5		V
			DS3675	2.7	3.5		V
V_{OL}	Logical "0" Output Voltage (With Load)	V_{CC} = 4.5V, I_{OL} = 20 mA	DS1645		0.6	1.1	V
			DS1675		0.4	0.5	V
			DS3645		0.6	1.0	V
			DS3675		0.4	0.5	V
I_{ID}	Logical "1" Drive Current	V_{CC} = 4.5V, V_{OUT} = 0V, (Note 4)			−250		mA
I_{OD}	Logical "0" Drive Current	V_{CC} = 4.5V, V_{OUT} = 4.5V, (Note 4)			150		mA
I_{HZ}	TRI-STATE Output Current	V_{OUT} = 0.4V to 2.4V, Output Disable = 2.0V		−40		40	μA
I_{CC}	Power Supply Current	V_{CC} = 5.5V	Output Disable = 3V, All Other Inputs = 0V		60	100	mA
			Input Enable = 3V, All Other Inputs = 0V		40	80	mA

Note 1: "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. Except for "Operating Temperature Range" they are not meant to imply that the devices should be operated at these limits. The table of "Electrical Characteristics" provides conditions for actual device operation.

Note 2: Unless otherwise specified min/max limits apply across the −55°C to +125°C temperature range for the DS1645 and DS1675 and across the 0°C to +70°C range for the DS3645 and DS3675. All typical values are for T_A = 25°C and V_{CC} = 5V.

Note 3: All currents into device pins shown as positive, out of device pins as negative, all voltages referenced to ground unless otherwise noted. All values shown as max or min on absolute value basis.

Note 4: When measuring output drive current and switching response for the DS1675 and DS3675 a 15 ohm resistor should be placed in series with each output. This resistor is internal to the DS1645/DS3645, and need not be added.

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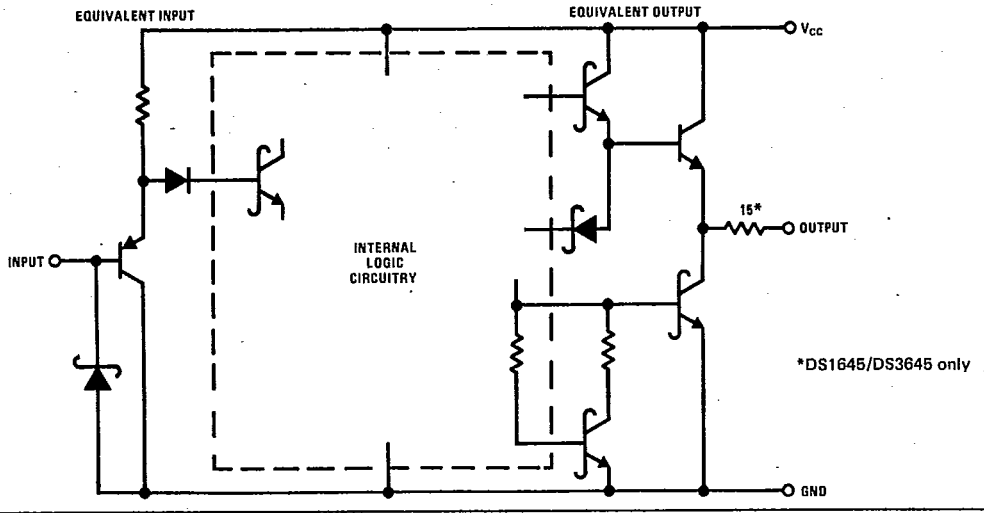
Switching Characteristics

V_{CC} = 5V, T_A = 25°C, unless otherwise noted. (Note 4)

PARAMETER		CONDITIONS		MIN	TYP	MAX	UNITS
t_{S+-}	Storage Delay Negative Edge	*(Figure 1)*	C_L = 50 pF		4.5	7	ns
			C_L = 500 pF		8	12	ns
t_{S-+}	Storage Delay Positive Edge	*(Figure 1)*	C_L = 50 pF		6	8	ns
			C_L = 500 pF		9	13	ns
t_F	Fall Time	*(Figure 1)*	C_L = 50 pF		5	8	ns
			C_L = 500 pF		21	35	ns
t_R	Rise Time	*(Figure 1)*	C_L = 50 pF		6	9	ns
			C_L = 500 pF		22	35	ns
t_{SET-UP}	Set-Up Time on Data Input Before Input Enables Goes Low			10	0		ns
t_{HOLD}	Hold Time on Data Input After Input Enable Goes Low			15	5		ns
t_W	Minimum Width of Enable Pulse to Latch Data			20	5		ns
t_{ZL}	Delay from Disable Input to Logical "0" Level (from High Impedance State)	C_L = 50 pF, R_L = 2 kΩ to V_{CC}, *(Figure 2)*			10	15	ns
t_{ZH}	Delay from Disable Input to Logical "1" Level (from High Impedance State)	C_L = 50 pF, R_L = 2 kΩ to Ground, *(Figure 2)*			10	15	ns
t_{LZ}	Delay from Disable Input to High Impedance State (from Logical "0" Level)	C_L = 50 pF, R_L = 400Ω to V_{CC}, *(Figure 3)*			16	25	ns
t_{HZ}	Delay from Disable Input to High Impedance State (from Logical "1" Level)	C_L = 50 pF, R_L = 400Ω to Ground, *(Figure 3)*			16	25	ns

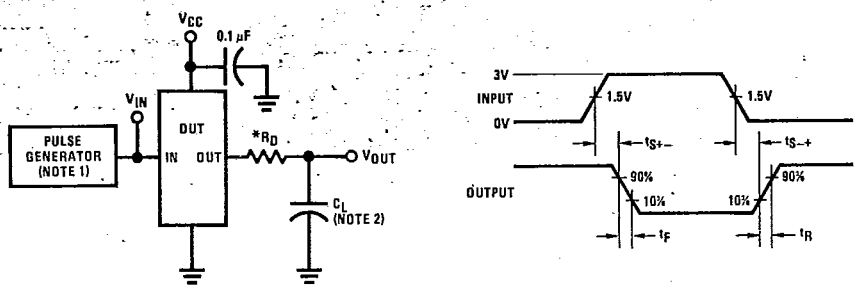
Schematic Diagram



*DS1645/DS3645 only

AC Test Circuits and Switching Time Waveforms

t_{S+-}, t_{S-+}, t_R, t_F

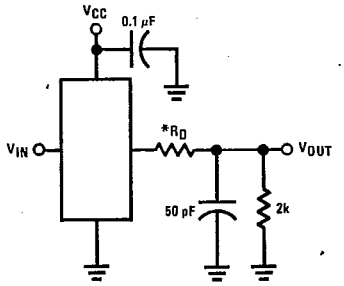


Note 1: The pulse generator has the following characteristics: Z_{OUT} = 50 Ω and PRR ≤ 1 MHz. Rise and fall times between 10% and 90% points ≤ 5 ns.

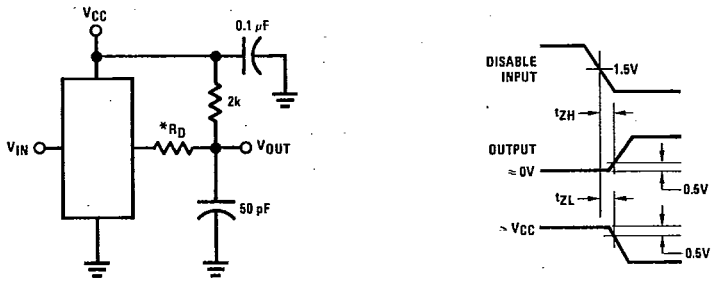
Note 2: C_L includes probe and jig capacitance.

FIGURE 1

t_{ZH}



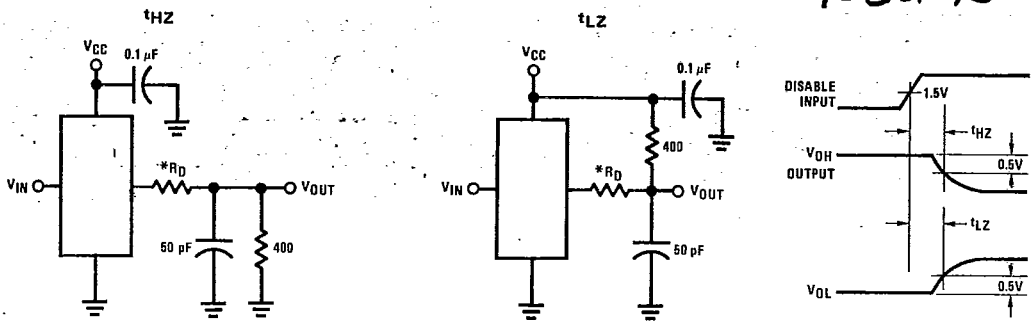
t_{ZL}



*Internal on DS1645 and DS3645

FIGURE 2

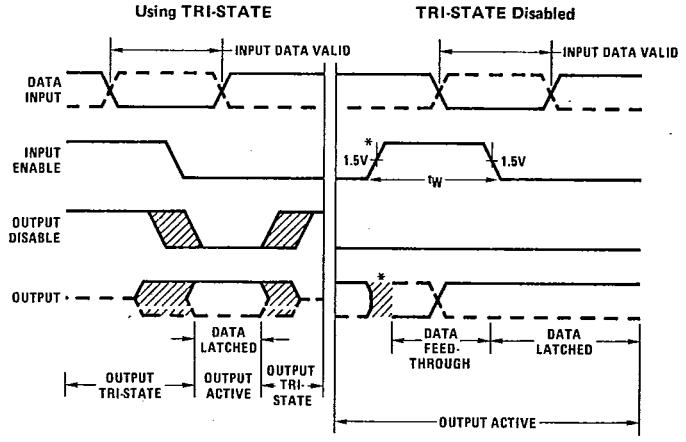
AC Test Circuits and Switching Time Waveforms (Continued)



*Internal on DS1645 and DS3645

FIGURE 3

Operating Waveforms



*When the Input Enable makes a positive transition the output will be indeterminate for a short duration. The positive transition of the Input Enable normally occurs during a don't-care timing state at the output.

Typical Applications

The DS3645 and DS3675 latch/driver has TRI-STATE outputs, which allows the outputs to be tied with those of another TRI-STATE driver, such as the DS3646 and DS3676 refresh counter. The DS3645 and DS3675 can be disabled while the alternate driver controls the address lines into the memory system.