DG300A/301A/302A/303A

CMOS Analog Switches

Features

- Analog Signal Range: ±15 V
- Fast Switching—t_{ON}: 150 ns
- Low On-Resistance—$r_{DS(on)}$: 30 Ω
- Single Supply Operation
- Latch-up Proof
- CMOS Compatible

Benefits

- Full Rail-to-Rail Analog Signal Range
- Low Signal Error
- Low Power Dissipation

Applications

- Low Level Switching Circuits
- Programmable Gain Amplifiers
- Portable and Battery Powered Systems

Description

The DG300A-DG303A family of monolithic CMOS switches feature three switch configuration options (SPST, SPDT, and DPST) for precision applications in communications, instrumentation and process control, where low leakage switching combined with low power consumption are required.

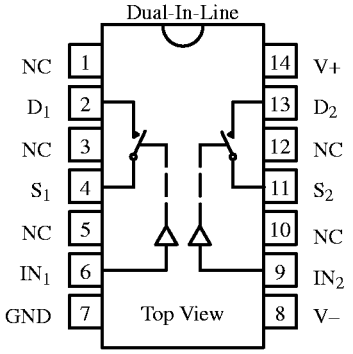
Designed on the Siliconix PLUS-40 CMOS process, these switches are latch-up proof, and are designed to block up to 30 V peak-to-peak when off. An epitaxial layer prevents latchup.

In the on condition the switches conduct equally well in both directions (with no offset voltage) and minimize error conditions with their low on-resistance.

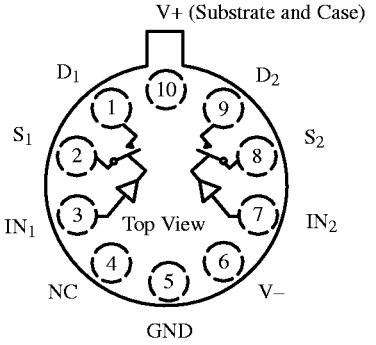
Featuring low power consumption (3.5 mW typ) these switches are ideal for battery powered applications, without sacrificing switching speed. Designed for break-before-make switching action, these devices are CMOS and quasi TTL compatible. Single supply operation is allowed by connecting the V– rail to 0 V.

Functional Block Diagram and Pin Configuration

DG300A
Dual-In-Line



DG300A
Metal Can



Truth Table

Logic	Switch
0	OFF
1	ON

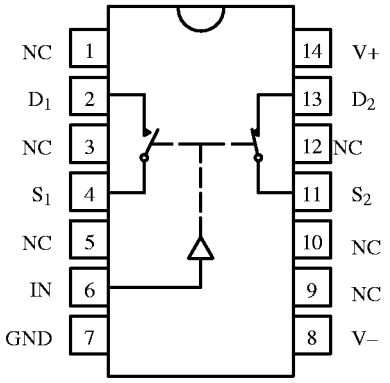
Logic "0" ≤ 0.8 V
Logic "1" ≥ 4 V

Updates to this data sheet may be obtained via facsimile by calling Siliconix FaxBack, 1-408-970-5600. Please request FaxBack document #70044.

Functional Block Diagram and Pin Configuration (Cont'd)

DG301A

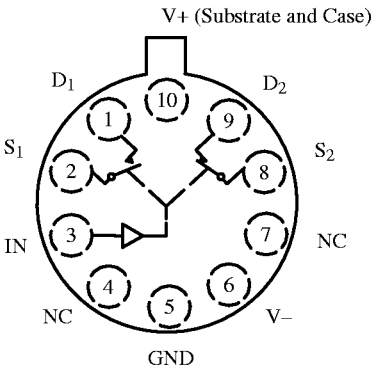
Dual-In-Line



Top View

DG301A

Metal Can



Top View

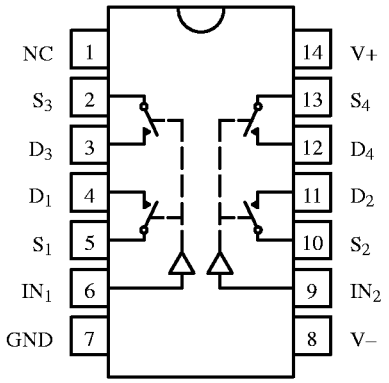
Truth Table

Logic	SW_1	SW_2
0	OFF	ON
1	ON	OFF

Logic "0" ≤ 0.8 V
Logic "1" ≥ 4 V

DG302A

Dual-In-Line



Top View

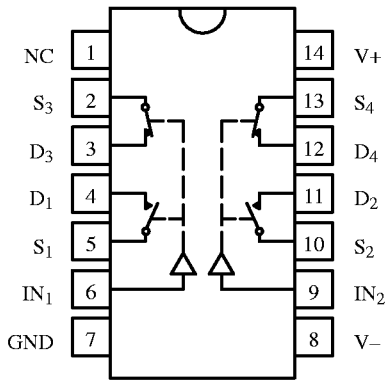
Truth Table

Logic	Switch
0	OFF
1	ON

Logic "0" ≤ 0.8 V
Logic "1" ≥ 4 V

DG303A

Dual-In-Line



Top View

Truth Table

Logic	SW_1, SW_2	SW_3, SW_4
0	OFF	ON
1	ON	OFF

Logic "0" ≤ 0.8 V
Logic "1" ≥ 4 V

Ordering Information

Temp Range	Package	Part Number
DG300A		
0 to 70°C	14-Pin Plastic DIP	DG300ACJ
–25 to 85°C	14-Pin CerDIP	DG300ABK
	10-Pin Metal Can	DG300ABA
–55 to 125°C	14-Pin CerDIP	DG300AAK
		DG300AAK/883
		JM38510/11601BCA
	14-Pin Sidebraze	JM38510/11601BCC
	10-Pin Metal Can	DG300AAA/883
		JM38510/11601BIA
DG301A		
0 to 70°C	14-Pin Plastic DIP	DG301ACJ
–25 to 85°C	14-Pin CerDIP	DG301ABK
	10-Pin Metal Can	DG301ABA
–55 to 125°C	14-Pin CerDIP	DG301AAK/883
		JM38510/11602BCA
	14-Pin Sidebraze	JM38510/11602BCC
	10-Pin Metal Can	DG301AAA
		DG301AAA/883
		JM38510/11602BIA
DG302A		
0 to 70°C	14-Pin Plastic DIP	DG302ACJ
–55 to 125°C	14-Pin CerDIP	DG302AAK
		DG302AAK/883
		JM38510/11603BCA
	14-Pin Sidebraze	JM38510/11603BCC
DG303A		
0 to 70°C	14-Pin Plastic DIP	DG303ACJ
–25 to 85°C	14-Pin CerDIP	DG303ABK
–45 to 85°C	14-SOIC	DG303ADY
–55 to 125°C	14-Pin CerDIP	DG303AAK
		DG303AAK/883
		JM38510/11604BCA
	14-Pin Sidebraze	JM38510/11604BCC

Absolute Maximum Ratings

Voltages Referenced to V–

V+ . . . . . 44 V

GND . . . . . 25 V

Digital Inputs[a], V_S, V_D . . . . . (V–) –2 V to (V+) +2V or 30 mA, whichever occurs first

Current, Any Terminal . . . . . 30 mA

Continuous Current, S or D
(Pulsed at 1 ms, 10% duty cycle max) . . . . . 100 mA

Storage Temperature (A & B Suffix) . . . . . –65 to 150°C
(C Suffix) . . . . . –65 to 125°C

Power Dissipationb

14-Pin Plastic DIP[c] . . . . . 470 mW

14-Pin CerDIP[d] . . . . . 825 mW

10-Pin Metal Can[e] . . . . . 450 mW

Notes:

a. Signals on S_X, D_X, or IN_X exceeding V+ or V– will be clamped by internal diodes. Limit forward diode current to maximum current ratings.
b. All leads welded or soldered to PC Board.
c. Derate 6.5 mW/°C above 25°C
d. Derate 11 mW/°C above 75°C
e. Derate 6 mW/°C above 75°C

Schematic Diagram (Typical Channel)

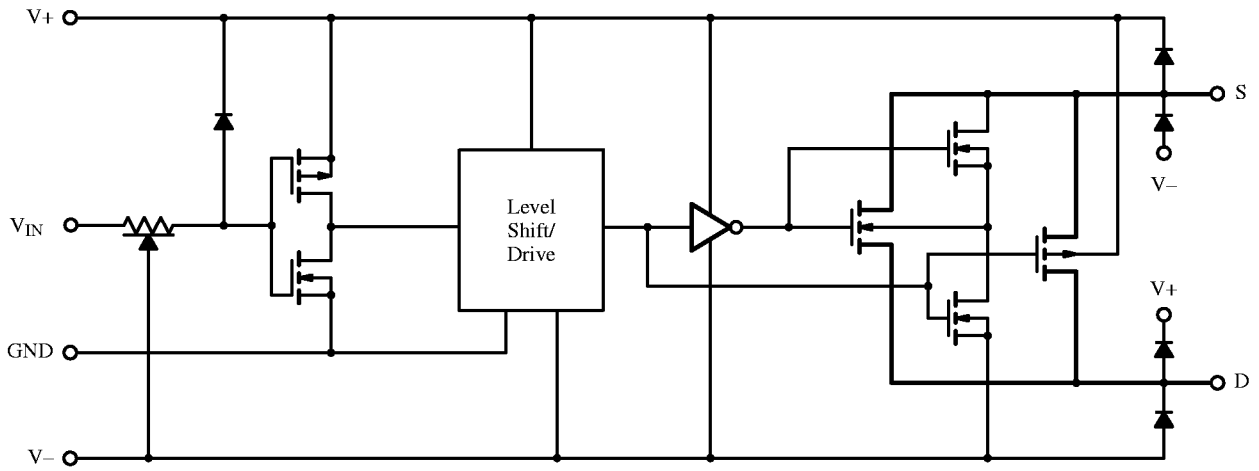


Figure 1.

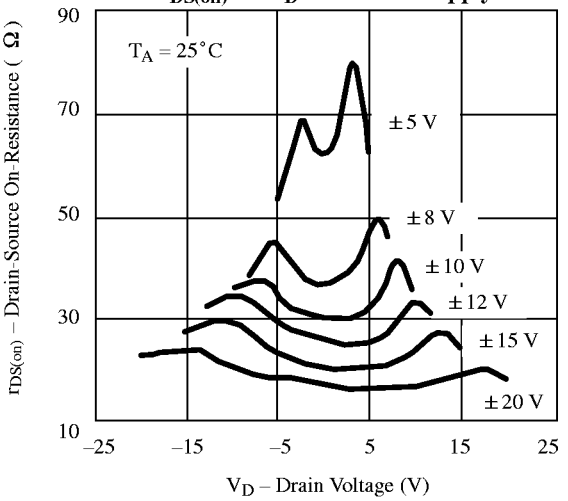
Specifications[a]

Parameter	Symbol	Conditions Unless Otherwise Specified V+ = 15 V, V– = –15 V V_{IN} = 0.8 V or V_{IN} = 4 V[f]	Temp[b]	Typ[c]	A Suffix –55 to 125°C Min[d]	A Suffix –55 to 125°C Max[d]	B. C Suffix Min[d]	B. C Suffix Max[d]	Unit
Analog Switch									
Analog Signal Range[e]	V_{ANALOG}		Full		–15	15	–15	15	V
Drain-Source On-Resistance	$r_{DS(on)}$	V_D = ±10 V, I_S = –10 mA	Room Full	30		50 75		50 75	Ω
Source Off Leakage Current	$I_{S(off)}$	V_S = ±14 V, V_D = ∓14 V	Room Hot	±0.1	–1 –100	1 100	–5 –100	5 100	nA
Drain Off Leakage Current	$I_{D(off)}$	V_S = ±14 V, V_D = ∓14 V	Room Hot	±0.1	–1 –100	1 100	–5 –100	5 100	nA
Drain On Leakage Current	$I_{D(on)}$	V_D = V_S = ±14 V	Room Hot	±0.1	–1 –100	1 100	–5 –100	5 100	nA
Digital Control									
Input Current with Input Voltage High	I_{INH}	V_{IN} = 5 V	Room Full	–0.001	–1 –1		–1		µA
		V_{IN} = 15 V	Room Full	0.001		1 1		1	µA
Input Current with Input Voltage Low	I_{INL}	V_{IN} = 0 V	Room Full	–0.001	–1 –1		–1		µA
Dynamic Characteristics									
Turn-On Time	t_{ON}	See Figure 2	Room	150		300			ns
Turn-Off Time	t_{OFF}	See Figure 2	Room	130		250			ns
Break-Before-Make Time	t_{OPEN}	DG301A/303A Only Figure 3	Room	50					ns
Charge Injection	Q	C_L = 1 nF, R_{gen} = 0 Ω V_{gen} = 0 V, Figure 4	Room	8					pC
Source-Off Capacitance	$C_{S(off)}$	V_S, V_D = 0 V, f = 1 MHz	Room	14					pF
Drain-Off Capacitance	$C_{D(off)}$	V_S, V_D = 0 V, f = 1 MHz	Room	14					pF
Channel-On Capacitance	$C_{D(on)}$	V_S, V_D = 0 V, f = 1 MHz	Room	40					pF
Input Capacitance	C_{in}	f = 1 MHz, V_{IN} = 0 V	Room	6					pF
		f = 1 MHz, V_{IN} = 15 V	Room	7					pF
Off-Isolation	OIRR	V_{IN} = 0 V, R_L = 1 kΩ V_S = 1 V_{rms}, f = 500 kHz	Room	62					dB
Crosstalk (Channel-to-Channel)	X_{TALK}	V_{IN} = 0 V, R_L = 1 kΩ V_S = 1 V_{rms}, f = 500 kHz	Room	74					dB
Power Supplies									
Positive Supply Current	I+	V_{IN} = 4 V (One Input) All Others = 0 V	Room Full	0.23		0.5 1		1	mA
Negative Supply Current	I–	V_{IN} = 4 V (One Input) All Others = 0 V	Room Full	–0.001	–10 –100		–100		µA
Positive Supply Current	I+	V_{IN} = 0.8 V (All Inputs)	Room Full	0.001		10 100		100	µA
Negative Supply Current	I–	V_{IN} = 0.8 V (All Inputs)	Room Full	–0.001	–10 –100		–100		µA

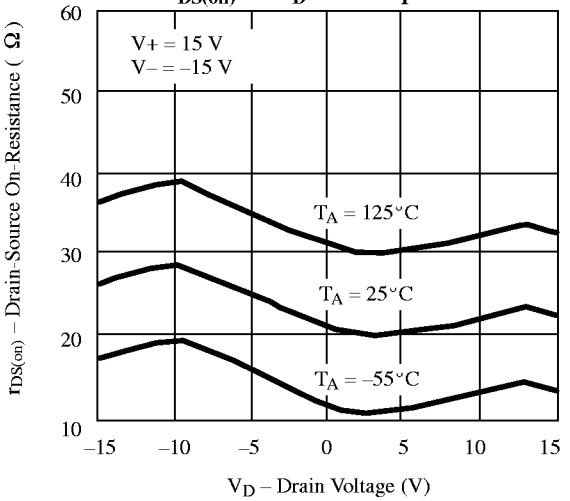
Notes:
a. Refer to PROCESS OPTION FLOWCHART.
b. Room = 25°C, Full = as determined by the operating temperature suffix.
c. Typical values are for DESIGN AID ONLY, not guaranteed nor subject to production testing.
d. The algebraic convention whereby the most negative value is a minimum and the most positive a maximum, is used in this data sheet.
e. Guaranteed by design, not subject to production test.
f. V_{IN} = input voltage to perform proper function.

Typical Characteristics

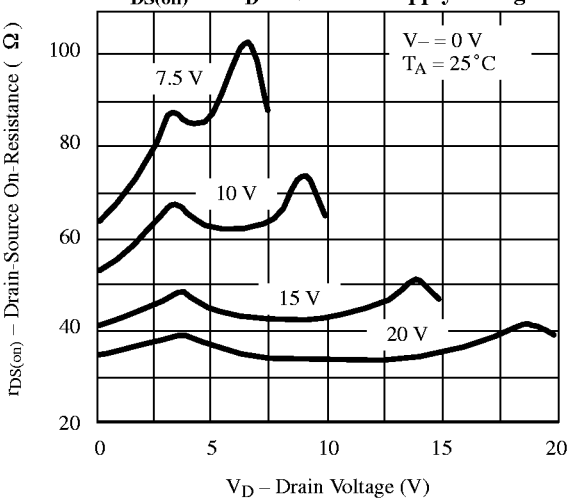
$r_{DS(on)}$ vs. V_D and Power Supply



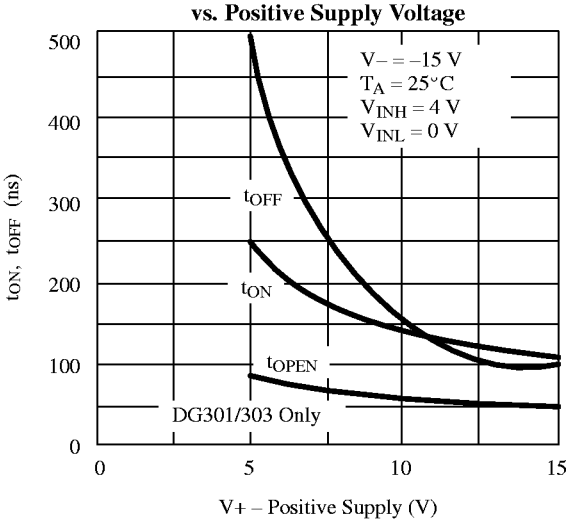
$r_{DS(on)}$ vs. V_D and Temperature



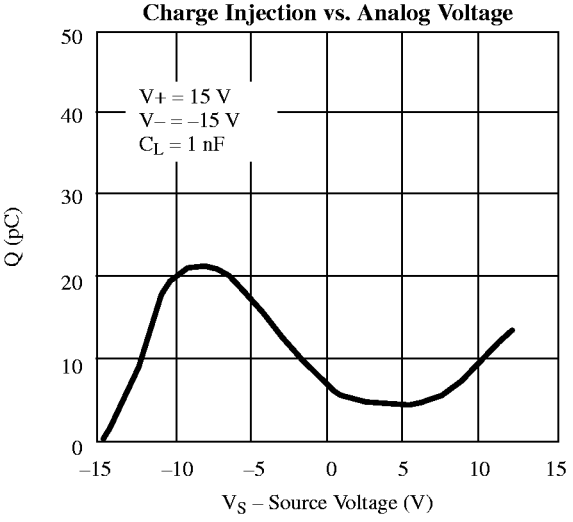
$r_{DS(on)}$ vs. V_D and Power Supply Voltage



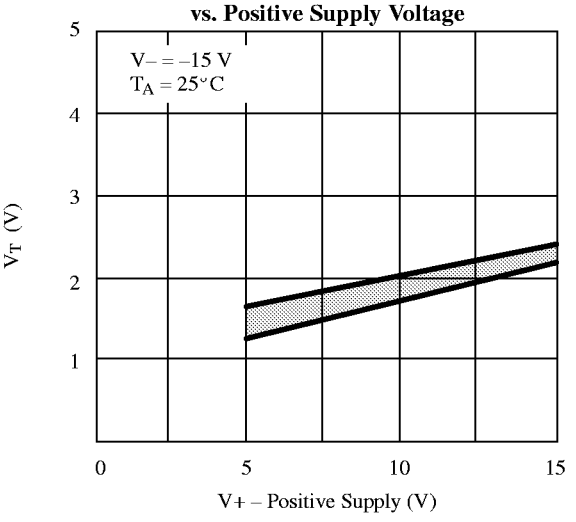
Switching Time and Break-Before-Make Time vs. Positive Supply Voltage



Charge Injection vs. Analog Voltage

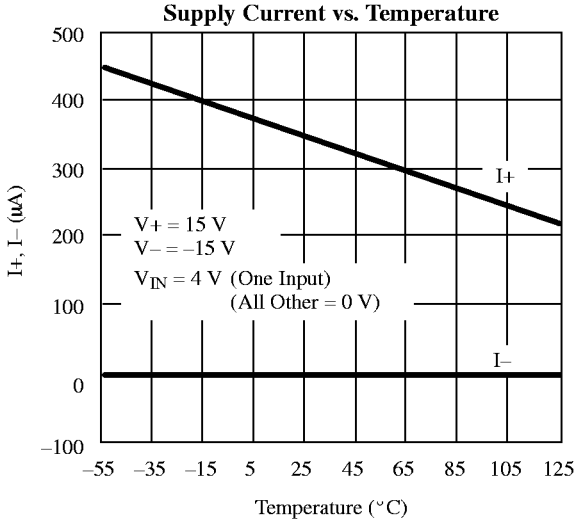


Input Switching Threshold vs. Positive Supply Voltage

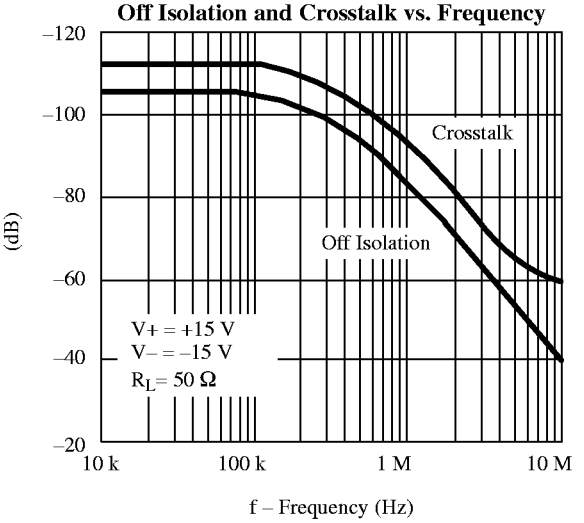


Typical Characteristics (Cont'd)

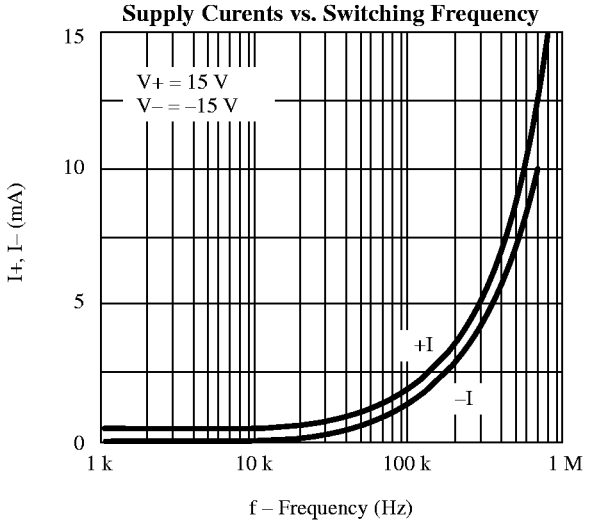
Supply Current vs. Temperature



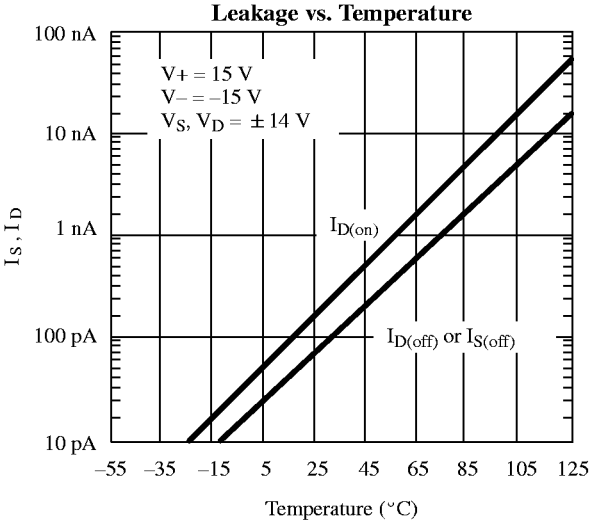
Off Isolation and Crosstalk vs. Frequency



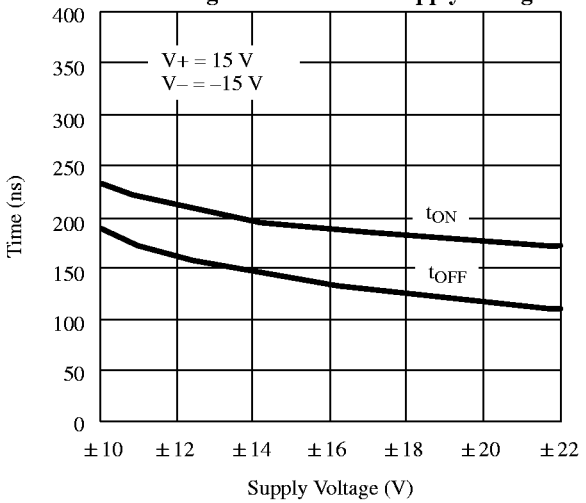
Supply Curents vs. Switching Frequency



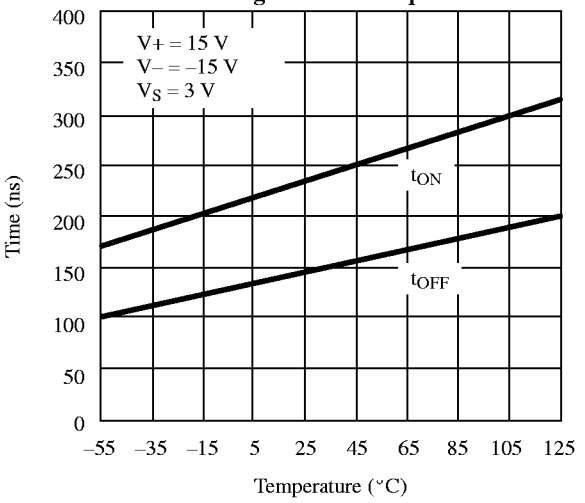
Leakage vs. Temperature



Switching Time vs. Power Supply Voltage



Switching Time vs. Temperature



Test Circuits

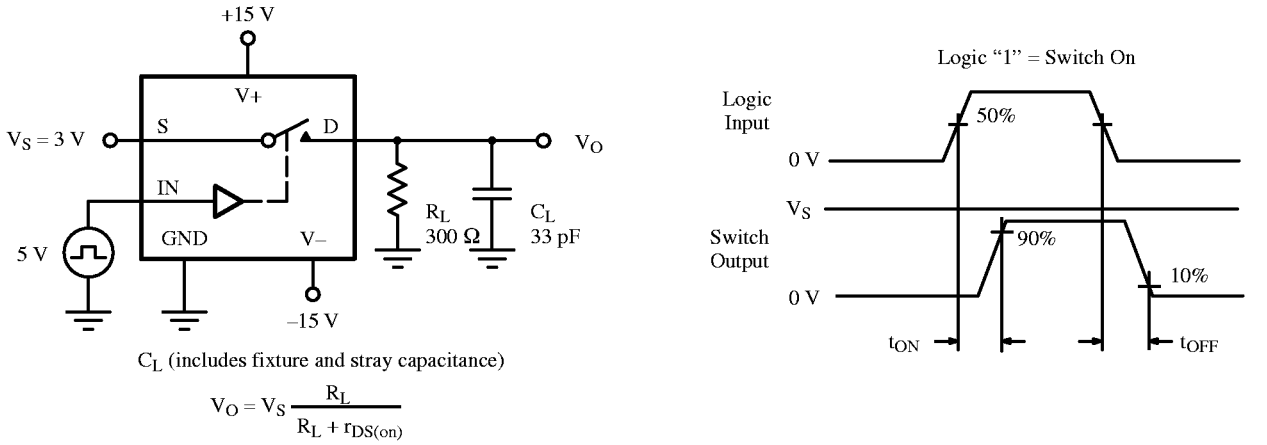


Figure 2. Switching Time

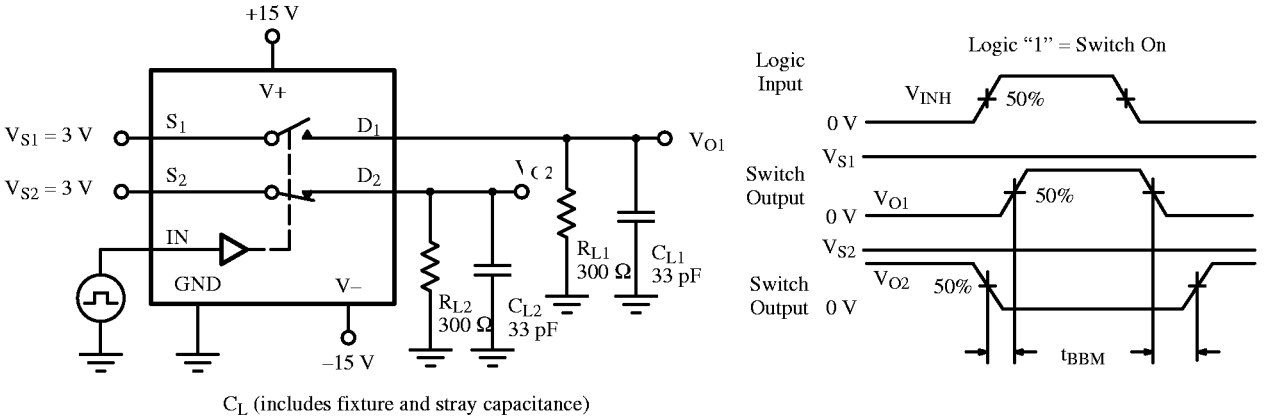


Figure 3. Break-Before-Make SPDT (DG301A, DG303A)

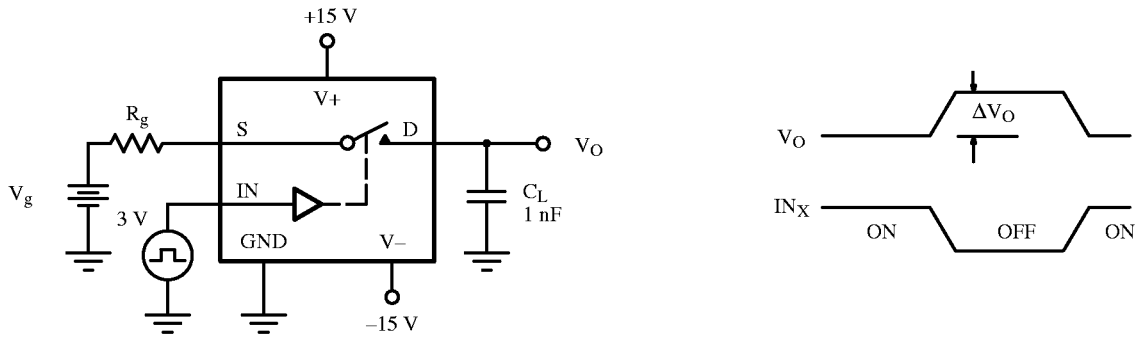


Figure 4. Charge Injection

Application Hints[a]

V+ Positive Supply Voltage (V)	V– Negative Supply Voltage (V)	GND Voltage (V)	V_{IN} Logic Input Voltage $V_{INH(min)}/V_{INL(max)}$ (V)	V_S or V_D Analog Voltage Range (V)
15	–15	0	4/0.8	–15 to 15
20	–20	0	4/0.8	–20 to 20
15	0	0	4/0.8	0 to 15

Note:
a. Application Hints are for DESIGN AID ONLY, not guaranteed and not subject to production testing.

Applications

The DG300A series of analog switches will switch positive analog signals while using a single positive supply. This facilitates their use in applications where only one supply is available. The trade-offs of using single supplies are: 1) Increased $r_{DS(on)}$; 2) slower switching speed. The analog voltage should not go above or below the supply voltages which in single operation are V+ and 0 V. (See Input Switching Threshold vs. Positive Supply Voltage Curve.)

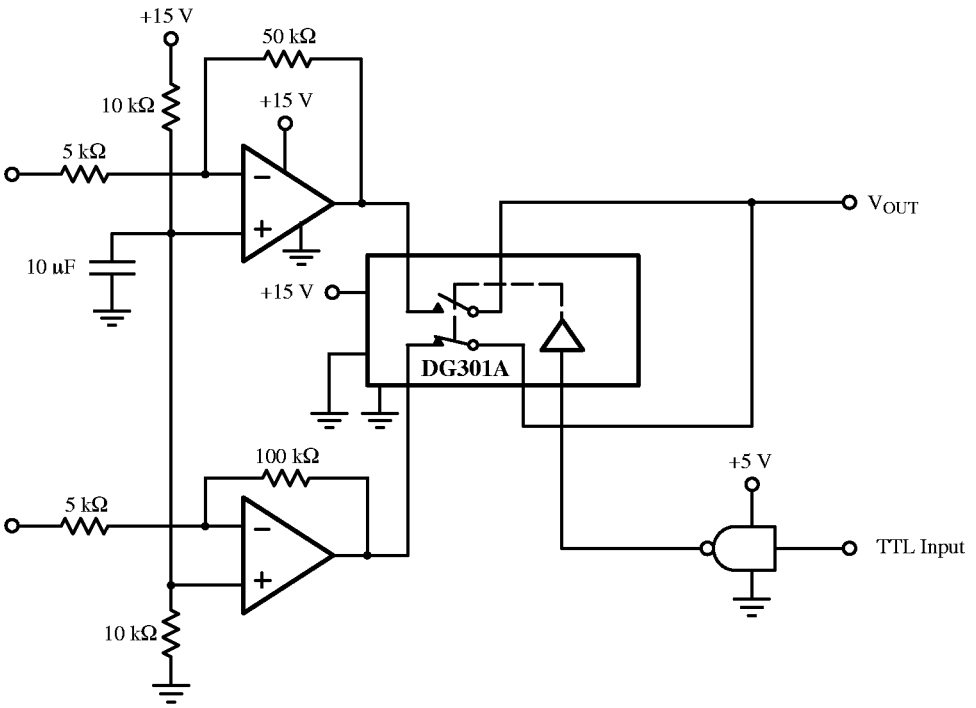


Figure 5. Single Supply Op Amp Switching

Applications (Cont'd)

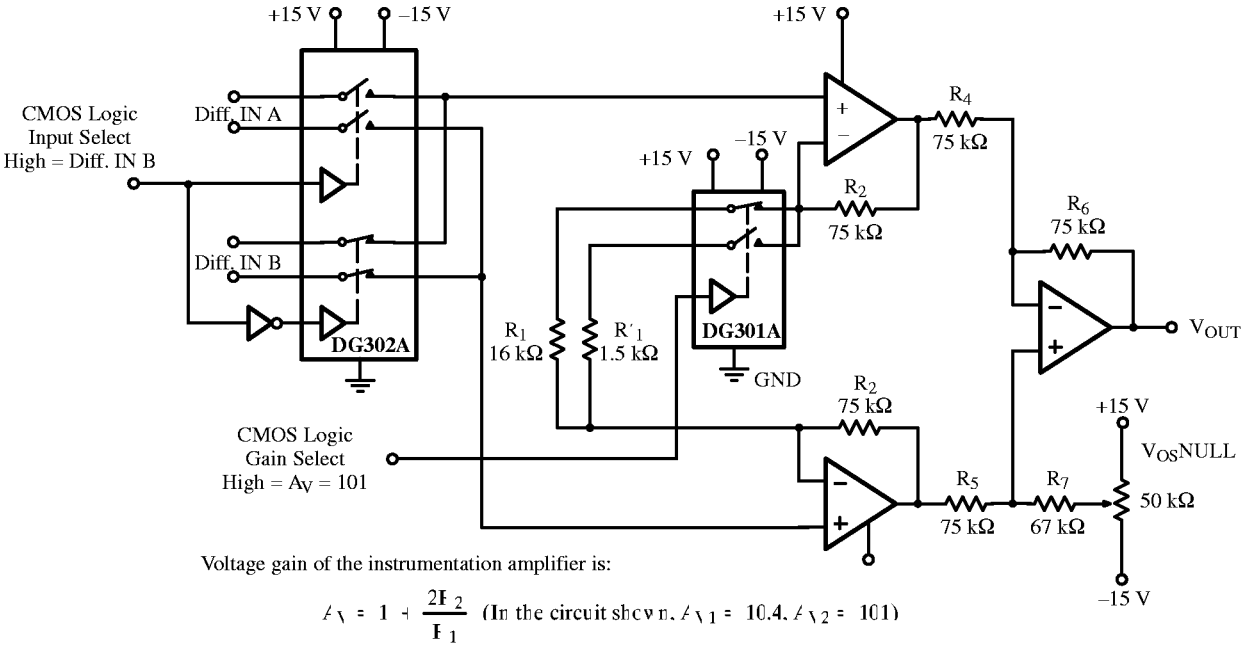
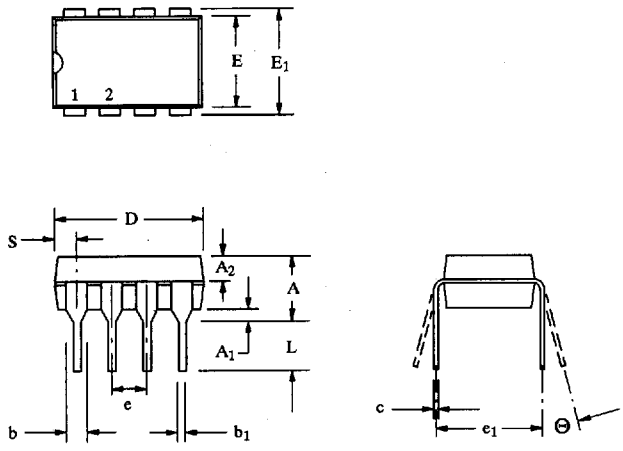


Figure 6. Low Power Instrumentation Amplifier with Digitally Selectable Inputs and Gain

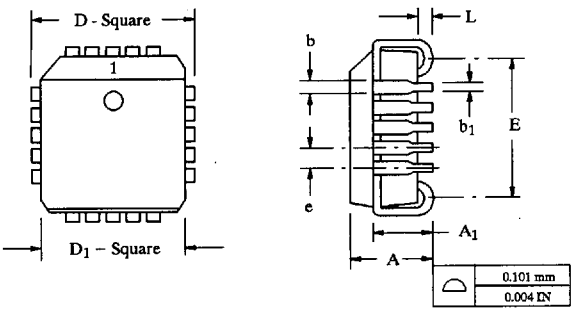
Package Information

■ Plastic DIP, 8- to 20-Pin



Dim	Millimeters		Inches	
	Min	Max	Min	Max
A	3.81	5.08	0.150	0.200
A_1	0.38	1.27	0.015	0.050
A_2	1.27	2.03	0.050	0.080
b	0.89	1.65	0.035	0.065
b_1	0.38	0.51	0.015	0.020
c	0.20	0.30	0.008	0.012
D–8	9.65	11.68	0.380	0.460
D–14	17.27	19.30	0.680	0.760
D–16	18.93	21.33	0.745	0.840
D–20	24.89	26.92	0.980	1.060
E	5.59	7.11	0.220	0.280
E_1	7.62	8.26	0.300	0.325
e	2.29	2.79	0.090	0.110
e_1	7.37	7.87	0.290	0.310
L	2.79	3.81	0.110	0.150
S–8	1.02	2.03	0.040	0.080
S–14	1.02	2.03	0.040	0.080
S–16	0.38	1.52	0.015	0.060
S–20	1.02	2.03	0.040	0.080
Θ	0°	15°	0°	15°

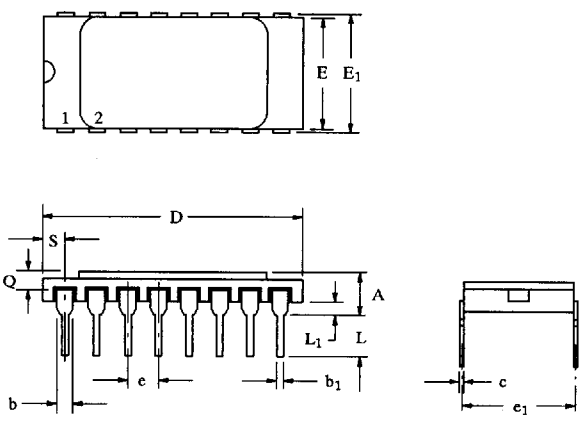
■ PLCC Package, 20-Pin



Dim	Millimeters		Inches	
	Min	Max	Min	Max
A	4.20	4.57	0.165	0.180
A_1	2.29	3.04	0.090	0.120
b	0.66	0.81	0.026	0.032
b_1	0.33	0.55	0.013	0.021
D	9.78	10.03	0.385	0.395
D_1	8.89	9.04	0.350	0.356
E	7.37	8.38	0.290	0.330
e	1.27 BSC		0.050 BSC	
L	0.51	–	0.020	–

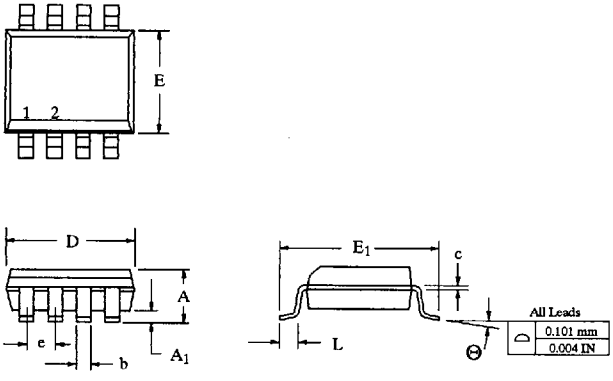
Package Information

■ Sidebraze DIP, 14- to 24-Pin



Dim	Millimeters		Inches	
	Min	Max	Min	Max
A	2.67	4.44	0.105	0.175
b	0.97	1.52	0.038	0.060
b_1	0.38	0.53	0.015	0.021
c	0.20	0.30	0.008	0.012
D–14	17.53	19.55	0.690	0.770
D–16	19.56	21.08	0.770	0.830
D–20	24.89	26.16	0.890	1.030
D–24	29.97	31.24	1.180	1.230
E	7.12	7.87	0.280	0.310
E_1	7.37	8.25	0.290	0.325
e	2.54 BSC		0.100 BSC	
e_1	7.62 BSC		0.300 BSC	
L	3.18	4.44	0.125	0.175
L_1	0.64	1.39	0.025	0.055
Q	0.25	–	0.010	–
S–14	0.77	2.41	0.030	0.095
S–16	0.51	1.65	0.020	0.065
S–20	0.77	1.65	0.030	0.065
S–24	0.77	2.41	0.030	0.095

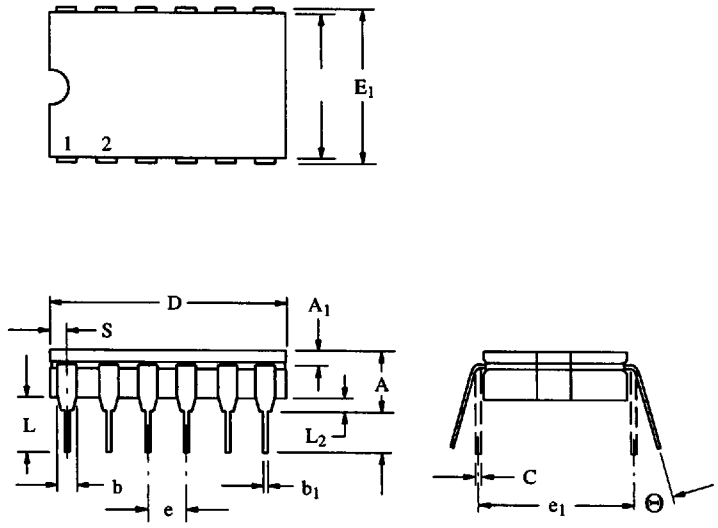
■ SO Package, 8- to 16-Pin



Dim	Millimeters		Inches	
	Min	Max	Min	Max
A	1.35	1.75	0.053	0.069
A_1	0.10	0.20	0.004	0.008
B	0.35	0.45	0.014	0.018
c	0.18	0.23	0.007	0.009
D-8	4.69	5.00	0.185	0.196
D-14	8.55	8.75	0.336	0.344
D-16	9.80	10.00	0.385	0.393
E	3.50	4.05	0.140	0.160
E_1	5.70	6.30	0.224	0.248
e	1.27 BSC		0.050 BSC	
L	0.60	0.80	0.024	0.031
Θ	0°	8°	0°	8°

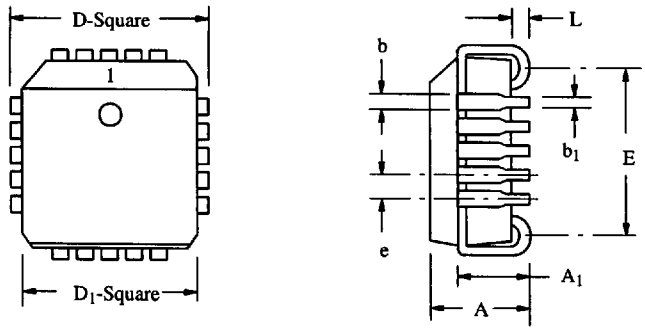
L	0.13	0.25	0.005	0.010
S	0.44	0.55	0.017	0.022
Θ	0°	8°	0°	8°

Ceramic DIP, 8–14 Leads



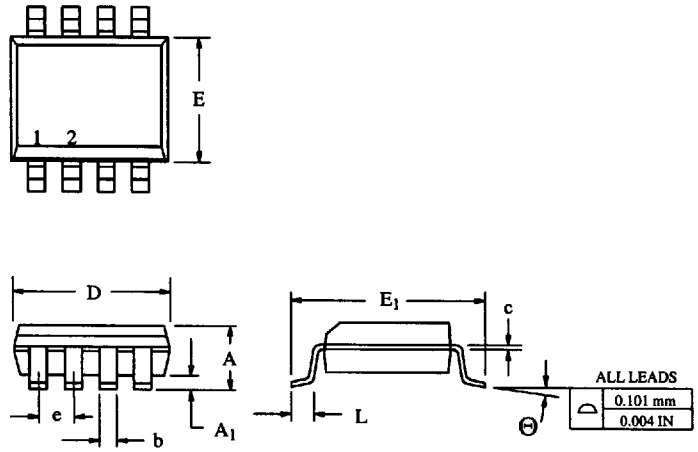
	Millimeters		Inches	
Dim	Min	Max	Min	Max
A	4.06	5.08	0.160	0.200
A_1	1.27	2.16	0.050	0.085
b	1.14	1.65	0.045	0.065
b_1	0.38	0.51	0.015	0.020
C	0.20	0.30	0.008	0.012
D–8	9.40	10.16	0.370	0.400
D–14	19.05	19.56	0.750	0.770
E	6.60	7.62	0.260	0.300
E_1	7.62	8.26	0.300	0.325
e	2.54 BSC		0.100 BSC	
e_1	7.62 BSC		0.300 BSC	
L	3.81	5.08	0.150	0.200
L_1	3.18	3.81	0.125	0.150
L_2	0.51	1.14	0.020	0.045
S–8	0.64	1.52	0.025	0.060
S–14	1.65	2.41	0.065	0.095
S–16	0.38	1.14	0.015	0.045
Θ	0°	15°	0°	15°

PLCC-20



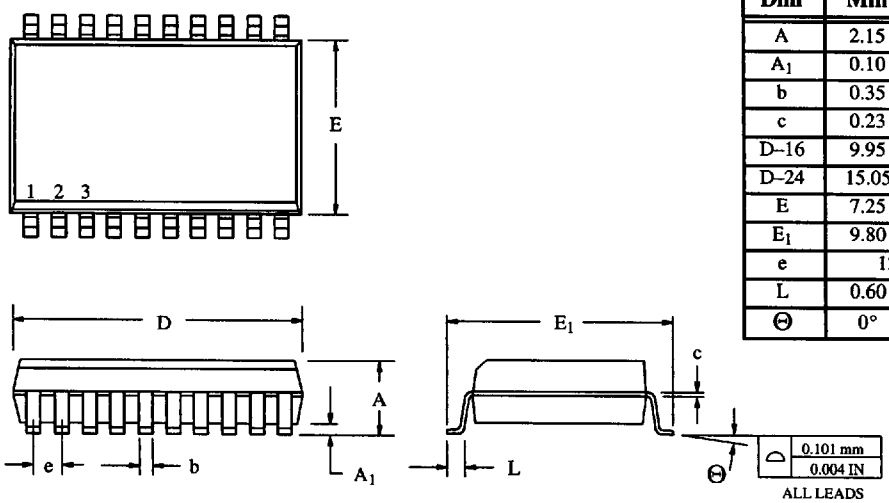
	Millimeters		Inches	
Dim	Min	Max	Min	Max
A	4.20	4.57	0.165	0.180
A_1	2.29	3.04	0.090	0.120
b	0.66	0.81	0.026	0.032
b_1	0.33	0.55	0.013	0.021
D	9.78	10.03	0.385	0.395
D_1	8.89	9.04	0.350	0.356
E	9.78	10.03	0.385	0.395
e	1.27 BSC		0.050 BSC	
L	0.51	–	0.020	–

SOIC, 8–16 Leads



Dim	Millimeters		Inches	
	Min	Max	Min	Max
A	1.35	1.75	0.053	0.069
A_1	0.10	0.20	0.004	0.008
B	0.35	0.45	0.014	0.018
c	0.18	0.23	0.007	0.009
D-8	4.69	5.00	0.185	0.196
D-14	8.55	8.75	0.336	0.344
D-16	9.80	10.00	0.385	0.393
E	3.50	4.05	0.140	0.160
E_1	5.70	6.30	0.224	0.248
e	1.27 BSC		0.050 BSC	
L	0.60	0.80	0.024	0.031
Θ	0°	8°	0°	8°

SOIC Wide-Body, 16–24 Leads



Dim	Millimeters		Inches	
	Min	Max	Min	Max
A	2.15	2.90	0.085	0.114
A_1	0.10	0.30	0.004	0.012
b	0.35	0.45	0.014	0.018
c	0.23	0.28	0.009	0.011
D–16	9.95	10.75	0.392	0.423
D–24	15.05	15.85	0.593	0.624
E	7.25	8.00	0.285	0.315
E_1	9.80	10.60	0.386	0.417
e	127 BSC		0.050 BSC	
L	0.60	0.80	0.024	0.031
Θ	0°	8°	0°	8°