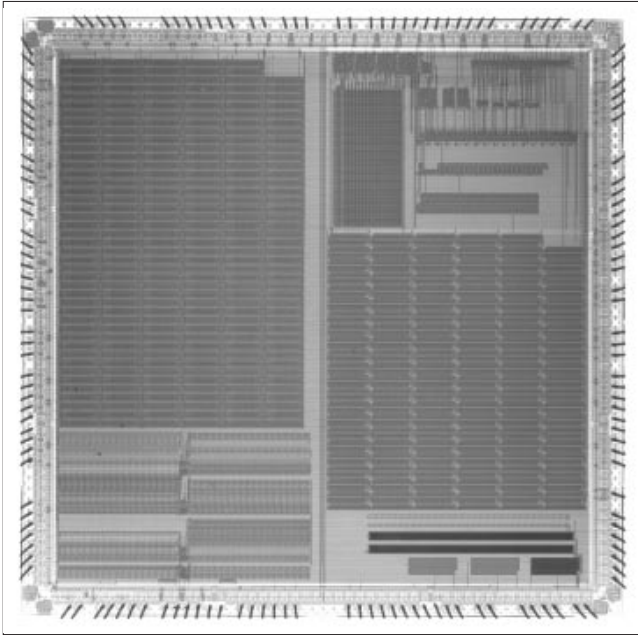


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CLA70000V

LOW VOLTAGE SPECIFICATION

1.0 μ CMOS GATE ARRAYS



GENERAL DESCRIPTION

Advances in processing technology have led to the development of an array family which can operate at 3 volts. This series of arrays may be used with the lower voltage power supply rails which are becoming increasingly common. Applications include battery portable such as laptop computers where low power consumption is essential as well as pagers and consumer applications like hand held language translators and games. This summary datasheet gives information on the CLA70000 series AC and DC characteristics at low voltage.

CLA70000 FAMILY

ARRAY	RAW GATES	PADS
CLA70000	5000	44
CLA71000	12000	68
CLA72000	19000	84
CLA73000	27000	100
CLA74000	39000	120
CLA75000	70000	160
CLA76000	110000	200
CLA77000	182000	256
CLA78000	256000	304

FEATURES

- Operates at 3.3V
- 1.0 μ (0.8 μ Leff) twin well, epitaxial CMOS process
- 5,000 to 250,000 available gates on a channelless array architecture
- Low current and power (<1 μ A/gate/MHz)
- Slew controlled outputs with drivers up to 12mA for bus driving and other applications.
- ESD protection in excess of 2kV
- Comprehensive cell library including DSP and compiled memory cells (ROM blocks to 64K bits and RAM blocks to 16K bits)
- Supports JTAG/BIST test philosophies (IEEE 1149-1 Test Procedures)
- Fully supported on Industry Standard workstations and in-house software

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CLA7000V

CMOS PROCESS TECHNOLOGY

The CLA70000 arrays are based on GEC Plessey Semiconductors well proven 1µ CMOS process, manufactured at GPS's advanced , Class 10, six-inch wafer fabrication facility. The process (fig.1) is a twin well, self aligned oxide-isolated technology, with an effective channel length of 0.8µm (1.0µm drawn), giving a low defect density, high reliability, and inherently low power dissipation. The process has excellent immunity to latch-up, and ESD, and exhibits stable performance characteristics.

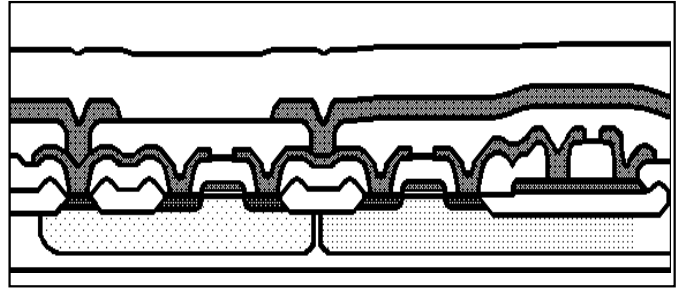


Figure 1 : Process 'VQ' Process Cross Section

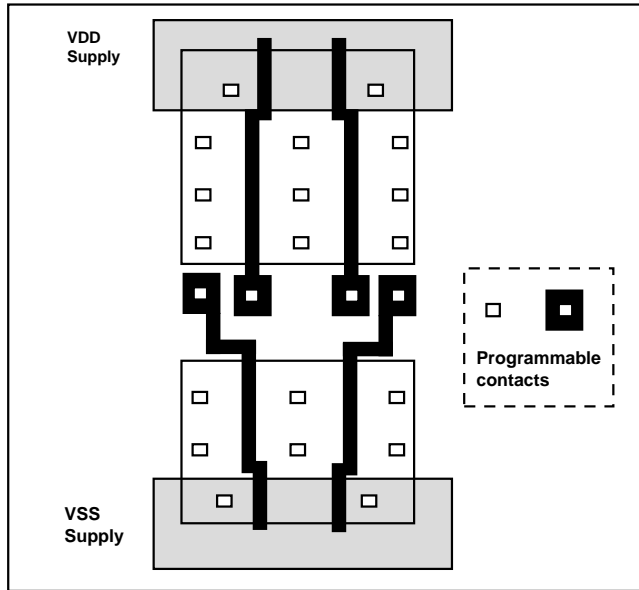


Figure 2 : Diagrammatic representation of Array Core Cell

CORE CELL DESIGN

A four transistor group (2 NMOS and 2 PMOS) (fig 2.) forms the basic cell of the core array. This array element is repeated in a regular fashion over the complete core area to give a homogeneous 'Full Field' (sea of gates) array. This lends itself to hierarchical design, allowing pre-routed user defined subcircuits to be repeated anywhere on the array. The core cell structure has been carefully designed to maximise the number of nets which may be routed through the cell. This enables optimal routing for both data flow and control signal distribution schemes thus giving very high overall utilisation figures. This feature is of particular benefit in designs using highly structured blocks such as memory or arithmetic functions.

INPUT/OUTPUT BUFFER DESIGN

The peripheral cells (fig.3) are fully programmable as Input, Output, VDD or GND, and they are designed to offer several interfacing options, TTL and CMOS for example. The cells already contain input 'pull-up' and 'pull-down' resistors and Electro Static Discharge protection elements. Components for implementing Schmitt Triggers, TTL threshold detectors, tristate control, and flip-flops for signal re-timing are also included. A range of output buffers is available with various output drive currents to match system requirements.

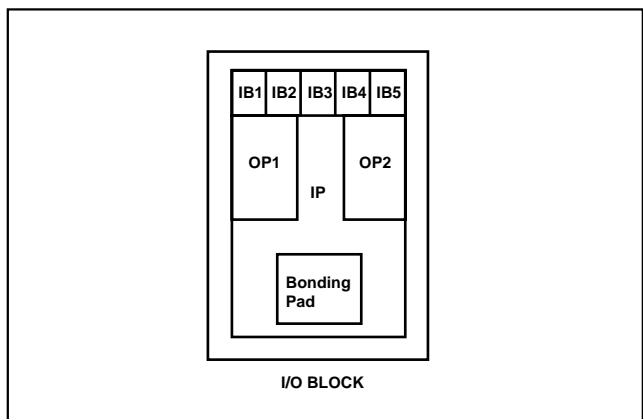


Figure 3

Noise transients due to a large number of simultaneously switching outputs are an increasing problem as bus widths widen (The supply pad location, and the inductance of the bond wires and package leads are also factors). CLA70000 Arrays offer several I/O buffers with the capability to control the output slew (di/dt) (fig.4) which are invaluable in controlling these transients when driving large capacitive loads such as busses.

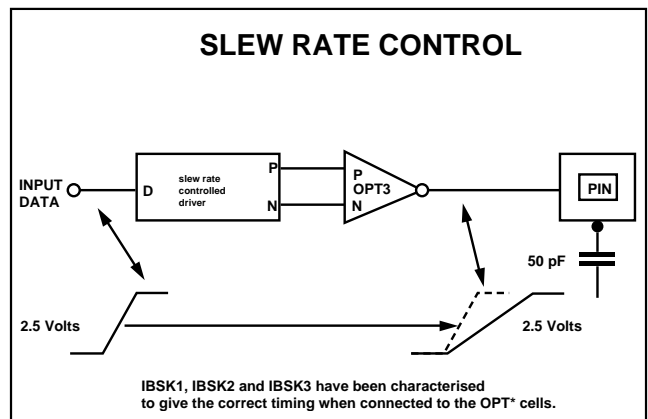


Figure 4

AC CHARACTERISTICS

The performance of the CLA70000V device depends on numerous factors including:

- Supply voltage
- Ambient temperature, and temperature of the devices active junctions
- Gate front, i.e. the logic loading on the gate outputs
- Interconnection loading on the gates
- Processing tolerance, i.e. the manufacturing spreads

The CLA70000 technology library contains all the performance information for each cell in the design libraries. The PDS design software suite accesses this data, and the simulation program automatically calculates the design's performance under the selected operating conditions. Prior to layout, estimates of the interconnection loadings are used in the simulations. After layout, track loadings are extracted from the physical design to allow re-simulation with actual values to confirm device performance.

The effect of those factors on the propagation delays of arrange of selected cells is illustrated in the tables below.

Fanout is in gate load units

INTERNAL CORE CELLS				Typical propagation Delay Ns 5 volts 25°C	Worst case Propagation Delay (ns) 3 volts 70°C	
					Fanout	
Name	Cells	Description	Symbol	Fanout = 2	2	4
INV2	1	INVERTER DUAL DRIVE	tpLH	0.27	0.95	1.14
			tpLH	0.18	0.64	0.76
NAND2	1	2-INPUT NAND GATE	tpHL	0.39	1.37	1.75
			tpLH	0.30	1.07	1.41
NOR2	1	2-INPUT NOR GATE	tpLH	0.50	1.77	2.46
			tpLH	0.22	0.78	1.09
DF	4	MASTER SLAVE D-TYPE FLIP FLOP	tpHL	0.54	1.90	2.18
			tpLH	0.55	1.96	2.11

INTERMEDIATE BUFFER CELLS				Typical propagation Delay Ns 5 volts 25°C	Worst case Propagation Delay (ns) 3 volts 70°C	
					Fanout	
Name	Cells	Description	Symbol	Fanout = 2	2	4
IBGATE	-	LARGE 2 INPUT NAND GATE +2 INPUT NOR	tpLH	0.34	1.20	1.39
			tpLH	0.27	0.97	1.14
IBDF	-	MASTER SLAVE D-TYPE FLIP FLOP	tpHL	0.48	1.69	1.96
			tpLH	0.50	1.78	1.93
IBCMOS1	-	CMOS INPUT BUFFER WITH 2 INPUT NAND GATE	tpLH	0.60	2.15	2.28
			tpLH	0.45	1.59	1.65

OUTPUT BUFFER CELLS				Typical propagation Delay Ns 5 volts 25°C	Worst case Propagation Delay (ns) 3 volts 70°C	
					Fanout	
Name	Cells	Description	Symbol	Fanout = 10pF	10pF	50pF
OP3	-	STANDARD OUTPUT BUFFER	tpLH	0.73	2.58	8.83
			tpLH	0.49	1.73	5.98
OP6	-	MEDIUM OUTPUT BUFFER	tpHL	0.50	1.77	4.88
			tpLH	0.33	1.16	3.29
OP12	-	LARGE OUTPUT BUFFER	tpLH	0.38	1.35	2.91
			tpLH	0.25	0.90	2.04

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DC ELECTRICAL CHARACTERISTICS

All characteristics at 3 - 5.5 volts and 0 -70°C temperature

CHARACTERISTIC	SYM	VALUE			UNIT	CONDITIONS
		Min	Typ	Max		
LOW LEVEL INPUT VOLTAGE TTL Inputs (IBTTL1/IBTTL2) CMOS Inputs (IBCMOS1/IBCMOS2)	VIL			0.6 0.2VDD	V	
HIGH LEVEL INPUT VOLTAGE TTL Inputs (IBTTL1/IBTTL2) CMOS Inputs (IBCMOS1/IBCMOS2)	VIH	2.2V 0.75VDD			V	
INPUT HYSTERESIS (IBST1) Rising Falling (IBST2) Rising Falling	VT+ VT- VT+ VT-		1.9 1.2 1.3 0.8		V	VIL to VIH VIH to VIL VIL to VIH VIH to VIL } VDD =3V
INPUT CURRENT/RESISTANCE (CMOS / TTL INPUTS) No Resistor Inputs with 1Kohm Resistors Inputs with 2Kohm Resistors Inputs with 4Kohm Resistors Inputs with 75Kohm Resistors Resistor values nominal - See note 1	IIN	0.50 1.00 2.00 20.00	1.00 2.00 4.00 75.00	1 2 4 8 250	μA KΩ KΩ KΩ KΩ	VIN = VDD or VSS
HIGH LEVEL OUTPUT VOLTAGE All outputs Smallest drive cell OP1/OPT1/OPOS1 Low drive cell OP2/OPT2/OPOS2 Standard drive cell OP3/OPT3/OPOS3 Medium drive cell OP6/OPT6/OPOS6 Large drive cell OP12/OPT12/OPOS12	VOH	0.75VDD 0.75VDD 0.75VDD 0.75VDD 0.75VDD	VDD - 0.05 0.9VDD 0.9VDD 0.9VDD 0.9VDD		V	IOH = -1μA IOH = -1mA IOH = -2mA IOH = -3mA IOH = -6mA IOH = -12mA
LOW LEVEL OUTPUT VOLTAGE All outputs Smallest drive cell OP1/OPT1/OPOD1 Low drive cell OP2/OPT2/OPOD2 Standard drive cell OP3/OPT3/OPOD3 Medium drive cell OP6/OPT6/OPOD6 Large drive cell OP12/OPT12/OPOD12	VOL		VSS + 0.05 0.2 0.2 0.2 0.2 0.2	0.4 0.4 0.4 0.4 0.4	V	IOL = 1μA IOL = 1mA IOL = 2mA IOL = 3mA IOL = 6mA IOL = 12mA
TRISTATE OUTPUT LEAKAGE CURRENT Tristate, open drain and open source output cells	IOZ	-1		1	μA	VOUT = VSS or VDD
OUTPUT SHORT CIRCUIT CURRENT Standard outputs OP3/OPT3/OPOD3 (See note 2) OP3/OPT3/OPOS3	IOS	67 37	135 75	270 150	mA	VDD = MAX, VOOUT = VDD VDD = MAX, VOOUT = 0V
OPERATING SUPPLY CURRENT (per gate) (see note 3)	IDDOP		1		μA/MHz	
INPUT CAPACITANCE	CI		5		pF	ANY INPUTS (Note 4)
OUTPUT CAPACITANCE	COUT		5		pF	ANY OUTPUT (Note 4)
BIDIRECTIONAL PIN CAPACITANCE	CVO		7		pF	ANY I/O PIN (Note 5)

Note 1: If resistors are used with outputs the correct value of the resistor must be used to maintain VOL/VOH logic levels.

Note 2: Standard driver output OP3 etc. Short circuit current for other outputs will scale. Not more than one output may be shorted at a time for a maximum duration of one second.

Note 3: Excluding peripheral buffers.

Note 4: Excludes package leadframe capacitance or bidirectional pins.

Note 5: Excludes package.

ABSOLUTE MAXIMUM RATINGS

PARAMETER	MIN	MAX	UNITS
Supply Voltage	- 0.5	7.0	V
Input Voltage	- 0.5	VDD+0.5	V
Output Voltage	- 0.5	VDD+0.5	V
Operation above these absolute maximum ratings or prolonged periods above the recommended operating limits may permanently damage device characteristics and may affect reliability.			
Storage Temperature:			
Ceramic	-65	150	degree C
Plastic	- 40	125	degree C

RECOMMENDED OPERATING LIMITS

PARAMETER	MIN	MAX	UNITS
Supply Voltage	3.0	5.5	V
Input Voltage	VSS	VDD	V
Output Voltage	VSS	VDD	V
Current per pad		100	mA
Operating Temperature:			
Commercial Grade	0	70	degree C
Industrial Grade	-40	85	degree C
Military Grade	-55	125	degree C

DESIGN TOOLS

The focus of the GEC Plessey design tool methodology is that of maintaining an open CAD system with all interfaces standardized via EDIF 2.0 . This enables us to provide full support for a variety of 3rd party ASIC design tools and facilitates rapid updating of associated libraries. It also provides an interface to the GEC Plessey (PDS2) design system, which offers a total design environment including behavioral and functional level modelling.

PDS2 - THE GPS ASIC DESIGN SYSTEM

- Behavioral, Functional, and Gate Level Modelling
- VHDL and Third Party Links
- Supports Hierarchical Design Techniques
- EDIF 2.0 Interface

PDS2 is GPS's own proprietary ASIC design system. It provides a fully-integrated, technology independent VLSI design environment for all GPS CMOS SemiCustom products.

THIRD PARTY SOFTWARE SUPPORT

- Design Kits for major industry standard ASIC design software tools
- All libraries include fully detailed timing information
- EDIF 2.0 Interface
- Post layout back annotation available

GPS supports a wide range of third party design tools including IKOS, Mentor, Verilog, and Viewlogic. The design kits offer fully detailed timing information for all cell libraries, netlist extraction utilities, and post layout back annotation capability where applicable. An example of a workstation design flow is shown in the figure 5 (opposite). Please contact your local GEC Plessey Semiconductor's sales office for further information about support of particular tools.

DESIGN SUPPORT

Design support is available from various centres worldwide each of which is connected to our Headquarters via high speed data links. A design centre engineer is assigned to each customers circuit, to ensure good communication, and a smooth and efficient design flow.

As part of the design process GPS operates a thorough design audit procedure to verify compliance with customer specification and to ensure manufacturability. The procedure includes four separate review meetings, with the customer, held at key stages of the design. The standard design audit procedure is outlined opposite.

PDS2 runs on Digital Equipment computers and is self configuring according to the available machine resources. It comprises design capture (schematic capture or VHDL), testability analysis, logic simulation, fault simulation, auto place and route, and back annotation. The system offers full support for hierarchical design techniques, maintained from design capture through to layout, as well as advanced design management tools. PDS2 may be used either at a GPS Design Center or under licence at the customer's premises. A three day training course is available for first time users.

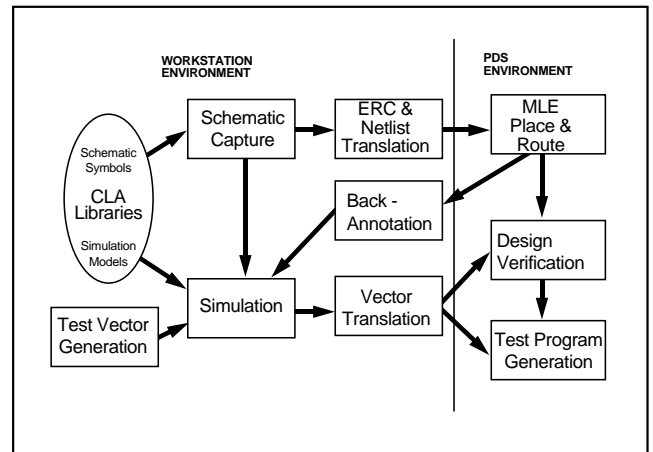


Figure 5 : Workstation Design Flow

- Review 1: Held at the beginning of the design cycle to check and agree on specifications and design timescales.
- Review 2: Held after Logic Simulation and prior to Layout. Checks to ensure satisfactory functionality, timing performance, and adequate fault coverage
- Review 3: Held after Layout and Post layout Simulation. Verification of design performance after insertion of actual track loads. Final check of all device specifications before prototype manufacture.
- Review 4: Held after prototype delivery. Confirms that the devices meet the specification and are suitable for full scale production.

CLA70000V

PACKAGING

Production quantities of the CLA70000 family are available in industry-standard ceramic and plastic packages according to the codes shown below. Prototype samples are normally supplied in ceramic only.

DC	DILMON	Dual in Line, Multilayer ceramic. Brazed leads Metal Sealed Lid. Through Board.
DG	CERDIP	Dual In Line, Ceramic body, Alloy leadframe, Glass Sealed, Through Board.
DP	PLASDIP	Dual In Line, Copper or Alloy leadframe, Plastic Moulded. Through Board.
AC	P.G.A.	Pin Grid Array, Multilayer Ceramic. Metal Sealed lid. Through Board.
AC (P)	POWER P.G.A.	As above with cavity down and Cu/W heat plate.
MP	SMALL OUTLINE (S.O.)	Dual In Line, 'Gullwing' Formed Leads. Plastic Moulded Surface Mount.
LC	LCC	Leadless Chip Carrier. Multilayer Ceramic. Metal Sealed Lid. Surface Mount.
HC	LEADED CHIP CARRIER	Quad Multilayer Ceramic. Brazed J Formed Leads. Metal Sealed Lid. Surface Mount
GC	LEADED CHIP CARRIER	Quad Multilayer Ceramic. Brazed Leads. Metal Sealed Lid. Surface Mount.
GC (P)	POWER LEADED CHIP CARRIER	As above with cavity down, and Cu/W heat plate.
HG	QUAD CERPAC	Quad Ceramic Body, 'J' Formed Leads. Glass Sealed. Surface Mount.
GG	CERAMIC QUAD FLATPACK	Quad Ceramic Body, 'Gullwing' Formed Leads. Glass Sealed. Surface Mount.
HP	PLCC	Quad Plastic Leaded Chip Carrier. 'J' Formed Leads. Plastic Moulded. Surface Mount
GP	PQFP	Plastic Quad Flat Pack. 'Gullwing' Formed Leads. Plastic Moulded. Surface Mount.

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