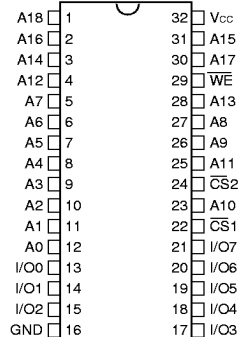
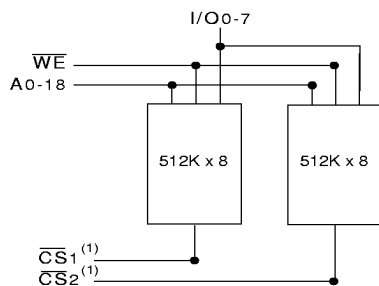


**2x512Kx8 DUALITHIC™ SRAM** *ADVANCED****PIN CONFIGURATION FOR WS1M8V-XCX****32 DIP
TOP VIEW****PIN DESCRIPTION**

A0-18	Address Inputs
I/O0-7	Data Input/Output
CS1-2	Chip Selects
WE	Write Enable
Vcc	+3.3V Power Supply
GND	Ground

BLOCK DIAGRAM**NOTE:**

1. CS1 and CS2 are used to select the lower and upper 512Kx8 of the device. CS1 and CS2 must not be enabled at the same time.

FEATURES

- Access Times 17, 20, 25, 35, 45, 55ns
- Evolutionary, Corner Power/Ground Pinout
- Packaging:
 - 32 pin, Hermetic Ceramic DIP (Package 300)
- Organized as two banks of 512Kx8
- Commercial, Industrial and Military Temperature Ranges
- 3.3V Power Supply
- Low Power CMOS
- TTL Compatible Inputs and Outputs
- Output Enable Internally tied to GND.

* This data sheet describes a product that may or may not be under development and is subject to change or cancellation without notice.

**ABSOLUTE MAXIMUM RATINGS**

Parameter	Symbol	Min	Max	Unit
Operating Temperature	T _A	-55	+125	°C
Storage Temperature	T _{STG}	-65	+150	°C
Signal Voltage Relative to GND	V _I	-0.5	+4.6	V
Junction Temperature	T _J		150	°C
Supply Voltage	V _{CC}	-0.5	5.5	V

RECOMMENDED OPERATING CONDITIONS

Parameter	Symbol	Min	Max	Unit
Supply Voltage	V _{CC}	3.0	3.6	V
Input High Voltage	V _{IH}	2.2	V _{CC} + 0.3	V
Input Low Voltage	V _{IL}	-0.3	+0.8	V
Operating Temp. (Mil.)	T _A	-55	+125	°C

TRUTH TABLE

$\overline{CS}$	$\overline{WE}$	Mode	Data I/O	Power
H	X	Standby	High Z	Standby
L	H	Read	Data Out	Active
L	L	Write	Data In	Active

NOTE: $\overline{OE}$ is internally tied to GND.**CAPACITANCE**(T_A = +25°C)

Parameter	Symbol	Condition	Max	Unit
Input capacitance	C _{IN}	V _{IN} = 0V, f = 1.0MHz	28	pF
Output capacitance	C _{OUT}	V _{OUT} = 0V, f = 1.0MHz	28	pF

This parameter is guaranteed by design but not tested.

DC CHARACTERISTICS(V_{CC} = 3.3V, GND = 0V, T_A = -55°C to +125°C)

Parameter	Sym	Conditions			Units
			Min	Max	
Input Leakage Current	I _{LI}	V _{CC} = 3.6, V _{IN} = GND to V _{CC}		10	μA
Output Leakage Current	I _{LO} ¹	$\overline{CS}$ = V _{IH} , V _{OUT} = GND to V _{CC}		10	μA
Operating Supply Current	I _{CC} ¹	$\overline{CS}$ = V _{IL} , f = 5MHz, V _{CC} = 3.6		160	mA
Standby Current	I _{SB} ¹	$\overline{CS}$ = V _{IH} , f = 5MHz, V _{CC} = 3.6		30	mA
Output Low Voltage	V _{OL}	I _{OL} = 8.0mA		0.4	V
Output High Voltage	V _{OH}	I _{OH} = -4.0mA	2.4		V

NOTE: DC test conditions: V_{IH} = V_{CC} - 0.3V, V_{IL} = 0.3V1. $\overline{OE}$ is internally tied to GND.

**AC CHARACTERISTICS**(V_{CC} = 3.3V, GND = 0V, T_A = -55°C to +125°C)

Parameter	Symbol	-17		-20		-25		-35		-45		-55		Units
		Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	
Read Cycle														
Read Cycle Time	t _{RC}	17		20		25		35		45		55		ns
Address Access Time	t _{AA}		17		20		25		35		45		55	ns
Output Hold from Address Change	t _{OH}	0		0		0		0		0		0		ns
Chip Select Access Time	t _{ACS}		17		20		25		35		45		55	ns
Chip Select to Output in Low Z	t _{CLZ} ¹	2		2		2		4		4		4		ns
Chip Disable to Output in High Z	t _{CHZ} ¹		9		10		12		15		20		20	ns

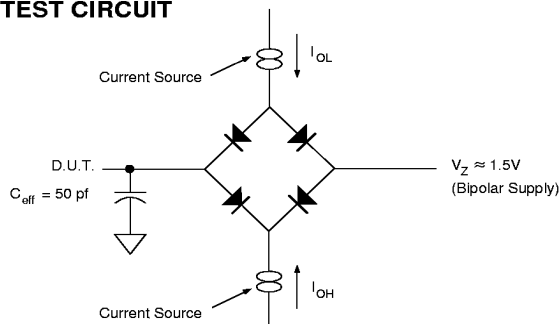
1. This parameter is guaranteed by design but not tested.

2. OE is internally tied to GND.

AC CHARACTERISTICS(V_{CC} = 3.3V, GND = 0V, T_A = -55°C to +125°C)

Parameter	Symbol	-17		-20		-25		-35		-45		-55		Units
		Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	
Write Cycle														
Write Cycle Time	t _{WC}	17		20		25		35		45		55		ns
Chip Select to End of Write	t _{CW}	14		14		15		25		35		50		ns
Address Valid to End of Write	t _{AW}	14		14		15		25		35		50		ns
Data Valid to End of Write	t _{DW}	9		10		10		20		25		25		ns
Write Pulse Width	t _{WP}	14		14		15		25		35		40		ns
Address Setup Time	t _{AS}	0		0		0		0		0		0		ns
Address Hold Time	t _{AH}	0		0		0		0		5		5		ns
Output Active from End of Write	t _{OW} ¹	2		3		4		4		5		5		ns
Write Enable to Output in High Z	t _{WHZ} ¹		9		9		10		15		15		25	ns
Data Hold Time	t _{DH}	0		0		0		0		0		0		ns

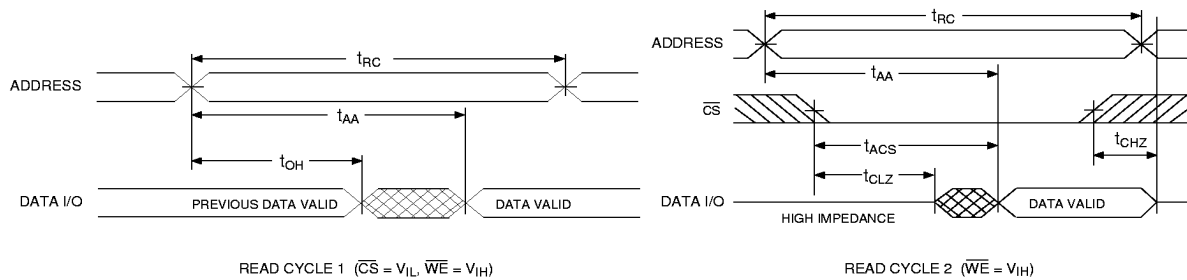
1. This parameter is guaranteed by design but not tested.

AC TEST CIRCUIT**AC TEST CONDITIONS**

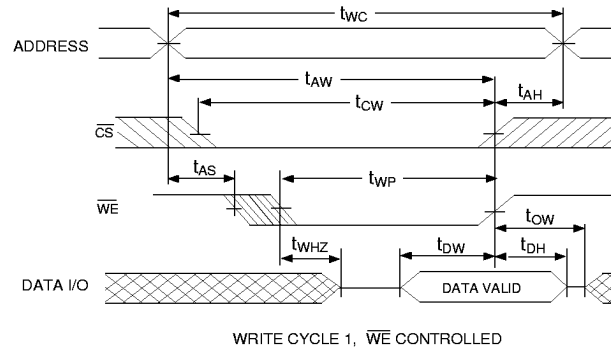
Parameter	Typ	Unit
Input Pulse Levels	V _{IL} = 0, V _{IH} = 2.5	V
Input Rise and Fall	5	ns
Input and Output Reference Level	1.5	V
Output Timing Reference Level	1.5	V

NOTES:V_Z is programmable from -2V to +7V.I_{OL} & I_{OH} programmable from 0 to 16mA.Tester Impedance Z₀ = 75 Ω.V_Z is typically the midpoint of V_{OH} and V_{OL}.I_{OL} & I_{OH} are adjusted to simulate a typical resistive load circuit.

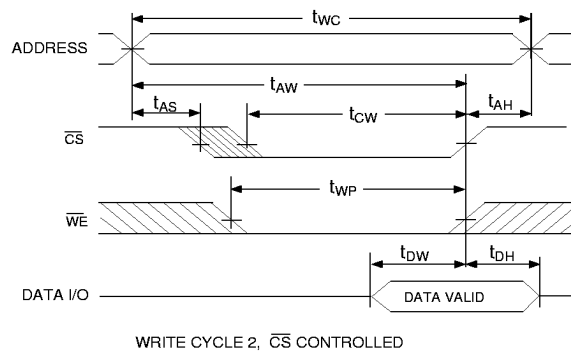
ATE tester includes jig capacitance.

**TIMING WAVEFORM - READ CYCLE**

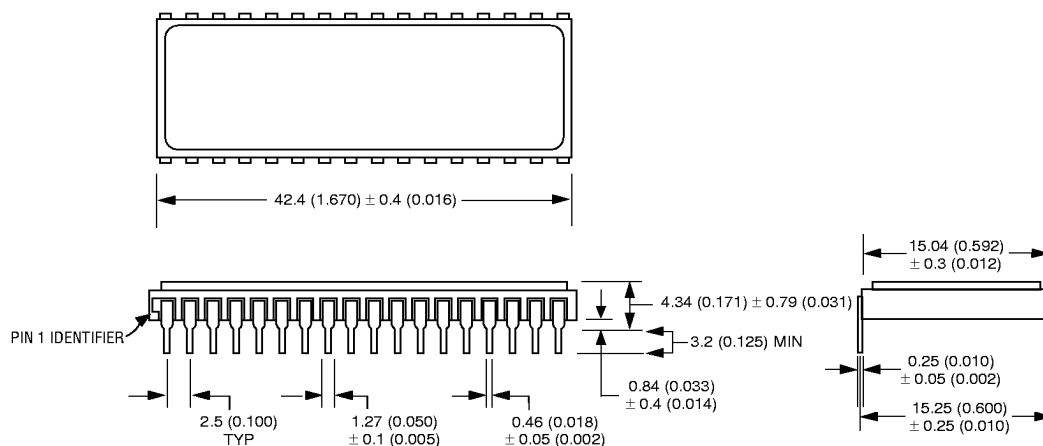
NOTE: $\overline{OE}$ is internally tied to GND.

WRITE CYCLE - $\overline{WE}$ CONTROLLED

WRITE CYCLE 1, $\overline{WE}$ CONTROLLED

WRITE CYCLE - $\overline{CS}$ CONTROLLED

WRITE CYCLE 2, $\overline{CS}$ CONTROLLED

**PACKAGE 300: 32 PIN, CERAMIC DIP, SINGLE CAVITY SIDE BRAZED**

ALL LINEAR DIMENSIONS ARE MILLIMETERS AND PARENTHETICALLY IN INCHES

ORDERING INFORMATION**W S 1M8 V - XXX C X X****LEAD FINISH:**

Blank = Gold plated leads

A = Solder dip leads

DEVICE GRADE:

M = Military Screened -55°C to +125°C

I = Industrial -40°C to +85°C

C = Commercial 0°C to +70°C

PACKAGE:

C = Ceramic 0.600" DIP (Package 300)

ACCESS TIME (ns)

Low Voltage Supply 3.3V ± 10%

ORGANIZATION, two banks of 512K x 8

SRAM

WHITE MICROELECTRONICS