Winbond Electronics Corp.

USB KEYBOARD/ DEVICE CONTROLLER

GENERAL DESCRIPTION

W81C280 is a single-chip microcontroller with Universal Serial Bus (USB) interface for keyboard application, it includes the core of Winbond•• 8-bit microprocessor W78C52. It implements a standard PC keyboard and enables connection to host system through low- speed (1.5Mhz) USB. It complies with USB Specification Revision 1.0 and HID Class Definition Revision 1.0.

W81C280 supports an 18 X 8 keyboard scan matrix wihich allows suspend wakeup, and also provides a port for PS/2 mouse. It consists of an 8051 compatible CPU core, a 6K-byte ROM, a 256-byte SRAM, and three 16-bit programmable timers.

W81C280 supports one device address and five endpoints, one for Control transfer and four for Interrupt transfer, it can be used for multi-function device design.

FEATURES

- Complying with USB spec. Rev.1.0 and HID Class Rev. 1.0
- Supporting one device address and five endpoints (one Control transfer, four Interrupt transfer)
- Implementing USB keyboard with PS/2 mouse connection
- Supporting 8-bit sense (row) input with wakeup interrupt on falling eage, internal pull-ups
- Supporting 18-bit drive (column) output, open drain with pull-ups
- 8-bit 8051 compatible CPU core
- 6K-byte ROM
- 256-byte SRAM
- 3 direct drive LED outputs with internal series resisters, Isink= 20 mA
- Supporting warm reset
- Supporting external serial EEPROM access
- 40-pin DIP
- 5V CMOS Device

Publication Release Date: May 1997
Revision A1

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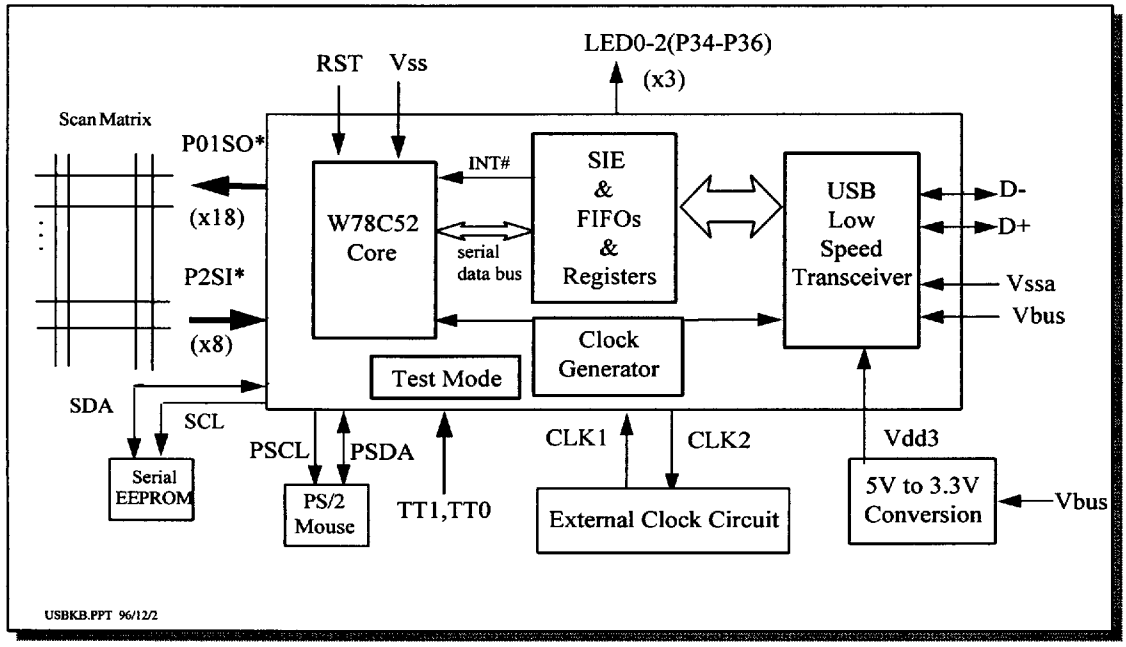
BLOCK DIAGRAM



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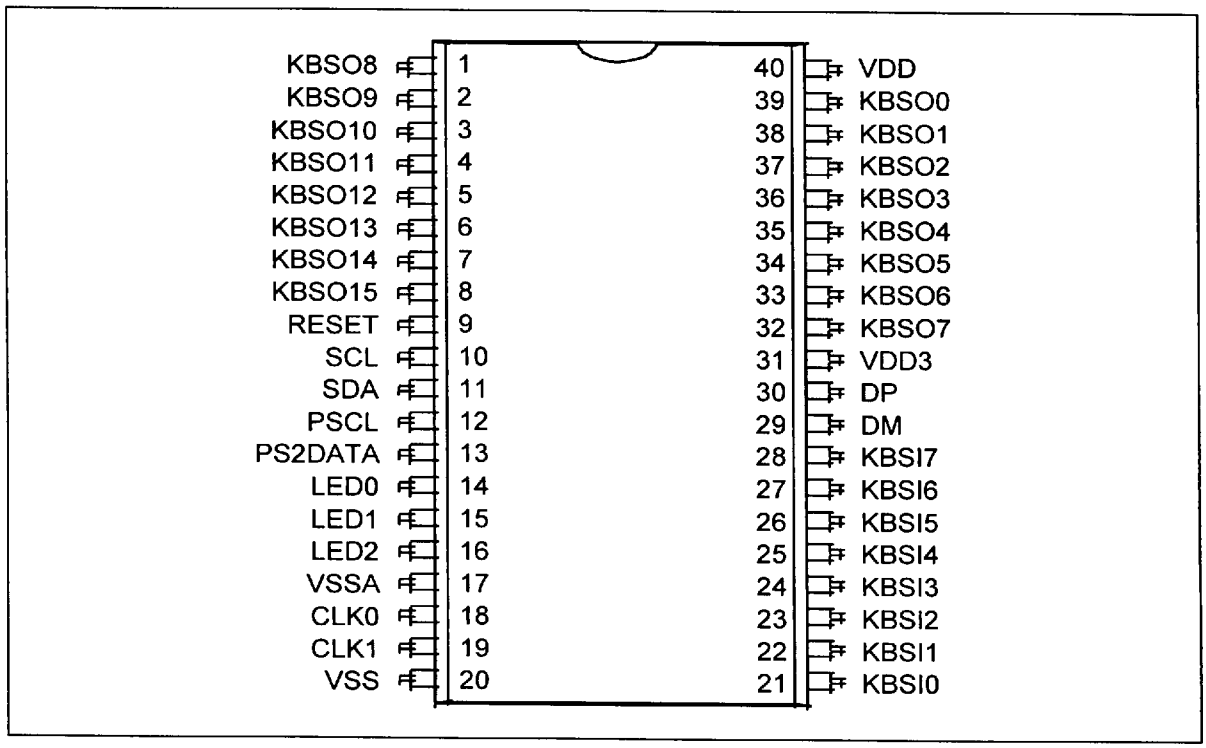
PIN CONFIGURATION



PIN DESCRIPTION

40 DIP PIN#	NAME	TYPE	DESCRIPTION
1	P10 / KBSO8	OUTPUT	Keyboard scan output
2	P11 / KBSO9	OUTPUT	Keyboard scan output
3	P12 / KBSO10	OUTPUT	Keyboard scan output
4	P13 / KBSO11	OUTPUT	Keyboard scan output
5	P14 / KBSO12	OUTPUT	Keyboard scan output
6	P15 / KBSO13	OUTPUT	Keyboard scan output
7	P16 / KBSO14	OUTPUT	Keyboard scan output

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3.1 Pin Description, continued

40 DIP PIN#	NAME	TYPE	DESCRIPTION
8	P17 / KBSO15	OUTPUT	Keyboard scan output
9	RESET	INPUT	Reset signal
10	P30(TT0) / SCL	I/O	P30 / EEPROM CLK (IE.6=1, IP.3=1,see 5.3) Pull high when RESET falling
11	P31(TT1) / SDA	I/O	P31 / EEPROM DATA (IE.6=1, IP.3=1,see 5.3) Pull high when RESET falling
12	PSCL	I/O	PS2 clock line
13	PSDA	I/O	PS2 data line
14*	P34/ KBSO16/ LED0	I/O	Keyboard scan output (Direct LED Drive)
15*	P35/ KBSO17/ LED1	I/O	Keyboard scan output (Direct LED Drive)
16	P36/ LED2	OUTPUT	Direct LED drive, Port36
17	VSSA	POWER	Analog ground
18	CLK0	OUTPUT	Crystal output
19	CLK1	INPUT	Crystal input
20	VSS	POWER	GND
21	P20/ KBSI0	INPUT	Keyboard scan intput
22	P21/ KBSI1	INPUT	Keyboard scan intput
23	P22/ KBSI2	INPUT	Keyboard scan intput
24	P23/ KBSI3	INPUT	Keyboard scan intput
25	P24/ KBSI4	INPUT	Keyboard scan intput
26	P25/ KBSI5	INPUT	Keyboard scan intput
27	P26/ KBSI6	INPUT	Keyboard scan intput
28	P27/ KBSI7	INPUT	Keyboard scan intput
29	DM	I/O	USB upstreampoint negative drive
30	DP	I/O	USB upstreampoint positive drive

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3.1 Pin Description, continued

40 DIP PIN#	NAME	TYPE	DESCRIPTION
31	VDD3	OUTPUT	3.3V input for USB bus drive
32	P07/ KBSO7	OUTPUT	Keyscan output
33	P06/ KBSO6	OUTPUT	Keyscan output
34	P05/ KBSO5	OUTPUT	Keyscan output
35	P04/ KBSO4	OUTPUT	Keyscan output
36	P03/ KBSO3	OUTPUT	Keyscan output
37	P02/ KBSO2	OUTPUT	Keyscan output
38	P01/ KBSO1	OUTPUT	Keyscan output
39	P00/ KBSO0	OUTPUT	Keyscan output
40	VDD	POWER	5V supply

* In 40 pin configuration,P34,P35 are shared by LED drive and Scanout function.

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FUNCTIONAL DESCRIPTION

First In First Out Storage (FIFO'S) Organization

The W81C280 has six FIFO's, one for receiving and five for transmitting.

FIFO or SRAM	SIZE (Byte)	NOTES
Endpt 0 Receiving	16	Data received on upstream port which contains the correct address and pids will be stored here for the CPU core to read.
Endpt 0 Transmitting	16	The CPU core writes the data here which will be sent to the host when the correct address and pids are transmitted by the host.
Endpt 1 Transmitting	16	The CPU core writes the data here which will be sent to the host when the correct address and pids are transmitted by the host.
Endpt 2 Transmitting	16	The CPU core writes the data here which will be sent to the host when the correct address and pids are transmitted by the host.
Endpt 3 Transmitting	16	The CPU core writes the data here which will be sent to the host when the correct address and pids are transmitted by the host.
Endpt 4 Transmitting	16	The CPU core writes the data here which will be sent to the host when the correct address and pids are transmitted by the host.

INTERFACE TO THE MICROCONTROLLER:

The FIFOs communicate with the CPU core via a 2-wire serial bus. One signal is the data (P30/MDA) and the other is the clock (P31/MCL). The clock is always generated by the CPU core. The data is bi-directional. After each byte of data (MSB first) an acknowledge bit (MDA=0) is sent by the receiver. The CPU core always initiates the communication with a start condition (MDA from 1 change to 0 while MCL=1) and the FIFO's address. The CPU core ends the transmission with a stop condition (MDA from 0 change to 1 while MCL=1). Data is always changed while MCL=0 and clocked in on the rising edge of MCL. The FIFO acts as a slave memory device at address E8h.

the serial BUS•• ADDRESS	READ FROM FIFO	WRITE TO FIFO
1110 100S	S=1	S=0

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The format for describing the interface to the FIFO is as follows:

ST = Start (MDA from 1 change to 0 while MCL=1)

AW = An acknowledge given by the FIFO Interface (the FIFO Interface brings MDA=0 during the 9th MCL pulse.)

AU = An acknowledge given by the CPU core (the CPU core brings MDA=0 during the 9th MCL pulse.)

NA = No acknowledge (this signifies the end of data being read from the FIFO Interface.)

SP = Stop (MDA from 0 change to 1 while MCL=1)

For example, for the CPU core to read the USB Interface's Status Register0 only and the value is E9h••

ST	11101001	AW	SR0 (8)	NA	SP

ST= Start AW= FIFO Interface Acknowledge

AU= CPU core Acknowledge

NA= No Acknowledge

SP= Stop

11101001= the serial bus's Read Address

SR0 (8) = Status Register 0 (8 bits) (MSB 1st)

Internal interrupts

The interrupt (P3.7 in CPU core) will be enabled and disabled under the following actions:

ENABLE INTERRUPT	DISABLE INTERRUPT
Resume	After the CPU core reads the Status Registers.
Endpoint 1 - 4 Handshake ACK received	After Status Registers are read.
Endpoint 0 data received	After the CPU core reads the Status Registers.
Turnaround time-out	After the CPU core reads the Status Registers.
Suspend (no activity) on the USB bus	After the CPU core reads the Status Registers.
Reset sent from upstream	After the CPU core reads the Status Registers.

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Reacting To The Internal interrupts

Since there is no condition which requires immediate attention by the CPU core, the NINT pin does not necessarily have to be used. The CPU core can access the W81C280 in following alternative way:

- Have the P3.7 to be an interrupt pin in the CPU core and read the W81C280 Status registers when it is enabled.

Reset

The W81C280 supports three types of reset. During a reset, all registers of the CPU core and USB return to their default status, and USB device address is set to zero.

External Reset

As in 8051 series controller, the external RESET signal is sampled at S5P2. To take effect, it must be held high at least two machine cycles while the oscillator is running.

An internal trigger circuit in the reset line is used to deglitch the reset line. The reset logic also has a special glitch remocal circuit that ignores glitches on the reset line.

During reset, the ports are initialized to FFH, the stack pointer to 07H, PCON(with exception of bit 4) to 00H, and all of the other SFR registers except SBUF to 00H. SBUF is not reset.

Warm Reset

W81C280 provides a warm reset by programming a ••• to bit 6 of control register 0.

USB Reset

The W81C280 handles the USB reset function independently from the CPU core. If a Single Ended Zero (SE0) is detected on the upstream port for greater then 2.5us, then the interrupt is enabled. The CPU core read flag from bit2 of status register 0 and t reset the device address to 0, and enter the active state.

USB SUSPEND

If there is no upstream activity for 3msec then the SUSPEND flag is set and the interrupt enabled. When SUSPEND flag is read by CPU core, The W81C280 go into suspend

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USB RESUME:

The suspend mode can be disabled by a 'resume'. The resume can occur by four methods.

- The host can send a resume to all ports by placing a 0 (K state) on the bus. The W81C280 sees the resume, disables the SUSPEND flag, and enables the interrupt. In this case, the CPU core does not have to perform any functions.
- The host can reset the bus.
- When any key in Keyboard is press The CPU core can initiate a resume by setting URESUME in the Control Register which will cause a K state to be sent. To un-resume, the CPU core must clear the URESUME bit in the Control Register.

FULL/LOW SPEED DEVICE DETECTION:

The W81C280 detects if upstream port is full speed (FS) or low speed (LS) and sets the appropriate flag. the CPU core has to configure it as a FS or LS device

ELECTRICAL CHARACTERISTICS & CAPACITANCE

(Ta = 0••to + 70••, VDD = +5V ± 5%)

SYMBOL	DESCRIPTION	MIN.	TYP.	MAX.	UNIT	NOTE
VDD	Power Support	4.75	5.0	5.25	V	
VIL	Input Low Voltage(except RESET)			0.8	V	
VIL1	Input Low Voltage(RESET)			0.6	V	
VIH1	Input High Voltage(except RESET)	2.0			V	
VIH2	Input High Voltage(RESET)	3.5			V	
VOH	Output High Voltage(D0 ~ D7)			2.4	V	IOH=-4mA
VOL	Output Low Voltage(D0 ~ D7)	0.4			V	IOL= 4mA
IOFL	Output Leakage Current(D0 ~D7), High-Z state)	-10		10	uA	
IIH	Input Leakage Current	-10		10	uA	VDD=5.5V VIN=VDD
IIL	Input Leakage Current	-10		10	uA	VDD=5.5V VIN=VSS

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	Symbol	Conditions	Min	Max	Unit
Leakage Current:					
Hi-Z State Data Line Leakage	ILO	0 V < VIN < 3.3V	-10	+10	µA
Input Levels:					
Differential Input Sensitivity	VDI	|(D+)-(D-)|, and Figure 0-4	0.2		V
Differential Common Mode Range	VCM	Includes VDI range	0.8	2.5	V
Single Endge Receiver Threshold	VSE		0.8	2.0	V
Output Levels:					
Static Output Low	VOL	RL of 1.5kΩ to 3.6V		0.3	V
Static Output High	VOH	RL of 1.5kΩ to GND	2.8	3.6	V
Capacitance:					
Transceiver Capacitance	CIN	Pin to GND		20	pF
Driver Characteristics:					
Transition Time:					
Rise Time	TR	CL=50pF/350pF	75	300	ns
Fall Time	TF	CL=50pF/350pF	75	300	ns
Rise / Fall Time Matching	TRFM	(TR / TF)	80	120	%
Output Signal Crossover Voltage	VCRS		1.3	2.0	V
Data Source Timings:					
Low Speed Data Rate	TDRATE	Ave.Bit Rate(1.5Mb/s± 1.5%)	1.4775	1.5225	Mbs
Source Differential Driver Jitter					
To Next Transition	TDJ1		-95	95	ns
For Paired Transitions	TDJ2		-150	150	ns
Source EOP Width	TEOPT		1.25	1.50	µs
Differential to EOP transition Skew	TDEOP		-40	100	ns
Receiver Data Jitter Tolerance					
To Next Transition	TJR1		-75	75	ns
For Paired Transitions	TJR2		-45	45	ns
EOP Width at receiver					
Must reject as EOP	TEORP1		330		ns
Must accept as EOP	TEOPR2		675		ns

USB KEYBOARD SAMPLE APPLICATION

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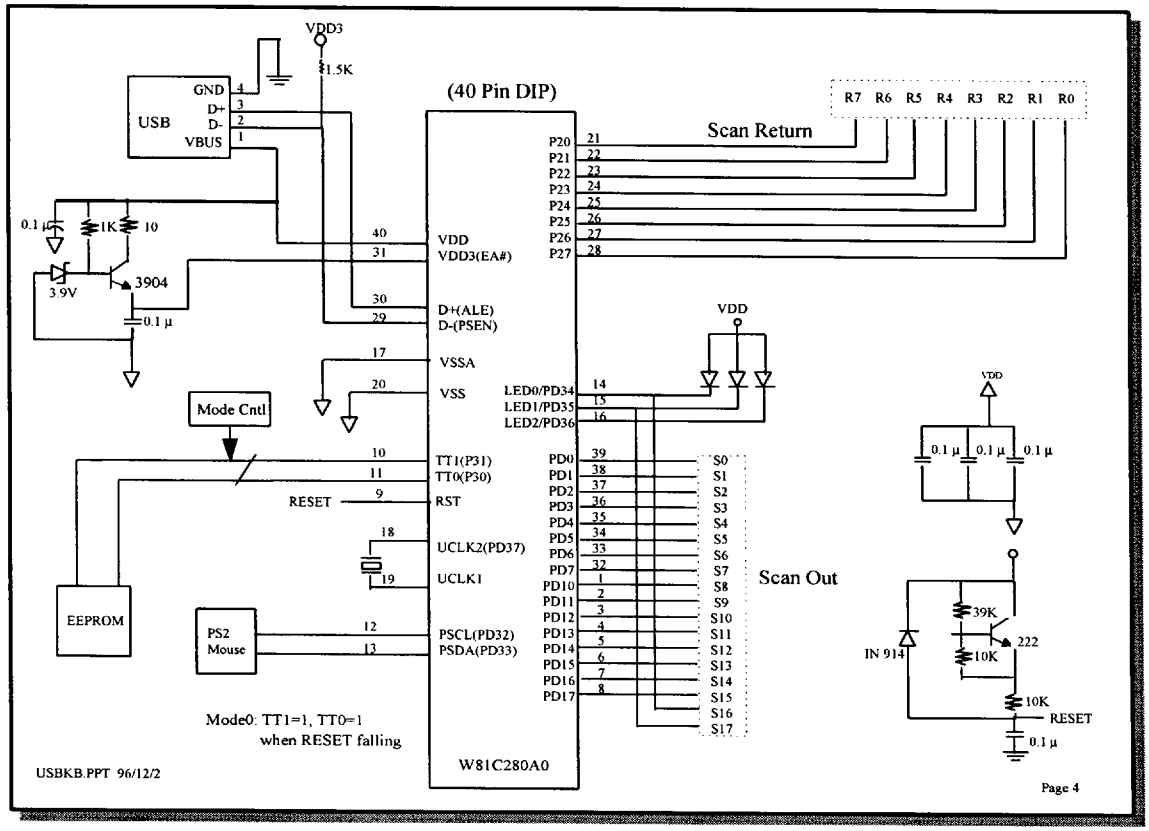

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