STK25C48

CMOS nvSRAM
2K x 8 High Performance
AutoStore™ Nonvolatile Static RAM

FEATURES

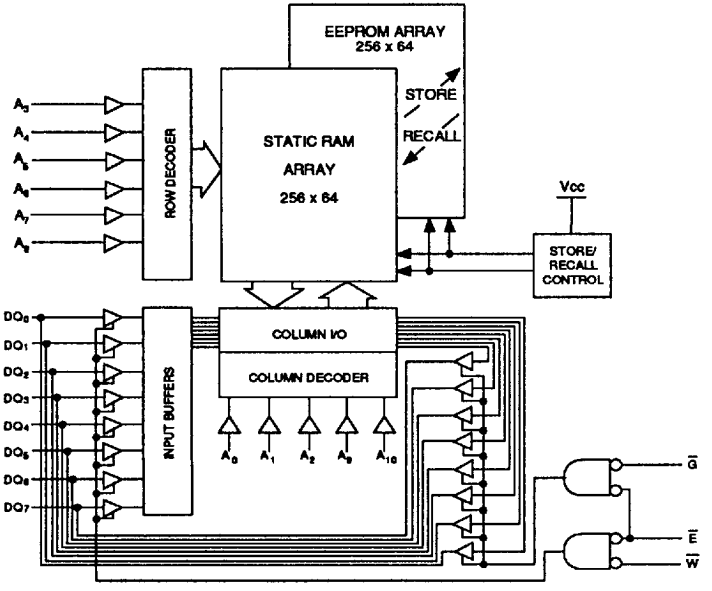
- **30, 35 and 45ns Access Times**
- **15 mA I_{CC} at 200ns Access Speed**
- **Automatic *STORE* to EEPROM on Power Down**
- **Unlimited SRAM Read and Write Cycles**
- **100,000 *STORE* cycles to EEPROM**
- **10 year data retention in EEPROM**
- **Automatic *RECALL* on Power Up**
- **Unlimited *RECALL* cycles from EEPROM**
- **Single 5V±10% Operation**
- **Commercial and Industrial Temperatures**

DESCRIPTION

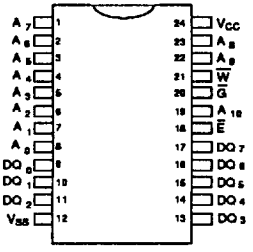
The Simtek STK25C48 is a fast static RAM (30, 35 and 45ns), with a nonvolatile EEPROM element incorporated in each static memory cell. The SRAM can be read and written an unlimited number of times, while independent nonvolatile data resides in EEPROM. Data transfers from the SRAM to the EEPROM (the *STORE* operation) take place automatically upon power down. Transfers from the EEPROM to the SRAM (the *RECALL* operation) take place automatically on power up.

The STK25C48 is available in a 24-pin 600 mil plastic DIP package.

LOGIC BLOCK DIAGRAM



PIN CONFIGURATIONS



24 - 600 PDIP

PIN NAMES

A_0 - A_{10}	Address Inputs
$\overline{W}$	Write Enable
DQ_0 - DQ_7	Data In/Out
$\overline{E}$	Chip Enable
$\overline{G}$	Output Enable
V_{CC}	Power (+5V)
V_{SS}	Ground

ABSOLUTE MAXIMUM RATINGS[a]

Voltage on typical input relative to V_{SS} ..... –0.6V to 7.0V
Voltage on DQ_{0-7} and $\overline{G}$ ..... –0.5V to (V_{CC}+0.5V)
Temperature under bias ..... –55°C to 125°C
Storage temperature ..... –65°C to 150°C
Power dissipation 1W
DC output current 15mA
(One output at a time, one second duration)

Note a: Stresses greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only, and functional operation of the device at conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

DC CHARACTERISTICS

(V_{CC} = 5.0V ± 10%)

SYMBOL	PARAMETER	COMMERCIAL		INDUSTRIAL		UNITS	NOTES
		MIN	MAX	MIN	MAX		
I_{CC_1}[b]	Average V_{CC} Current		85		95	mA	t_{AVAV} = 30ns
			80		85	mA	t_{AVAV} = 35ns
			75		80	mA	t_{AVAV} = 45ns
I_{CC_2}[b]	Average V_{CC} Current at t_{AVAV} = 200ns		15		15	mA	All inputs ≤ 0.2V or ≥ (V_{CC} - 0.2V)
I_{CC_3}	Average V_{CC} Current during AutoStore™ Cycle		4		4	mA	$\overline{E}$ ≤ 0.2V, $\overline{W}$ ≥ (V_{CC} – 0.2V) others ≤ 0.2V or ≥ (V_{CC} – 0.2V)
I_{SB_1}	Average V_{CC} Current (Standby, Cycling TTL Input Levels)		35		39	mA	t_{AVAV} = 30ns
			32		35	mA	t_{AVAV} = 35ns
			28		32	mA	t_{AVAV} = 45ns $\overline{E}$ ≥ V_{IH}; all others cycling
I_{SB_2}[c]	Average V_{CC} Current (Standby, Stable CMOS Input Levels)		3		3	mA	$\overline{E}$ ≥ (V_{CC} – 0.2V) all others V_{IN} ≤ 0.2V or ≥ (V_{CC} – 0.2V)
I_{ILK_3}	Input Leakage Current (Any Input)		±1		±1	µA	V_{CC} = max V_{IN} = V_{SS} to V_{CC}
I_{OLK}	Off State Output Leakage Current		±5		±5	µA	V_{CC} = max V_{OUT} = V_{SS} to V_{CC}
V_{IH}	Input Logic "1" Voltage	2.2	V_{CC}+.5	2.2	V_{CC}+.5	V	All Inputs
V_{IL}	Input Logic "0" Voltage	V_{SS}–.5	0.8	V_{SS}–.5	0.8	V	All Inputs
V_{OH}	Output Logic "1" Voltage	2.4		2.4		V	I_{OUT} = –4mA
V_{OL}	Output Logic "0" Voltage		0.4		0.4	V	I_{OUT} = 8mA
T_A	Operating Temperature	0	70	-40	85	°C	

Note b: I_{CC_1} and I_{CC_2} are dependent on output loading and cycle rate. The specified values are obtained with outputs unloaded.
Note c: Bringing $\overline{E}$ ≥ V_{IH} will not produce standby current levels until any nonvolatile cycle in progress has timed out. See MODE SELECTION table.

AC TEST CONDITIONS

Input Pulse Levels ..... V_{ss} to 3V
Input Rise and Fall Times ..... ≤ 5ns
Input and Output Timing Reference Levels 1.5V
Output Load ..... See Figure 1

CAPACITANCE[d] (T_A=25°C, f=1.0MHz)

SYMBOL	PARAMETER	MAX	UNITS	CONDITIONS
C_{IN}	Input Capacitance	8	pF	ΔV = 0 to 3V
C_{OUT}	Output Capacitance	7	pF	ΔV = 0 to 3V

Note d: These parameters are guaranteed but not tested.

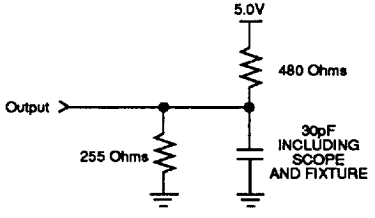


Figure 1: AC Output Loading

SRAM MEMORY OPERATION

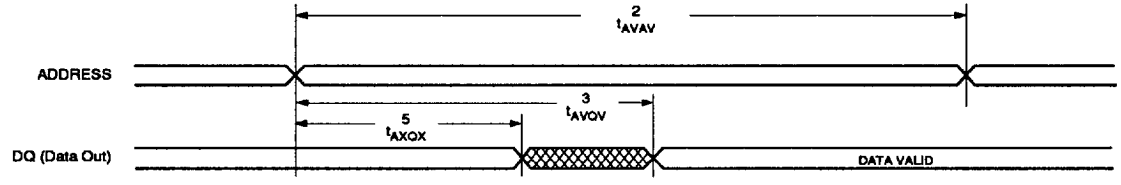
READ CYCLES #1 & #2

(V_{CC} = 5.0V ± 10%)

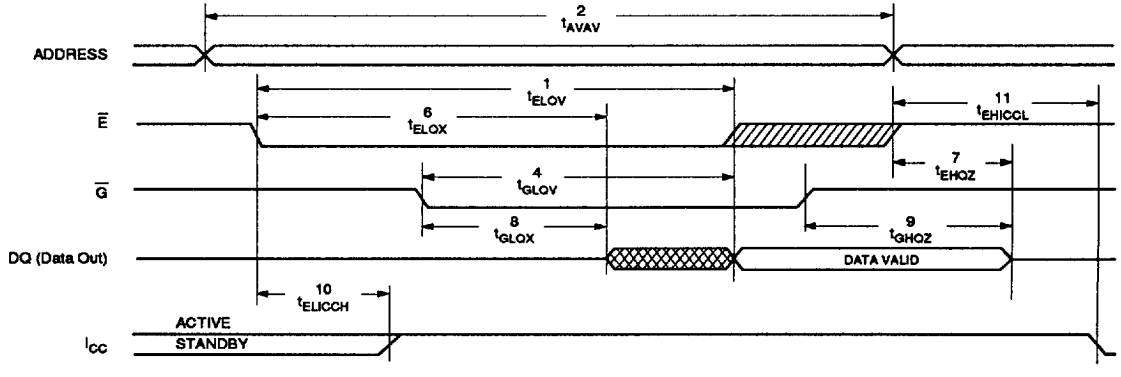
NO.	SYMBOLS		PARAMETER	STK25C48-30		STK25C48-35		STK25C48-45		UNITS
	#1, #2	Alt.		MIN	MAX	MIN	MAX	MIN	MAX	
1	t_{ELQV}	t_{ACS}	Chip Enable Access Time		30		35		45	ns
2	t_{AVAV}	t_{RC}	Read Cycle Time	30		35		45		ns
3	t_{AVQV}[g]	t_{AA}	Address Access Time		30		35		45	ns
4	t_{GLQV}	t_{OE}	Output Enable to Data Valid		15		20		25	ns
5	t_{AXQX}	t_{OH}	Output Hold After Address Change	5		5		5		ns
6	t_{ELQX}	t_{LZ}	Chip Enable to Output Active	5		5		5		ns
7	t_{EHQZ}[h]	t_{HZ}	Chip Disable to Output Inactive		15		17		20	ns
8	t_{GLQX}	t_{OLZ}	Output Enable to Output Active	0		0		0		ns
9	t_{GHQZ}[h]	t_{OHZ}	Output Disable to Output Inactive		15		17		20	ns
10	t_{ELICCH}[g]	t_{PA}	Chip Enable to Power Active	0		0		0		ns
11	t_{EHICCL}[g]	t_{PS}	Chip Disable to Power Standby		30		35		45	ns

Note e: Parameter guaranteed but not tested.
Note f: For READ CYCLE #1 and #2, $\overline{W}$ is high for entire cycle.
Note g: Device is continuously selected with $\overline{E}$ low and $\overline{G}$ low.
Note h: Measured ± 200mV from steady state output voltage.

READ CYCLE #1 [g,h]



READ CYCLE #2 [g]



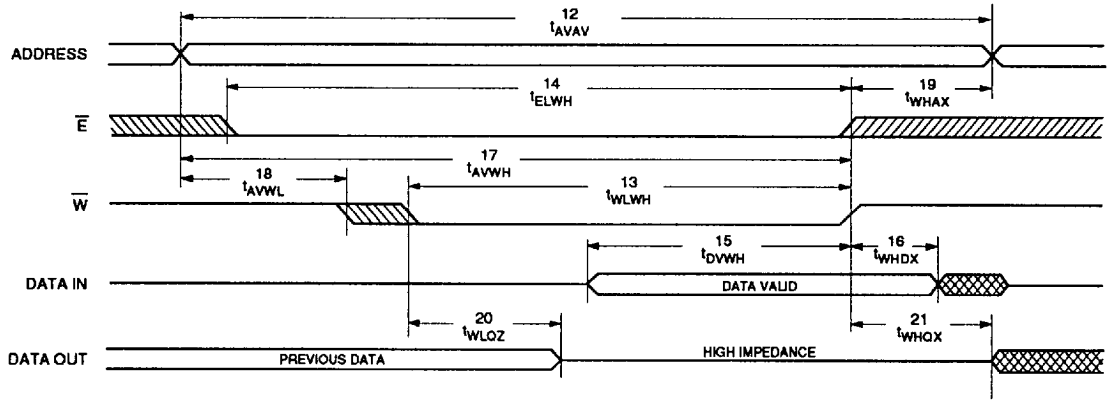
WRITE CYCLES #1 & #2

(V_{CC} = 5.0V ± 10%)

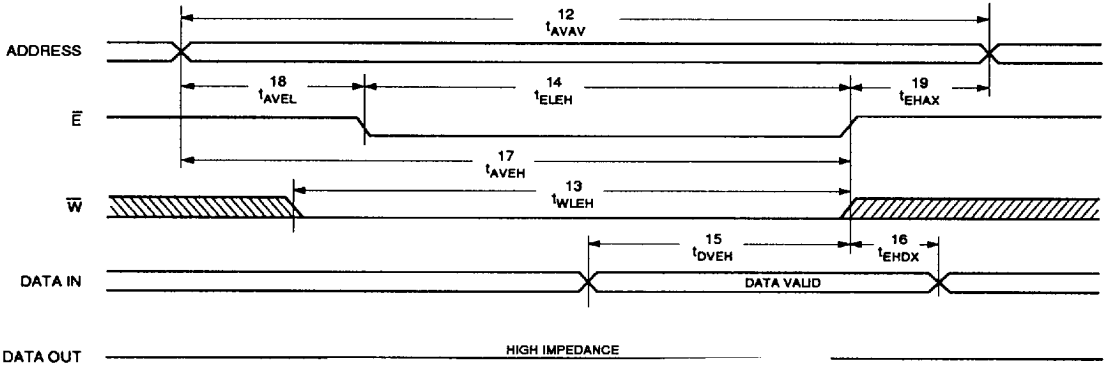
NO.	SYMBOLS			PARAMETER	STK25C48-30		STK25C48-35		STK25C48-45		UNITS
	#1	#2	Alt.		MIN	MAX	MIN	MAX	MIN	MAX	
12	t_{AVAV}	t_{AVAV}	t_{WC}	Write Cycle Time	30		35		45		ns
13	t_{WLWH}	t_{WLEH}	t_{WP}	Write Pulse Width	25		30		35		ns
14	t_{ELWH}	t_{ELEH}	t_{CW}	Chip Enable to End of Write	25		30		35		ns
15	t_{DVWH}	t_{DVEH}	t_{DW}	Data Set-up to End of Write	15		18		20		ns
16	t_{WHDX}	t_{EHDX}	t_{DH}	Data Hold After End of Write	0		0		0		ns
17	t_{AVWH}	t_{AVEH}	t_{AW}	Address Set-up to End of Write	25		30		35		ns
18	t_{AVWL}	t_{AVEL}	t_{AS}	Address Set-up to Start of Write	0		0		0		ns
19	t_{WHAX}	t_{EHAX}	t_{WR}	Address Hold After End of Write	0		0		0		ns
20	t_{WLQZ}[h,j]		t_{WZ}	Write Enable to Output Disable		15		17		20	ns
21	t_{WHQX}		t_{OW}	Output Active After End of Write	5		5		5		ns

Note h: Measured ±200mV from steady state output voltage.
Note i: $\overline{E}$ or $\overline{W}$ must be ≥V_{IH} during address transitions.
Note j: If $\overline{W}$ is low when $\overline{E}$ goes low, the outputs remain in the high impedance state.

WRITE CYCLE #1: $\overline{W}$ CONTROLLED[j]



WRITE CYCLE #2: $\overline{E}$ CONTROLLED[j]



NONVOLATILE MEMORY OPERATION

MODE SELECTION

$\overline{E}$	$\overline{W}$	$\overline{G}$	MODE	I/O	POWER
H	X	X	Not Selected	Output High Z	Standby
L	H	L	Read SRAM	Output Data	Active
L	L	X	Write SRAM	Input Data	Active
L	H	H	No Operation	High Z	Active

AUTOSTORE™ AND POWER-UP RECALL

NO.	SYMBOLS	PARAMETER	MIN	MAX	UNITS	NOTES
22	t_{RECALL}	*RECALL* Cycle Duration		20	µs	Note k
23	$t_{POSTORE}$	Power Down *STORE* Duration		10	ms	
	V_{SWITCH}	Low Voltage Trigger Level	4.0	4.5	V	

Note k: A RECALL cycle is initiated automatically at power up when V_{CC} exceeds V_{SWITCH}. t_{RECALL} is measured from the point at which V_{CC} exceeds 4.5V.

DEVICE OPERATION

The STK25C48 has two separate modes of operation: SRAM mode and nonvolatile mode. In SRAM mode, the memory operates as a standard fast static RAM. In nonvolatile mode, data is transferred from SRAM to EEPROM (the *STORE* operation) or from EEPROM to SRAM (the *RECALL* operation). In this mode SRAM functions are disabled.

STORE cycles are automatically initiated when the power supply voltage level of the chip falls below V_{SWITCH}. *RECALL* operations are automatically initiated upon power-up and whenever the power supply voltage level rises above V_{SWITCH}.

SRAM READ

The STK25C48 performs a READ cycle whenever $\overline{E}$ and $\overline{G}$ are LOW and $\overline{W}$ is HIGH. The address specified on pins A_{0-10} determines which of the 2048 data bytes will be accessed. When the READ is initiated by an address transition, the outputs will be valid after a delay of t_{AVQV}. If the READ is initiated by $\overline{E}$ or $\overline{G}$, the outputs will be valid at t_{ELQV} or at t_{GLQV}, whichever is later. The data outputs will repeatedly respond to address changes within the t_{AVQV} access time without the need for transitions on any control input pins, and will remain valid until another address change or until $\overline{E}$ or $\overline{G}$ is brought HIGH or $\overline{W}$ is brought LOW.

SRAM WRITE

A write cycle is performed whenever $\overline{E}$ and $\overline{W}$ are LOW. The address inputs must be stable prior to entering the WRITE cycle and must remain stable until either $\overline{E}$ or $\overline{W}$ go HIGH at the end of the cycle. The data on pins DQ_{0-7} will be written into the memory if it is valid t_{DVWH} before the end of a $\overline{W}$ controlled WRITE or t_{DVEH} before the end of an $\overline{E}$ controlled WRITE.

It is recommended that $\overline{G}$ be kept HIGH during the entire WRITE cycle to avoid data bus contention on the common I/O lines. If $\overline{G}$ is left LOW, internal circuitry will turn off the output buffers t_{WLQZ} after $\overline{W}$ goes LOW.

During power-up, or after any low power condition (V_{CC} < V_{SWITCH}), when V_{CC} exceeds the sense voltage of V_{SWITCH}, a *RECALL* cycle will automatically be initiated. After the initiation of this automatic *RECALL*, if V_{CC} falls below V_{SWITCH}, then another *RECALL* operation will be performed whenever V_{CC} again rises above V_{SWITCH}.

AUTOMATIC *STORE* OPERATION

The STK25C48 AutoStore™ nvSRAM continuously monitors V_{CC}. When V_{CC} drops below V_{SWITCH} (and an SRAM WRITE has occured since power-up), the part will automatically perform a *STORE* operation,

saving the data into the EEPROM. *Figure 1* illustrates the timing of the *AutoStore™* cycle. V_{CC} to the STK25C48 must not fall below 3.6V before the AutoStore™ cycle is complete (t_{STORE}). In order to prevent unneeded STORE operations, automatic STORE will not occur unless at least one WRITE operation has taken place since power-up.

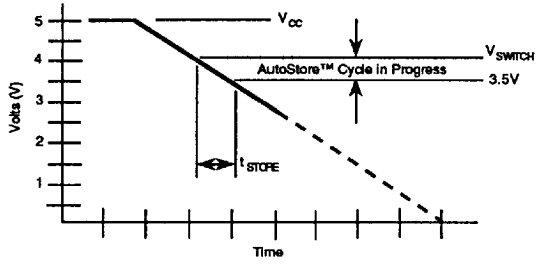


Figure 1
AutoStore™ Cycle Timing Diagram

Note: On power-up, as soon as the STK25C48 completes the power-up recall, it becomes an SRAM; if $\overline{E}$ and $\overline{W}$ are both low the address on the inputs will be written to, corrupting the recalled data. If V_{CC} bounces below V_{SWITCH}, the part will AutoStore™ this corrupted SRAM data.

IMPLEMENTATION

Normally, the STK25C48 relies on the system V_{CC} remaining between V_{SWITCH} (min) and 3.6V for the STORE time, t_{STORE}. In the unusual case that the system power supply decays too quickly (not remaining between V_{SWITCH} (min) and 3.6V for at least 10ms), a possible alternative implementation is shown in *Figure 2*. The capacitor charge will hold up the DUT V_{CC} long enough for the AutoStore™ to occur. However, from a system point of view, the 0.3V drop across the diode will effectively cause the V_{SWITCH} value to be 0.3V higher; the part could do an AutoStore™ when the system V_{CC} is as high as V_{SWITCH} (max) + 0.3V. Note that the STK25C48 is a high speed memory and therefore must have a high frequency bypass capacitor of approximately 0.1µF connected between DUT V_{CC} and V_{SS}, using leads and traces that are as short as possible. As with all high speed CMOS ICs, normal careful routing of power, ground and signals will help prevent noise problems.

LOW AVERAGE ACTIVE POWER

The STK25C48 has been designed to draw significantly less power when $\overline{E}$ is LOW (chip enabled) but the access cycle time is longer than 55ns. *Figure 3* below shows the relationship between I_{CC} and access times for READ cycles. All remaining inputs are assumed to cycle, and current consumption is given for all inputs at CMOS or TTL levels, over the commercial temperature range. *Figure 4* shows the same relationship for WRITE cycles. When $\overline{E}$ is HIGH, the chip consumes only standby currents and these plots do not apply.

The cycle time used in *Figure 3* corresponds to the length of time from the later of the last address transition or $\overline{E}$ going LOW to the earlier of $\overline{E}$ going HIGH or the next address transition. $\overline{W}$ is assumed to be HIGH, while the state of $\overline{G}$ does not matter. Additional current is consumed when the address lines change state while $\overline{E}$ is asserted. The cycle time used in *Figure 4* corresponds to the length of time from the later of $\overline{W}$ or $\overline{E}$ going LOW to the earlier of $\overline{W}$ or $\overline{E}$ going HIGH.

The overall average current drawn by the part depends on the following items: 1) CMOS or TTL input levels; 2) the time during which the chip is disabled ($\overline{E}$ HIGH); 3) the cycle time for accesses ($\overline{E}$ LOW); 4) the ratio of reads to writes; 5) the operating temperature and; 6) the V_{CC} level.

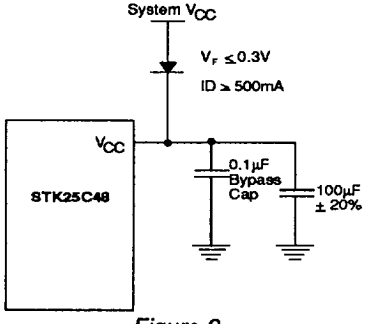


Figure 2
Alternate AutoStore™ Implementation Circuit if V_{CC} decays too quickly

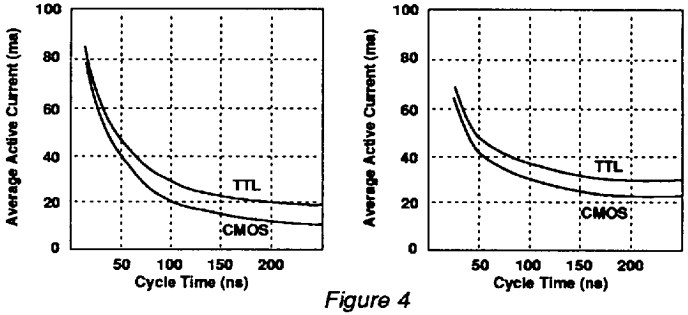


Figure 4
I_{CC} (Max) Writes

Note: Typical at 25°C

ORDERING INFORMATION