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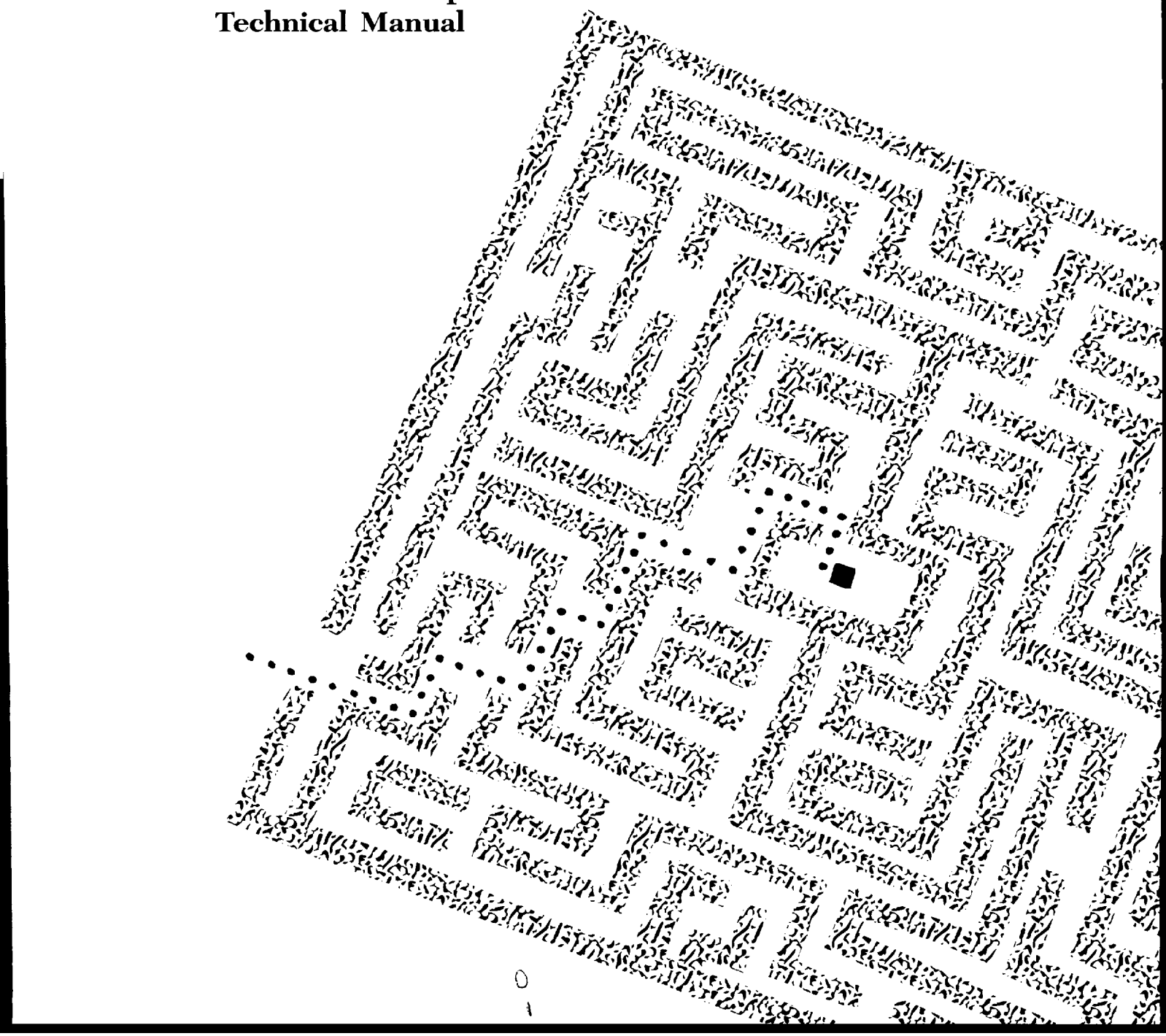
L64863
Clock Chip
Technical Manual



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Preface

The SparKIT™ family of chipsets from LSI Logic makes designs of SPARC-compatible RISC workstations straightforward. This book is the primary reference and user's manual for the L64863 Clock Chip, which is a part of the SparKIT-40/SS10 chipset. This book contains a complete functional description for the L64863 with physical and electrical specifications.

Audience

This book assumes that you have some familiarity with microprocessors and related support devices. The people who benefit from this book are:

- Engineers and managers who are evaluating the processor for possible use in a system
- Engineers who are designing the processor into a system

Organization

This book has the following chapters:

- Chapter 1 **Introduction**
- Chapter 2 **Overview**
- Chapter 3 **Signal Descriptions**
- Chapter 4 **Specifications**

Related Publications

The SBus Specification, Revision B, available from Sun Microsystems, Inc., 2550 Garcia Avenue, Mountain View, CA 94042

SPARC Architecture Manual, Version 7, Order Number L64811AM from LSI Logic

L64854 SBus DMA2 Controller (DMA2) Technical Manual, part number M14020, from LSI Logic

L64860 Error Correcting Memory Controller (EMC) Technical Manual, order number M14021, from LSI Logic

L64861 SBus to EBus I/O Controller (SEC) Technical Manual, order number M14022, from LSI Logic

L64862 Mbus to SBus Interface Chip (MSI) Technical Manual, order number M 14023, from LSI Logic

Serial Communication Controller (AMD, 85C30) 07513C

Digital Subscriber Controller DSC (AMD, 79C30) 09456-1B

Microprocessor and Peripheral Handbook Volume 2 (Intel, 82077AA)

In addition to the above, the *SparKIT-40/SS10 System User's Manual*, part number MS71-000121-99 A, from LSI Logic, is available as part of the SparKIT-40/SS10 design kit.

Conventions Used in this Manual

The following signal naming conventions are used throughout this manual:

- A level-significant signal that is true or valid when the signal is LOW has an overbar ($\overline{\quad}$) over its name or is followed by an underbar (MAS_).
- An edge-significant signal that initiates actions on a HIGH-to-LOW transition always has an overbar ($\overline{\quad}$) over its name.

Hexadecimal numbers are indicated by the prefix "0x" before the number—for example, 0x32CF.

Contents

Tables

Chapter 1
Introduction

1.1 Introduction

The L64863 Clock Chip in the SparKIT-40/SS10 chipset generates clock signals for components on the SBus and Mbus. The clock chip also contains the JTAG circuitry and glue logic needed on the SparKIT-40/SS10 motherboard.

Each component in the system that requires either bus clock receives a separate clock line. Because each chip receives a separate clock line, the skew between clock lines is the sum of the skew between the output drivers of the Clock Chip and the trace skew. To minimize trace skew the clock traces to each chip are matched in delay. Both the SBus clock and the Mbus clock have a 50% duty cycle.

The skew requirement for the Mbus clocks is 1.5 ns between the Mbus clock signal at the die of any two receiver chips. It was not possible to generate the Mbus clocks in SparKIT-40/SS10 with such a low skew using standard CMOS components. SparKIT-40/SS10 design goals were to use low-power CMOS components where possible, which precluded using ECL clock drivers. A viable solution was to make a clock chip. Because the process and temperature of the drivers in the Clock Chip are all the same, the clock skew generated inside the Clock Chip is due mostly to the variations in metal trace lengths on the die. LSI routing programs can route trace lengths to within 50 ps of delay. Using such a CMOS Clock Chip, Mbus clock skew is then due mostly to variations of the following factors.

1. Trace impedance between the Mbus modules and the SparKIT-40/SS10 motherboard
2. Variations in the capacitive load on each clock line due to vias and component package variations
3. Trace length differences between the different clock traces

The trace lengths of the Mbus clocks on the motherboard are matched, so that the trace length variations are mostly due to differences between Mbus

Clock trace impedances on the SparKIT-40/SS10 motherboard and the Mbus modules. The clock skew because of variations in the trace impedances between the Mbus modules and the SparKIT-40/SS10 motherboard is 0.5 ns over process and temperature. Variation in the temperature of the drivers and the receivers can also produce another 0.5 ns of clock skew. Thus, with the SparKIT-40/SS10 Clock Chip, the Mbus clock skew can be held to 1.0 ns, which is 0.5 ns below the Mbus specification of 1.5 ns.

The Mbus to SBus Interface (MSI) chip has a skew requirement between the SBus clock and the Mbus clock of 2.5 ns. Because the SBus clocks and the Mbus clocks are generated from the same chip, and because the skew between the Mbus clocks is less than 1.5 ns, the skew between the Mbus and SBus clocks at the MSI is less than 1.5 ns, which is within the MSI specification for 2.5 ns skew between Mbus and SBus clocks.

The slew rate for the Mbus clocks is for 0.8 V to 2.0 V equal to 0.63 V/ns minimum and for 2.0 V to 0.8 V equal to 0.75 V/ns minimum. From zero-crossing to zero-crossing, the width of the active HIGH and LOW portion of the Mbus clock signal is 11 ns minimum and 14 ns maximum.

The grounds are separated at the corners of the die to prohibit ground noise from coupling between the two different clock output drivers.

Actual measured skew on the tester is 200 ps between any one clock output with respect to any other.

Figure 1.1 shows the devices on the SparKIT-40/SS10 motherboard and the clock signals sent to each. A legend that follows the figure gives the number of each device on the SBus and Mbus.

Figure 1.1
Motherboard
System Clocking

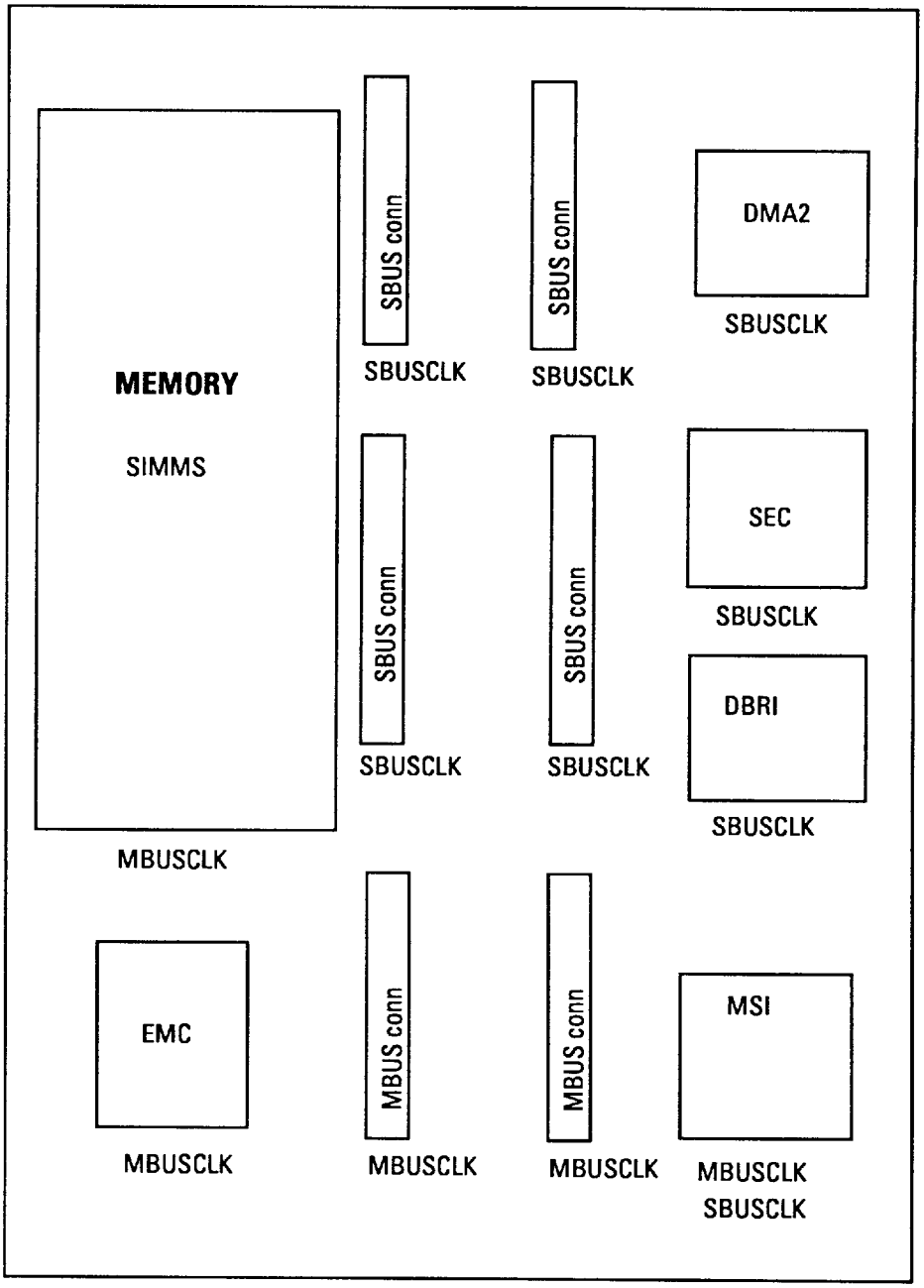


Figure 1.2 Number of Each Device

PART	*DEFINITION*	*QUANTITY*
Mbus Subsystem		
EMC	Mbus Memory Interface Chip	1
MSI	Mbus to SBus Interface Chip	1
Mbus connector	Mbus connector for modules	2
Memory SIMMs	Video SIMMs use the Mbus clock	4
SBus Subsystem		
SEC	Slow I/O Devices Interface Chip	1
MSI	Mbus to SBus Interface Chip	1
DMA2	DMA for SCSI & Ethernet Interface Chip	1
DBRI	ISDN with SBus interface	1
SBus connector	Mbus connector for modules	2

1.2 Features

The following features are incorporated into the Clock Chip.

- Generates 14 Mbus clock lines, four per module, one for the MSI, one for the EMC, four for the Video Simms.
- Generates six SBus clock lines, one for each pair of SBus slots, the SEC, DMA2, MSI, and DBRI.
- Generates Mbus and SBus clocks with less than 0.5-ns skew at the chip boundary.
- Contains the IEEE P.1149 JTAG standard master control circuitry.
- Contains global reset logic.

Chapter 2
Overview

2.1 Clock Chip

There are three basic modules that comprise the L64863 Clock Chip. They include the clock generators, the reset logic, and the JTAG control circuitry. Each of these modules is discussed in the following overview. The modules are presented in a block diagram in Figure 2.1. The Clock Generation tree is presented in Figure 2.2.

Figure 2.1 Clock Chip Block Diagram

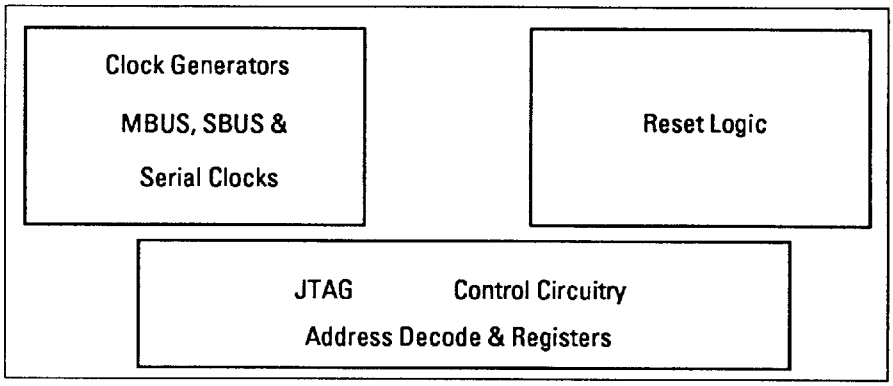
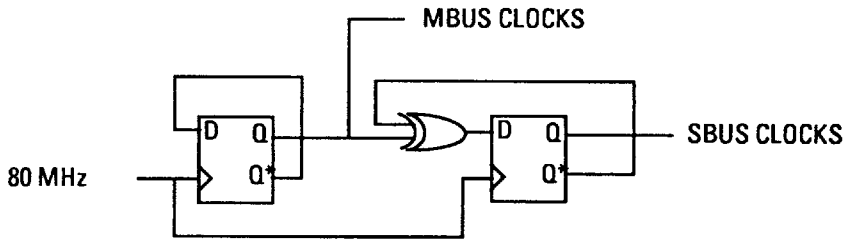


Figure 2.2 MBUS - SBUS Clock Generation Tree



2.2 Clock Generation

There are two clock inputs to the Clock Chip, the 80-MHz oscillator input (MOSC) and the external oscillator input (EXTOSC). The input oscillators are muxed using the MUXOSC input. None of these inputs is on the parametric chain.

The 80-MHz oscillator input is divided by two to produce the 40-MHz Mbus clock and then divided by two again to produce the 20-MHz SBus clock. The Mbus and SBus clocks are then driven to the center of the die by CLKI drivers on either side of a common clock net, which guarantees the skew between points on the common clock net to be less than 50 ps. From that center point, equal length traces are routed to the output drivers for the different copies of the Mbus clocks. In this manner the clock skew internal to the chip between Mbus clocks will be on the order of 100 ps. The same procedure is followed for the copies of the SBus clock.

The Mbus clocks are on one side of the chip and the SBus clocks are on the other side. The Mbus grounds are separated from the SBus grounds. This minimizes the ground bounce when the SBus clock is switching and the Mbus clock is not. There is a separate power and ground for each SBus and Mbus clock output.

The Mbus and SBus clocks run during reset, that is, the Mbus and SBus clocks are running while $\overline{\text{ResetOut}}$ is asserted. The relation among the two bus clock signals and the 80 MHz oscillator is shown in Figure 2.3.

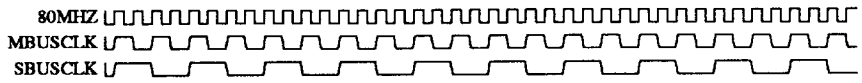


Figure 2.3 Mbus and SBus Timing

2.3 STOPCLOCK and STEPCLOCK Control

It is possible to stop and single step the Mbus and SBus clocks using the STOPCLOCK and STEPCLOCK inputs to the Clock Chip. Both STOPCLOCK and STEPCLOCK inputs to the Clock Chip are double-rank synchronized to the MOSC Clock Chip input, which runs at 80 MHz. STOPCLOCK simply stops the MOSC clock input to the divide-by-two and divide-by-four dividers in whatever phase MOSC was in. The Mbus and SBus clocks can also be stopped by a bit scanned into the JTAG Clock bypass bits. Then, while the Mbus/SBus clocks are running, SVTAS is turned on. This holds the transparent latch output of Mbus STOPCLOCK bit at its current value. The JTAG Clock is then turned on which loads the Mbus STOPCLOCK bit into the Clock Status register using SVTAS as the load enable. When SVTAS goes LOW the Mbus STOPCLOCK bit stops the Mbus clock. This method allows the JTAG Clock to be running continuously.

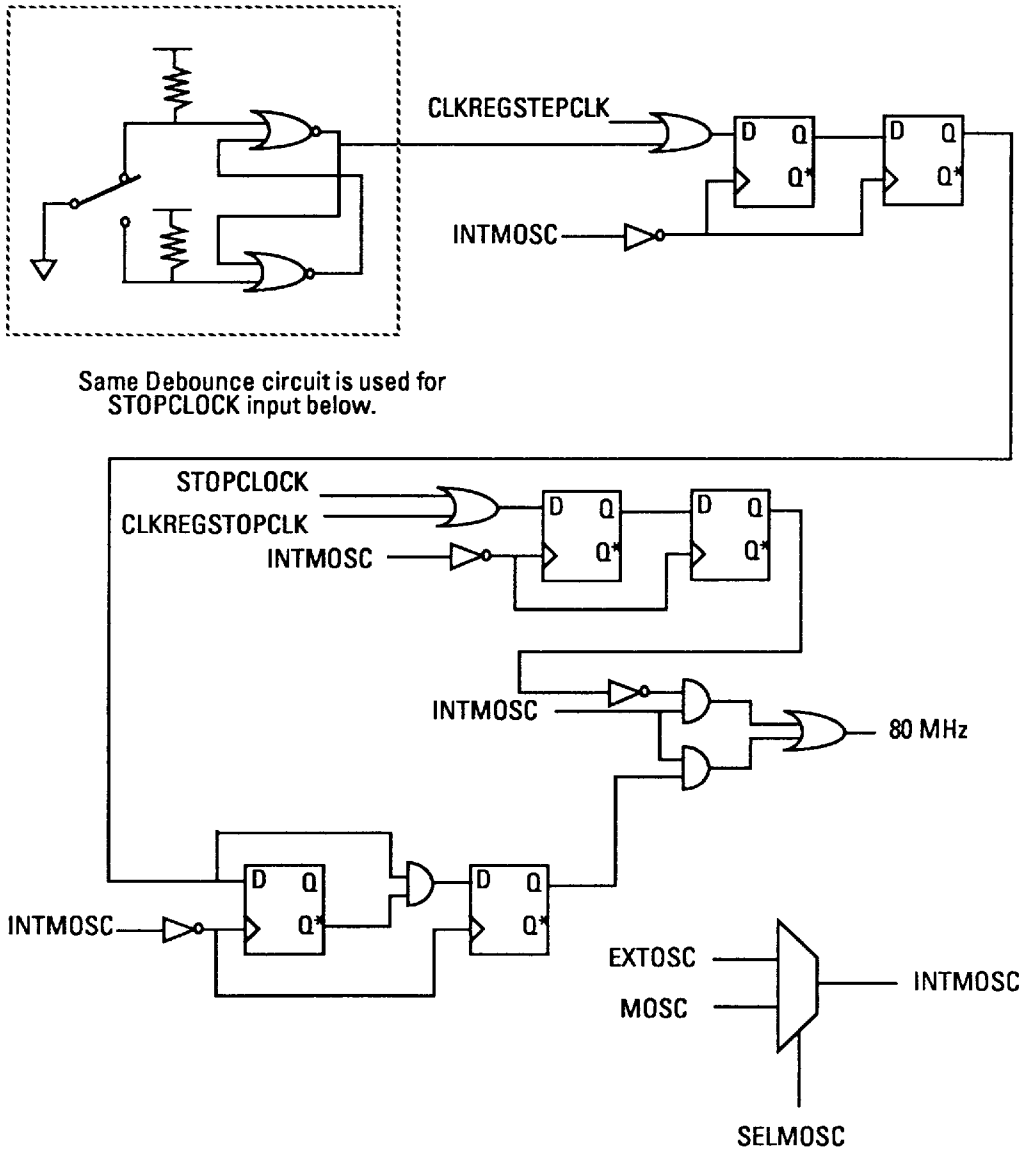
STEPCLOCK can be initiated by a push button input so that when the input goes HIGH, a single 80 MHz cycle is sent to the 80 MHz clock

dividers. This is accomplished by two flip-flops, functioning as a one-shot circuit. Each pulse of the STEPCLOCK input steps the 80 MHz Clock input to the clock dividers.

JTAGTMS is used to transition between the states of the JTAG state controller.

Circuits for STOPCLOCK and STEPCLOCK control signals are shown in Figure 2.4.

Figure 2.4
STOPCLOCK and
STEPCLOCK Control



2.4 Clock Status Register

The clock status resister has two read/write bits, StepClock and StopClock and two read only bits, Mbus_Clock_Phase and SBus_Clock_Phase. One can stop the clock and single step it to a state where the Mbus and SBus clocks are at any phase desired by using the two phase bits for the clocks and the control signals STEPCLOCK and STOPCLOCK.

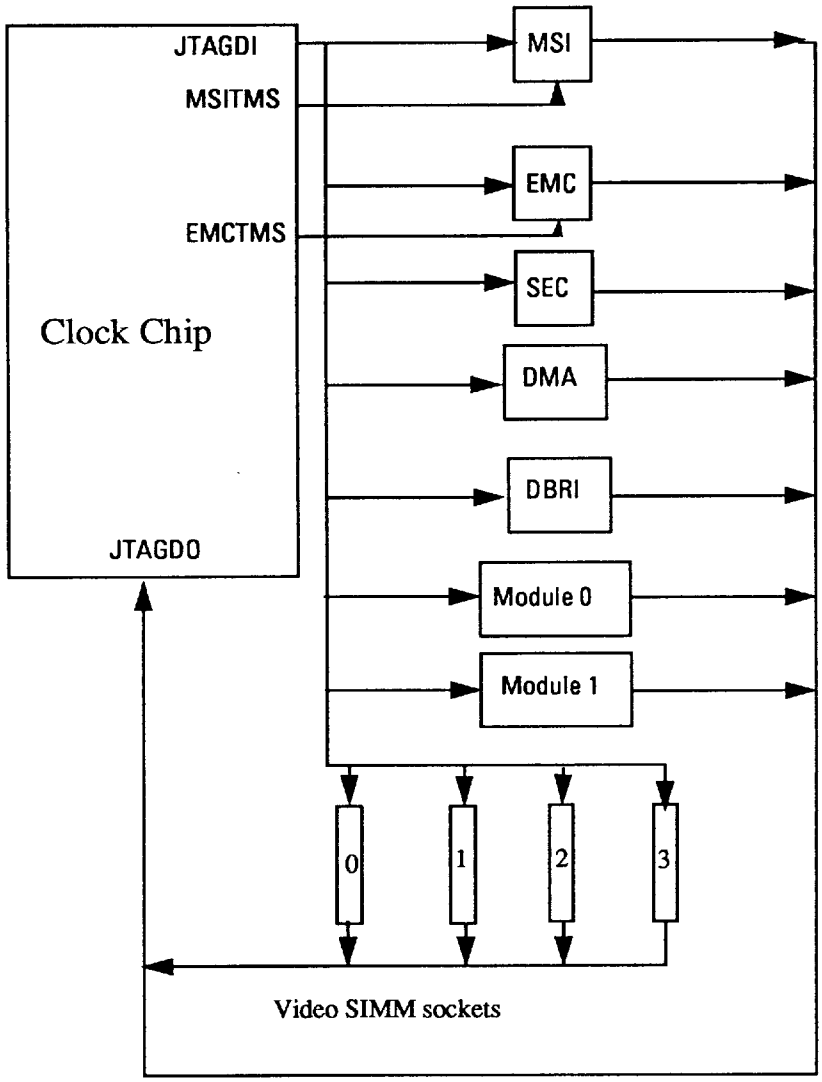
The clock status register is accessed just like any JTAG scan ring in the system; its address is zero. The JTAG scan ring is illustrated in Figure 2.5.

The bits of the clock status register are reset to zero after a reset is issued. The bit position in the register and name are shown in Table 2.1.

Table 2.1 Clock Status Register Bits

Bit	*Type*	*Function*
0	R/W	StopClock
1	R/W	StepClock
2	R	Phase of Mbus Clock
3	R	Phase of SBus Clock

Figure 2.5
Scan Ring Diagram



2.5 Scan Ring Addresses

Each part that has JTAG functionality is on a separate scan ring. Each scan ring is selected by having data sent to the scan ring on its own separate JTAGTMS line. Each JTAGTMS line is selected by decoding an address that is shifted into the Clock Chip when SVTAS is asserted HIGH. This

address is shifted into a shift register whose input is SVDI. When SVTAS is asserted, the TMS line that was selected before is active. When SVTAS is deasserted, the scan_address is released to the address decoder which is simultaneously enabled by the deassertion of SVTAS. The new address, that was shifted into the eight-bit address shift register, is output from the TMS decode unit when SVTAS is deasserted. The TMS decoder enables the separate JTAGTMS signals, which are AND'ed with the SVTMS signal and sent to the individual scan rings. Only one output of the TMS decode stage is active HIGH, the rest are LOW, which pegs the TMS line for the other rings at logic one. The TMS line that was selected as HIGH enables the NAND gate shown, to allow SVTMS data to pass to the scan ring selected. On reset, the JTAGTMS signals are asserted HIGH.

Hence the JTAG scan rings are all connected in parallel with the same JTAGDI and JTAGDO inputs. The addresses below are shown in terms of scan tool addressing.

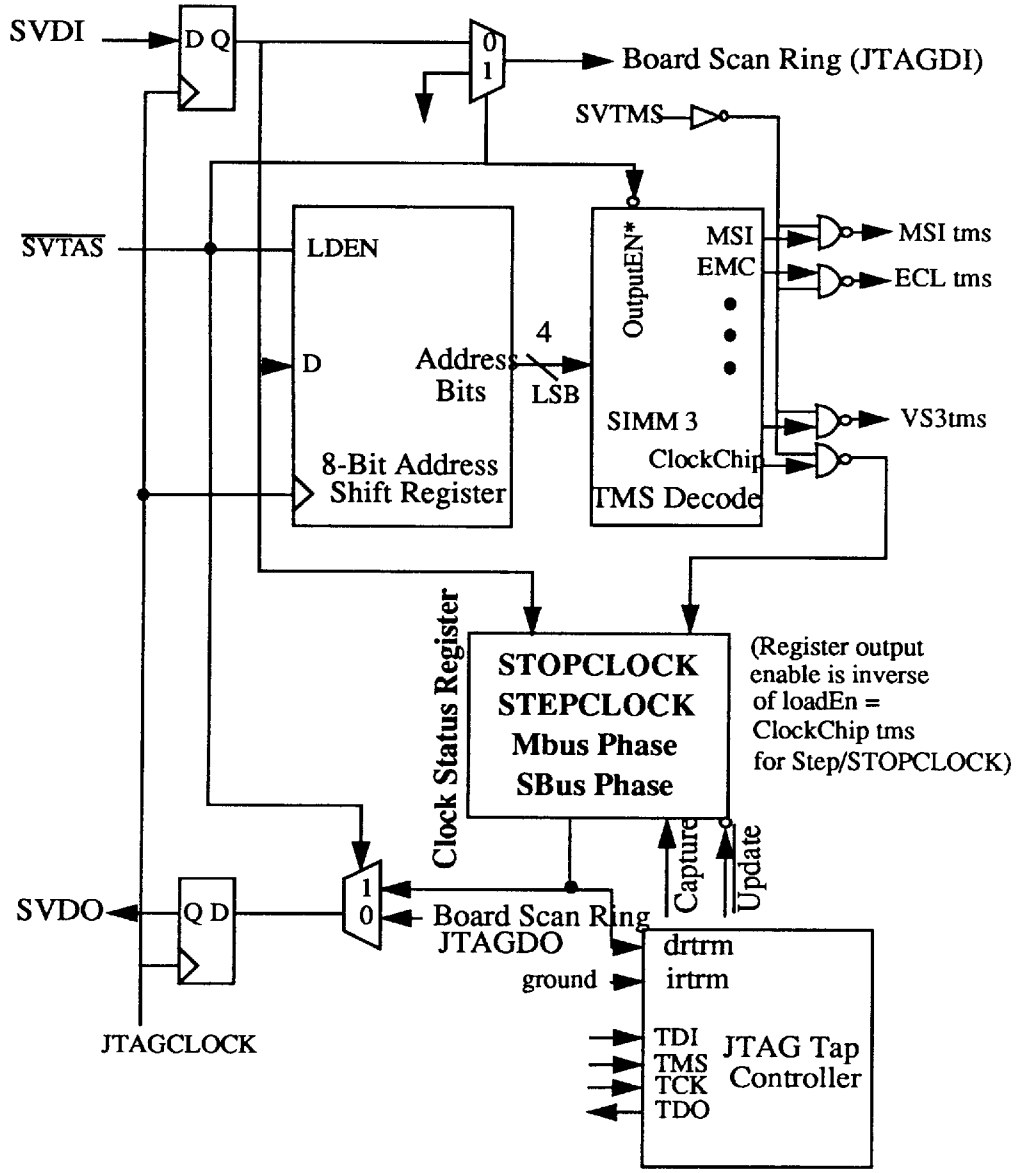
Ring	*Board Address (7:4)*	*Ring Address (3:0)*
ClockChip	0	0
MSI	4	0
EMC	2	0
SEC	6	0
DMA2	1	0
Mbus Module 0	5	0
Mbus Module 1	3	0
Video SIMM 0	7	0
Video SIMM 1	0	8
Video SIMM 2	4	8
Video SIMM 3	2	8
DBRI	6	8

Note: The ClockChip Ring is the one selected after a Reset.

Table 2.2 Encoding TMS Selects

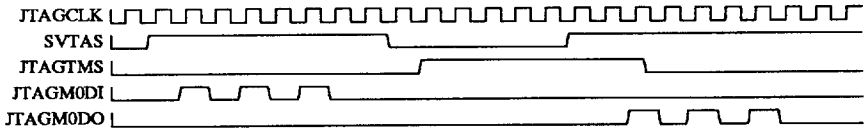
SVRESET	*SVTAS*	*TMS_decode*	*Selected TMS*	*Unselected TMS*
0	X	All outputs are zero, since on reset Clock Chip ring selected		
1	0	Previous selected decode	1	0
1	1	New Selected decode	1	0

2.6 JTAG Control Circuitry



1. Note: SV signals are ANDed with !SVMP*

Figure 2.6
Scan Ring Clocking



2.7 JTAG Clock Generation

The JTAGCLOCK is generated from two sources. If a service processor is present, indicated by $\overline{\text{SVMP}}$ in Figure 2.7, the JTAGCLOCK is generated from the service processor clock signal, SVCLK. The Clock Chip also provides for the possibility of producing the JTAGCLOCK from the 80-MHz oscillator input when the service processor is not present. This approach uses the 80-MHz oscillator input, MOSC, and divides the 80 MHz down to 5 MHz using a four-bit synchronous counter. The JTAGCLOCK is needed because some chips assume the JTAG clock is running so that they can reset. If the service processor is not present, the JTAG clock that is running during $\overline{\text{ResetOut}}$, is turned off when $\overline{\text{ResetOut}}$ is deasserted and the JTAGCLOCK is left in the LOW state. The JTAGCLOCK signal and related waveforms are shown in Figure 2.8.

Figure 2.7
JTAGCLK Circuit

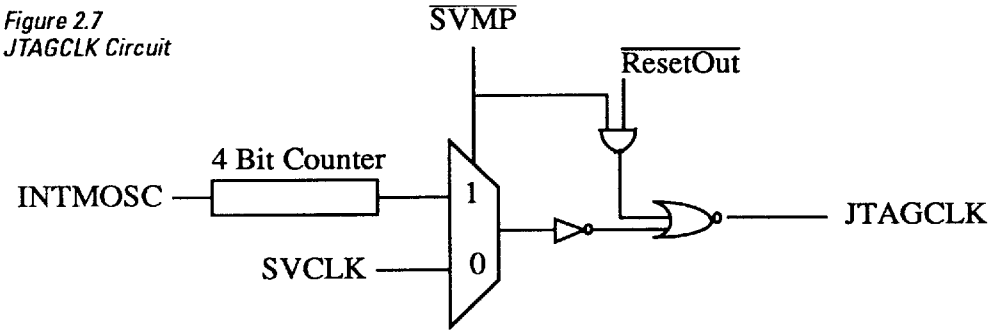
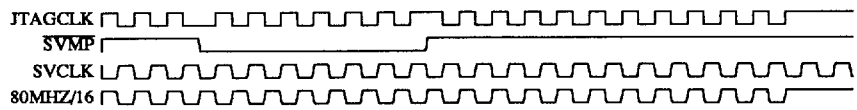


Figure 2.8
JTAGCLK Waveform



2.8 System Reset Signals

The motherboard is reset with the Clock Chip output signal $\overline{\text{ResetOut}}$. $\overline{\text{ResetOut}}$ is sent from the Clock Chip to the SEC chip. $\overline{\text{ResetOut}}$ is generated when Power-on-Reset ($\overline{\text{PORin}}$) is active or service processor is present ($\overline{\text{SVMP}}$ is active), and a service processor Reset ($\overline{\text{SVRESET}}$) has been generated. The SEC chip generates $\overline{\text{ResetOut}}$ from the input signal the other resets for the other chips on the motherboard such as $\overline{\text{MEMRESET}}$ (for the EMC), $\overline{\text{SBRESET}}$ (for the SBus, DMA, MSI, and SEC chips) and $\overline{\text{MRST}}$ (for the Mbus modules,). Inverted versions are created with on board buffers for parts which require reset active positive, such as the floppy drive controller.

The generation of board reset circuitry is shown in Figure 2.9, whereas other resets generated by $\overline{\text{ResetOut}}$ are shown in Figure 2.10.

Figure 2.9
Board Reset Circuit

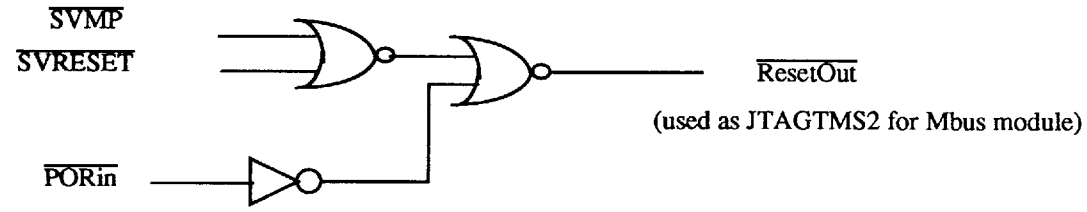
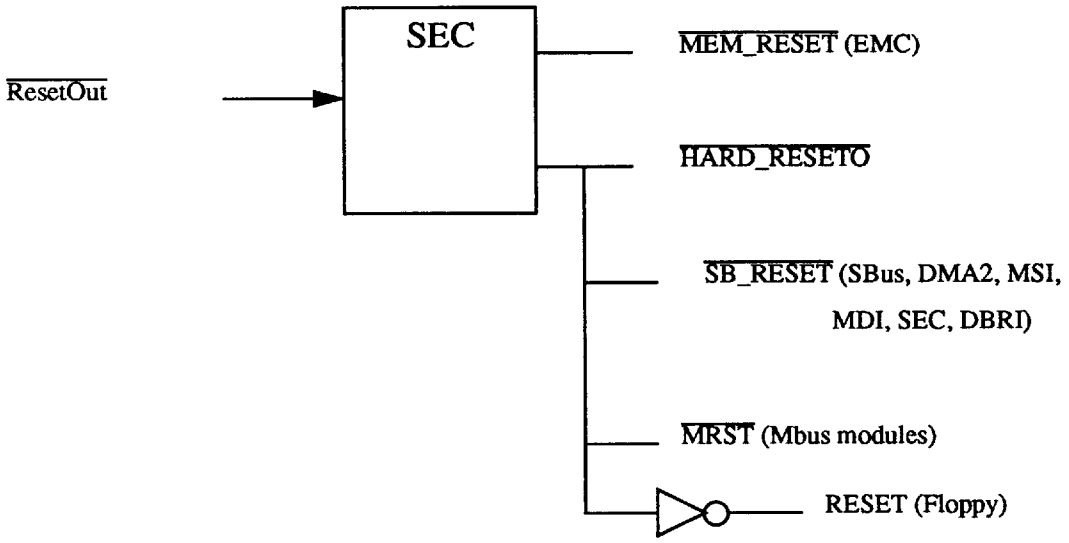
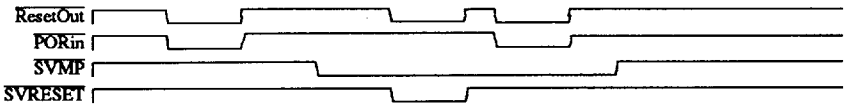


Figure 2.10
System Reset Circuit



The relation among reset signals is shown in the waveform in Figure 2.11

Figure 2.11
Reset Waveforms



Chapter 3
Signal Descriptions

3.1 Clock Chip Signal Descriptions

This section describes the Clock Chip signals. The Clock Chip generates timing signals for the SBus, Mbus, and all chips on the motherboard.

The Clock Chip is produced in a 100-pin PQFP package with 99 pins used for signals. The following list shows the number of pins dedicated to each signal:

- Clock Inputs and Outputs - 8
- JTAG Interface - 14
- Mbus Clocks - 14
- Power and Ground - 45
- Resets - 2
- SBus Clocks - 6
- System Reset, Service Processor and Miscellaneous - 9

The following list of signal descriptions is alphabetized.

$\overline{\text{ResetOut}}$ **Board Reset**
Generated from $\overline{\text{PORin}}$ or $\overline{\text{SVRESET}}$ and $\overline{\text{SVMP}}$ and used to reset the SparKIT-40/SS10 motherboard.

JTAGCLK Bd
50% duty cycle Clock used to clock motherboard JTAG circuitry. Maximum frequency is 6.25 MHz.

JTAGCLK Mod
50% duty cycle Clock used to clock Mbus module JTAG circuitry. Maximum frequency is 6.25 MHz.

JTAGDI
JTAG Scan data input into scan ring.

JTAGDO
JTAG Scan data output out of scan ring.

JTAGTMSMBUS0
JTAG Mbus Module 0 Scan Ring Select

JTAGTMSMBUS1
JTAG Mbus Module 1 Scan Ring Select

JTAGTMSMSI
JTAG MSI Scan Ring Select

JTAGTMSEMC
JTAG EMC Scan Ring Select

JTAGTMSDMA2
JTAG DMA2 Scan Ring Select

JTAGTMSSEC
JTAG SEC Scan Ring Select

JTAGTMSV0
JTAG Video SIMM 0 Scan Ring Select

JTAGTMSV1
JTAG Video SIMM 1 Scan Ring Select

JTAGTMSV2
JTAG Video SIMM 2 Scan Ring Select

JTAGTMSV3
JTAG Video SIMM 3 Scan Ring Select

JTAGTMSDBRI
JTAG DBRI Select

MCLK **Mbus Clock**
Mbus clocks are 40 MHz clocks generated synchronously from a 80-MHz crystal.

Clock Name	*Clock Destination*
MCLK0	Mbus clock slot 0 - #0
MCLK1	Mbus clock slot 0 - #1
MCLK2	Mbus clock slot 0 - #2
MCLK3	Mbus clock slot 0 - #3
MCLK4	Mbus clock slot 1 - #0
MCLK5	Mbus clock slot 1 - #1
MCLK6	Mbus clock slot 1 - #2
MCLK7	Mbus clock slot 1 - #3
MCLK8	Mbus clock for the EMC
MCLK9	Mbus clock for the MSI
MCLK10	Mbus clock Video SIMM 0
MCLK11	Mbus clock Video SIMM 1
MCLK12	Mbus clock Video SIMM 2
MCLK13	Mbus clock Video SIMM 3

ParaTest **Parametric Test Output**

$\overline{\text{PORin}}$ **Power On Reset**
Used to generate $\overline{\text{ResetOut}}$.

SBCLK **SBus Clock**
SBus clocks are 20 MHz clocks generated synchronously from the 80 MHz crystal synchronized to the 40 MHz Mbus clock

Clock Name	*Clock Destination*
SB_CLK0	SBus clock for SEC
SB_CLK1	SBus clock for MSI
SB_CLK2	SBus clock for DMA2
SB_CLK3	SBus clock for SBus slot 1 & 2
SB_CLK4	SBus clock for SBus slot 3 & 4
SB_CLK5	SBus clock for DBRI

SCCXTAL[1,2] **Serial Clock Crystal**
4.9152-MHz crystal input used to generate the serial clock.

SCCCLK **Serial Clock**
Serial Clock output generated by the 4.9152-MHz crystal.

STEPCLOCK
When HIGH this signal steps Mbus clock one cycle, and correspondingly steps SBus one-half cycle.

STOPCLOCK
When HIGH stops Mbus and SBus clocks in their current phase.

$\overline{\text{SVRESET}}$ **Service Processor Reset**
Asserted to initialize the system.

SVCLK **Service Processor Clock**
Data is shifted serially on the falling edge of this clock. Data is sampled on the rising edge of this signal. The cycle time is 200 ns = 5 MHz.

SVTMS **Service Processor Mode Select**
Used to select between shifting data into the system or capturing data in the system. Some systems have more than one scan ring and hence a separate TMS for each ring.

SVDI **Service Processor Data In**
Used to shift data into the selected device on the falling edge of SVCLK.

SVD0 **Service Processor Data Out**
Used to shift data out of the selected device on the falling edge of SVCLK.

SVTAS **Service Processor Address Strobe**
HIGH = allows data to be clocked into JTAG chips.

$\overline{\text{SVMP}}$ **Service Processor Master Present**
This signal is asserted to indicate that a service processor is present in the system. This is not part of the IEEE P.1149.1 JTAG Standard.

$\overline{\text{TN}}$ **Turns off 3-state outputs for testing errors**

The following inputs are not connected to the parametric chain.

EXTOSC **External oscillator input**
The second clock input.

MOSC **80-MHz oscillator input from 80-MHz TTL-can.**
One of two clock inputs.

SELMOSC **Selects external clock input**

Selects between 80 MHz clock input and EXTOSC clock input.
HIGH selects MOSC = 80 MHz input, LOW selects EXTOSC input.

Note: The power and ground pins for each clock output type are separate. Thus the power and grounds for the Mbus clocks, the SBus clocks, and the JTAG clocks are completely separate.

Chapter 4
Specifications

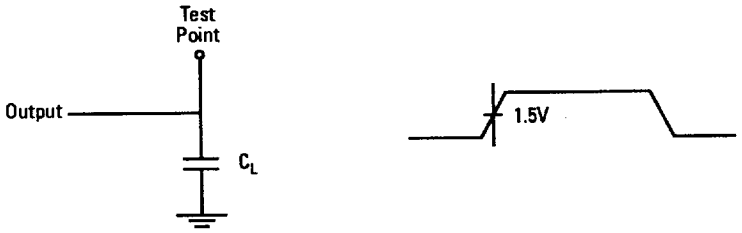
This chapter specifies the electrical and mechanical characteristics of the L64863 Clock Chip. This chapter is divided into three sections:

- Section 4.1, AC Timing
- Section 4.2, Electrical Requirements
- Section 4.3, Packaging

4.1 AC Timing

This section describes the AC timing characteristics of the L64863. During AC testing, HIGH inputs are driven at 3.0 V, and LOW inputs are driven at 0 V. For transitions between HIGH, LOW, and invalid states, timing measurements are made at 1.5 V, as shown in Figure 4.1. The test load, C_L, for each output signal is given in Table.

Figure 4.1 AC Test Load and Waveform for Standard Outputs



For three-state outputs, timing measurements are made from the point at which the output turns ON or OFF. An output is ON when its voltage is greater than 3.5 V or less than 1.5 V. An output is OFF when its voltage is less than VDD – 1.5 V or greater than 1.5 V, as shown in Figure 4.2.

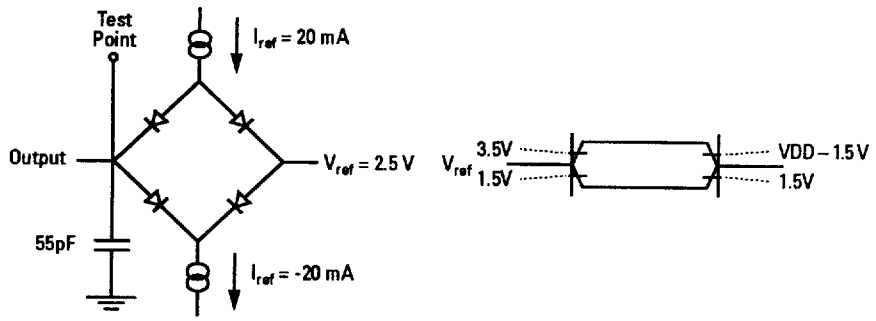


Figure 4.2 AC Test Load and Waveform for 3-State Outputs

4.2 Electrical Requirements

This subsection specifies the electrical requirements for the Clock Chip. Four tables list electrical data in the following categories:

- Recommended Operating Conditions (Table 4.1)
- Capacitive Pin Loading (Table 4.2)
- DC Characteristics (Table 4.3)
- Pin Description Summary (Table 4.4)

Table 4.1 Recommended Operating Conditions

Symbol	*Parameter*	*Limits*	*Unit*
VDD	DC Supply	+4.75 to +5.25	V
TA	Ambient Temperature	0 to +70	°C

Table 4.2 Capacitive Loading

Name	*Description*	*Load pf (inputs + trace)*
Bus Clocks		
MCLK[0-13]	Mbus clock slots	40
SBCLK[0-5]	SBus clock for SEC	40
Clock Inputs & Outputs		
MOSC	80 MHz clock input	5
EXTOSC	External clock input	5
SELMOSC	Clock input mux select	5
SCCXTAL[1,2]	4.9152 MHz serial clock input 1	10
SCCCLK	Serial clock output	10
STOPCLOCK	Stop Mbus and SBus Clock input	5
STEPCLOCK	Step Mbus and SBus Clock input	5

Name	*Description*	*Load pf (inputs + trace)*
JTAG Interface		
JTAGCLKBd and MOD)	JTAG clock	200
JTAGDI	JTAG data out	5
JTAGDO	JTAG data in	15
JTAGtmsMBUS[0,1]	JTAG Mbus Module 0 TMS	15
JTAGTMSMSI	JTAG MSI TMS	15
JTAGTMSEMC	JTAG EMC TMS	15
JTAGTMSDMA2	JTAG DMA2 TMS	15
JTAGTMSSEC	JTAG SEC TMS	15
JTAGTMSV[0-3]	JTAG Video SIMM 0-3 TMS	15
System Reset, Service Processor & Miscellaneous		
$\overline{\text{SVRESET}}$	Service Processor Reset	10
SVCLK	Service Processor Clock	5
SVTMS	SP Test Mode Select	5
SVDI	Service Processor Data In	5
SVDO	Service Processor Data Out	100
SVTAS	SP Address Strobe	5
SVMP	SP Master Present	5
ParaTest	Parametric Test Output	10
$\overline{\text{TestEn}}$	Test Enable Input	5
Resets		
$\overline{\text{PORin}}$	Power on reset	5
$\overline{\text{ResetOut}}$	Board Reset	15
Power / Ground		
MCVCC	Mbus Clock power	10
MCGND	Mbus Clock ground	13
SCVCC	SBus Clock power	4
SCGND	SBus Clock ground	6
VSS	Input power	4
VSS2	Input and Core power	4
GND	Input and Core ground	4

Table 4.3 lists the DC characteristics of the L64863 at VDD equal to 5 V ± 5% at ambient temperature over the specified range.

Table 4.3
DC Characteristics

Symbol	*Parameter*	*Conditions*	*Min*	*Max*	*Unit*
VIL	Input Voltage Low		–	0.8	V
VIH	Input Voltage High		2.0	–	V
VOL	Output Voltage Low	IOL = 4.0 mA IOL = 8.0 mA IOL = 12.0 mA	–	0.4	V
VOH	Output Voltage High	IOH = 4.0 mA IOH = 8.0 mA IOH = 12.0 mA	2.4	–	V
IIL	Input Current Leakage Low TTL Input, with Pullup	VIN = 0V	–175	-2.0	µA
IIH	Input Current Leakage High TTL Input, with Pullup	VIN = VDD	–	-2.0	µA
IOZ	3-State output leakage current, with Pullup	VO = VSS, VO = VDD	-10	10	µA
IOSN	3-State Bidirect or Output Buffer 4 mA Drive 8 mA Drive 12 mA Drive	VOUT = VDD	 30.00 60.00 90.00	 140.00 280.00 420.00	mA
IOSP	3-State Bidirect or Output Buffer 4 mA Drive 8 mA Drive 12 mA Drive	VOUT = 0V	 -25.00 -50.00 -75.00	 -140.00 -280.00 -420.00	mA
ICC	Dynamic supply current		–	120	mA
IDD	Quiescent current	VIN = VDD or VSS, VDD = Max	–	2.0	mA

Table 4.4
Pin Description Summary

Mnemonic	*Description*	*Driver*	*Drive (mA)*	*Active*
Mbus Clocks - 14				
MCLK0	Mbus clock slot 0 - #0	3-State Output	12	High
MCLK1	Mbus clock slot 0 - #1	3-State Output	12	High
MCLK2	Mbus clock slot 0 - #2	3-State Output	12	High
MCLK3	Mbus clock slot 0 - #3	3-State Output	12	High

Table 4.4
Pin Description Summary

Mnemonic	*Description*	*Driver*	*Drive (mA)*	*Active*
MCLK4	Mbus clock slot 1 - #0	3-State Output	12	High
MCLK5	Mbus clock slot 1 - #1	3-State Output	12	High
MCLK6	Mbus clock slot 1 - #2	3-State Output	12	High
MCLK7	Mbus clock slot 1 - #3	3-State Output	12	High
MCLK8	Mbus clock for the EMC	3-State Output	12	High
MCLK9	Mbus clock for the MSI	3-State Output	12	High
MCLK10	Mbus clock Video SIMM 0	3-State Output	12	High
MCLK11	Mbus clock Video SIMM 1	3-State Output	12	High
MCLK12	Mbus clock Video SIMM 2	3-State Output	12	High
MCLK13	Mbus clock Video SIMM 3	3-State Output	12	High
SBUS Clocks - 6				
SB_CLK0	SBus clock for SEC	3-State Output	12	High
SB_CLK1	SBus clock for MSI	3-State Output	12	High
SB_CLK2	SBus clock for DMA2	3-State Output	12	High
SB_CLK3	SBus clock for SBus slot 1 & 2	3-State Output	12	High
SB_CLK4	SBus clock for SBus slot 3 & 4	3-State Output	12	High
SB_CLK5	SBus clock for DBRI	3-State Output	12	High
Clock Inputs & Outputs - 8				
MOSC	80 MHz clock input	Input	–	High
EXTOSC	External clock input	Input	–	High
SELMOSC	Clock input mux select	Input	–	High
SCCXTAL1	4.9152 MHz serial clock input 1	Input	–	High
SCCXTAL2	4.9152 MHz serial clock input 2	Input	–	High
SCC_CLK	Serial Clock Output	Output	4	High
STOPCLK	Stop Mbus & SBus Clock input	Input	–	High
STEPCLK	Step Mbus & SBus Clock input	Input	–	High
JTag Interface - 14				
JTAGCLKBD	JTAG clock	3-State Output	12	High
JTAGCLKMOD	JTAG clock	3-State Output	12	High
JTAGDO	JTAG data out	3-State Output	4	High
JTAGDI	JTAG data in	Input	–	High

Table 4.4
Pin Description Summary

Mnemonic	*Description*	*Driver*	*Drive (mA)*	*Active*
JTAGTMSMBUS0	JTAG Mbus Module 0 TMS	3-State Output	4	High
JTAGTMSMBUS1	JTAG Mbus Module 1 TMS	3-State Output	4	High
JTAGTMSMSI	JTAG MSI TMS	3-State Output	4	High
JTAGTMSEMC	JTAG EMC TMS	3-State Output	4	High
JTAGTMSDMA2	JTAG DMA2 TMS	3-State Output	4	High
JTAGTMSSEC	JTAG SEC TMS	3-State Output	4	High
JTAGTMSV0	JTAG Video SIMM 0 TMS	3-State Output	4	High
JTAGTMSV1	JTAG Video SIMM 1 TMS	3-State Output	4	High
JTAGTMSV2	JTAG Video SIMM 2 TMS	3-State Output	4	High
JTAGTMSV3	JTAG Video SIMM 3 TMS	3-State Output	4	High
JTAGTMSDBRI	JTAG DBRI TMS	3-State Output	4	High
System Reset, Service Processor & Miscellaneous - 9				
$\overline{\text{SV\_RESET}}$	Service Processor Reset	Input	–	Low
SV_CLK	Service Processor Clock	Input	–	High
SV_TMS	SP Test Mode Select	Input	–	High
SV_DI	Service Processor Data In	Input	–	High
SV_DO	Service Processor Data Out	Output	4	High
SV_TAS	SP Address Strobe	Input	–	High
$\overline{\text{SV\_MP}}$	SP Master Present	Input	–	Low
ParaTest	Parametric Test Output	Output	4	High
$\overline{\text{TestEn}}$	Test Enable Input	Input	–	Low
Resets - 2				
$\overline{\text{PORin}}$	Power on reset 5	Input	–	Low
$\overline{\text{ResetOut}}$	Board Reset	Output	8	Low

4.3 Packaging

The Clock Chip is an LSI gate array in a 100-pin PQFP package. The die's physical dimensions are 4.7 mm x 4.7 mm. The number of pads on the die is 98, including 90 for I/O signals, and eight dedicated power & grounds.

The 100-pin PQFP package has the following electrical characteristics:

Characteristic	*Value*
Inductance/pin	6 nH to 13 nH
Capacitance/pin	1.2 pF to 1.8 pF
Resistance/pin	0.13 Ohms to 0.26 Ohms

The actual measured power consumption is 0.5 watts. The 100 PQFP package has a ThetaJ of 80 C/W which generates a junction temperature of 40 ambient + 15 rise + 0.5 * 80, which equals 95 °C.

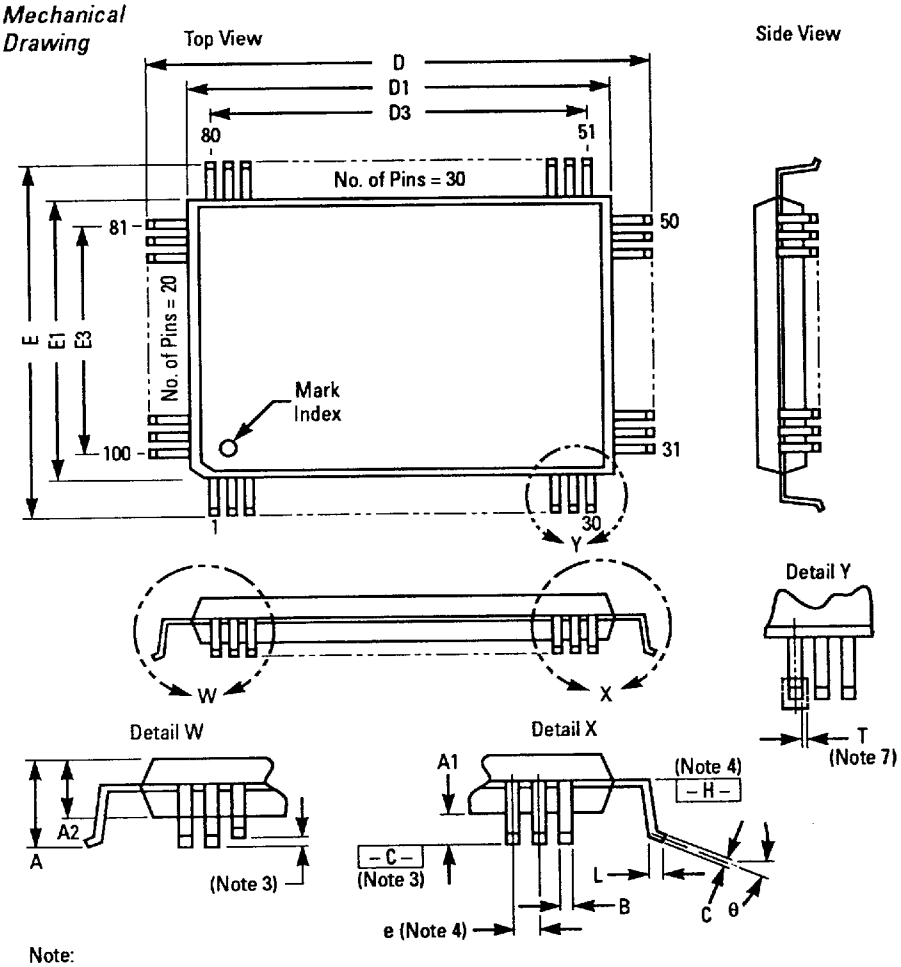
Table 4.5 gives signal names and their corresponding PQFP pin number. Note that pin 25 is shown as STEPCLK on the schematic and tied LOW as well as being shown as VSS.

Table 4.5
100-pin PQFP Pin List

Signal Name	*Pin*	*Signal Name*	*Pin*	*Signal Name*	*Pin*	*Signal Name*	*Pin*
EXTOSC	54	MCLK6	22	STEPCLK	25	VDD	45
JTAGDI	76	MCLK7	29	STOPCLK	24	VDD	48
JTAGDO	65	MCLK8	31	SV_CLK	80	VDD	52
JTAGCLKBD	81	MCLK9	34	SV_DI	26	VDD	53
JTAGCLKMOD	82	MCLK10	37	SV_DO	95	VDD	59
JTAGTMSDBRI	86	MCLK11	44	$\overline{\text{SV\_MP}}$	55	VDD	62
JTAGTMSDMA2	96	MCLK12	47	$\overline{\text{SV\_RESET}}$	38	VDD	68
JTAGTMSEMC	94	MCLK13	50	SV_TAS	43	VDD	70
JTAGTMSMBUS0	87	MOSC	93	SV_TMS	1	VDD	73
JTAGTMSMBUS1	88	ParaTest	56	$\overline{\text{TestEn}}$	51	VDD	77
JTAGTMSMSI	92	$\overline{\text{PORin}}$	64	VDD	3	VDD	78
JTAGTMSSEC	79	$\overline{\text{ResetOut}}$	42	VDD	6	VDD	89
JTAGTMSV0	97	SB_CLK0	75	VDD	9	VSS	2
JTAGTMSV1	98	SB_CLK1	72	VDD	12	VSS	5
JTAGTMSV2	99	SB_CLK2	69	VDD	14	VSS	8
JTAGTMSV3	100	SB_CLK3	63	VDD	18	VSS	11
MCLK0	4	SB_CLK4	60	VDD	20	VSS	15
MCLK1	7	SB_CLK5	57	VDD	27	VSS	17
MCLK2	10	SCCCLK	83	VDD	28	VSS	21
MCLK3	13	SCCXTAL1	85	VDD	33	VSS	30
MCLK4	16	SCCXTAL2	84	VDD	36	VSS	32

Signal Name	*Pin*	*Signal Name*	*Pin*	*Signal Name*	*Pin*	*Signal Name*	*Pin*
MCLK5	19	SELMOSC	23	VDD	41	VSS	35
VSS	39	VSS	49	VSS	66	VSS	74
VSS	40	VSS	58	VSS	67	VSS	90
VSS	46	VSS	61	VSS	71	VSS	91

Figure 4.3
100-pin PQFP
Mechanical
Drawing



Dimension		mm
A	Max	3.40
A1	Min	0.25
	Max	0.35
A2	Min	2.55
	Nom	2.80
	Max	3.05
B	Min	0.22
	Nom	0.30
	Max	0.38
C	Min	0.12
	Max	0.25
D	Min	23.65
	Nom	23.90
	Max	24.15
D1	Min	19.90
	Nom	20.00
	Max	20.10
D3	Ref	18.85
e	BSC	0.65
E	Min	17.65
	Nom	17.90
	Max	18.15
E1	Min	13.90
	Nom	14.00
	Max	14.10
E3	Ref	12.35
L	Min	0.65
	Nom	0.80
	Max	0.95
T	Max	0.10
θ	Min	0°
	Max	7°

Note:
1. Total number of pins is 100.
2. Drawing is not to scale.
3. Coplanarity of all leads shall be within 0.10 mm (difference between the highest and lowest lead with seating plane – C – as reference).
4. Datum plane – H – is located at mold parting line and is coincident with the bottom of the lead, where the lead exits the plastic body. Lead pitch determined at – H –.
5. Dimensions D1 and E1 do not include mold protrusion. Allowable protrusion is 0.25 mm per side. These dimensions to be determined at – H –.
6. Dimensions D3 and E3 to be centered relative to dimensions D1 and E1, respectively, ±0.200 mm.
7. Tolerance window for lead skew from true position is determined at seating plane – C –.
8. For board layout and manufacturing, you may obtain engineering drawings from your LSI Logic Products marketing representative by requesting the outline drawing for package code PB.

MD92.PB