HIGH PERFORMANCE BYTE ORGANIZED ROMS

Features

- JEDEC Standard Versions:

  IMP23208 32 Pin 2Meg (262,144 word × 8 Bit)
  IMP23408 32 Pin 4Meg (524,288 word × 8 Bit)

- Fast Access Times:

From Chip Enable	120 ns
From Any Address	110 ns
From Output Enable	50 ns

- Single +5 Volt Power Supply

- Low Power Supply Current (worst case):

	t_{AA} = 110ns
Operating Current	25 mA
Standby Current	100 μA

- Class 3 (4,000 volt) ESD Protection

- Programmable Active Level on Select Output Enable Pins for Maximum System Flexibility. See Figure 1.

- Available in Both Standard Dual In-Line and Surface Mount Packages

- Automatic Low-Power Standby Mode Initiated by Chip Enable Going to Non-select Mode

- DC Noise Immunity:

Guaranteed	400 mV
Typical	> 1 Volt

- Expandable Design Hierarchy and Common Process Provide Simplified IMP23000 Series Family Qualification

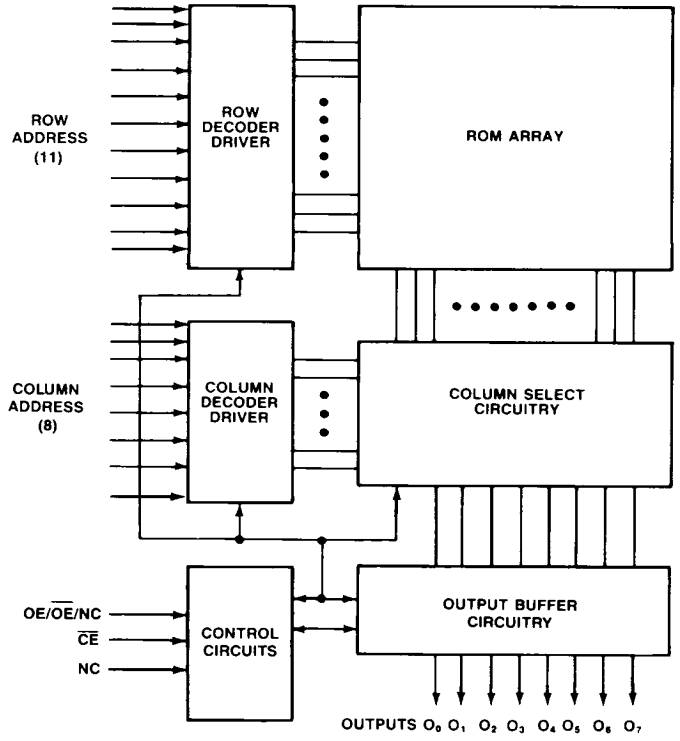

Fig. 1 Block Diagram

Note: Some control circuit input pins are not programmable on these devices.

Packaging Options

IMP P/N	32 PDIP	44 PLCC	44 PQFP
IMP23208	•	•	•
IMP23408	•	•	•

Alternate Packages Available

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Absolute Maximum Ratings

Ambient Operating Temperature .....–10 to +80°C
Storage Temperature .....–65 to +150°C
Supply Voltage to
Ground Potential .....–0.5 to +7.0 V
Applied Output Voltage .....–0.5 to +7.0 V
Applied Input Voltage .....–0.5 to +7.0 V
Power Dissipation .....1.0 W

Stress above those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliablity.

Capacitance: T_A = 25°C, f = 1.0 MHz, Note 6

Symbol	Parameter	Min	Max	Unit	Conditions
C_I	Input Capacitance	—	5	pF	V_{IN} = 0 V
C_O	Output Capacitance	—	5	pF	V_{OUT} = 0 V

DC Characteristics: T_A = 0 to +70°C, V_{CC} = +5 V ± 10%

Symbol	Parameter	Min	Max	Unit	Conditions
V_{OH}	Output HIGH Voltage	2.4	V_{CC}	V	I_{OH} = –1.0 mA
V_{OL}	Output LOW Voltage	—	0.4	V	I_{OL} = 3.2 mA
V_{IH}	Input HIGH Voltage	2.0	V_{CC}	V	
V_{IL}	Input LOW Voltage	–0.5	0.8	V	
I_{LI}	Input Leakage Current	—	1	μA	V_{IN} = 0 V to V_{CC}
I_{LO}	Output Leakage Current	—	1	μA	V_{OUT} = 0 V to V_{CC}
I_{CC}	Operating Supply Current	—	25	mA	Note 1
I_{SB}	Standby Supply Current	—	100	μA	Note 2
I_{OS}	Output Short Circuit Current	—	70	mA	Note 3

AC Characteristics: T_A = 0 to +70°C, V_{CC} = +5 V ± 10%

		–11		–14		–19			
Symbol	Parameter	Min	Max	Min	Max	Min	Max	Units	Conditions
t_{CYC}	Read Cycle Time	—	120	—	150	—	200	ns	
t_{AA}	Address Access Time	—	110	—	140	—	190	ns	
t_{OH}	Output Hold After Address Change	10	—	10	—	10	—	ns	
t_{ACE}	Chip Enable Access Time	—	120	—	150	—	200	ns	
t_{AOE}	Output Enable Access Time	—	50	—	60	—	75	ns	
t_{LZ}	Output LOW Z Delay	10	—	10	—	10	—	ns	Note 4
t_{HZ}	Output HIGH Z Delay	—	40	—	50	—	65	ns	Note 5
t_{PU}	Power-Up Time	0	—	0	—	0	—	ns	
t_{PD}	Power-Down Time	—	40	—	50	—	65	ns	

Notes

1. Measured with device selected and Inputs = V_{IH}/V_{IL}, $\overline{CE}$ = V_{IL}.
2. Measured with device selected and Inputs = V_{CC} – 0.2V/0.2V, $\overline{CE}$ = 0.2V.
3. For a duration not to exceed 30 seconds.
4. Output LOW impedance delay (TLZ) is measured from $\overline{CE}$ or $\overline{OE}$ going active.
5. Output HIGH impedance delay (THZ) is measured from $\overline{CE}$ or $\overline{OE}$ going inactive.
6. This parameter is periodically sampled and is not 100% tested.

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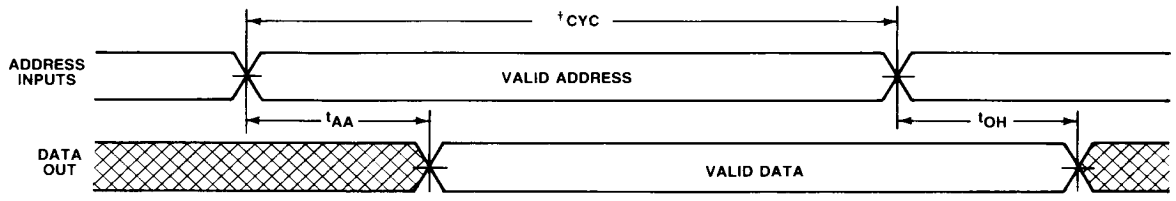
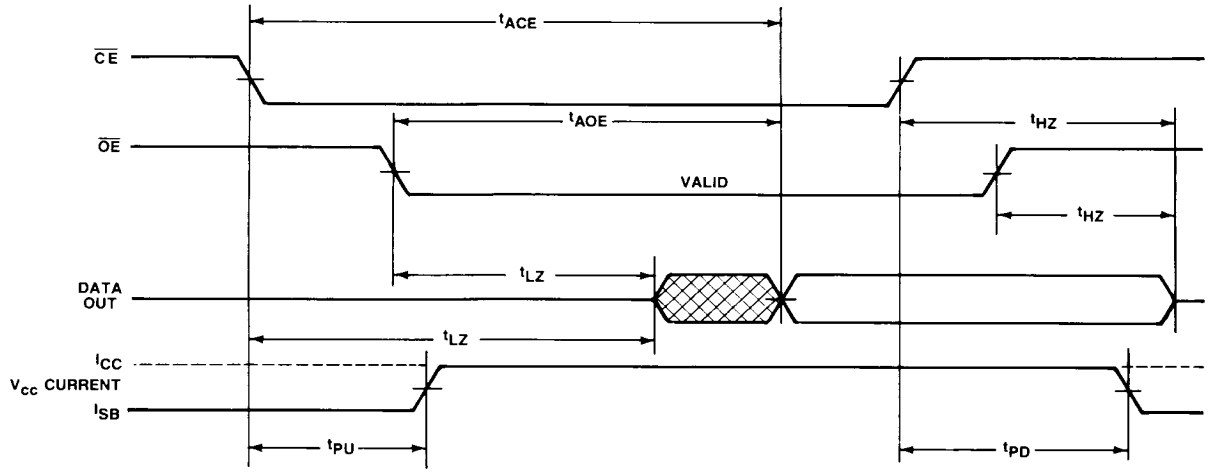
Timing Diagrams

Propagation Delay From Address ($\overline{CE}$/$\overline{OE}$ = Active)



Propagation Delay From Chip Enable or Output Enable (Address Valid)



AC Test Conditions

Input Pulse Levels	0.4 to 2.4 V
Input Rise and Fall Times	10 ns
Input Timing Level	1.5 V
Output Timing Level	1.5 V
Output Load	See Figure 2

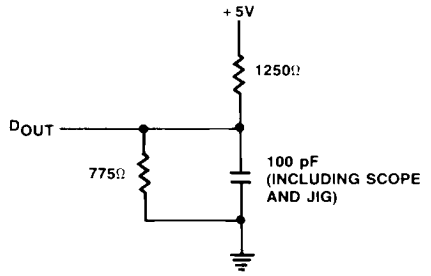


Fig. 2 AC Test Output Load Condition

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IMP23208 (2048K) BYTE ORGANIZED HIGH PERFORMANCE ROMS

Features

- JEDEC Standard Version
- Fast Access Times:

From Chip Enable	120 ns
From Any Address	110 ns
From Output Enable	50 ns

- Low Power Supply Current (worst case):

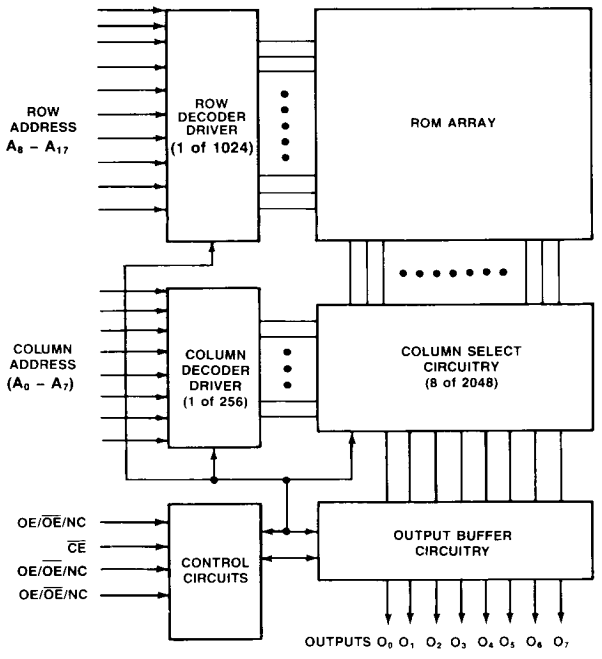
t_{AA} = 110ns	
Operating Current	25 mA
Standby Current	100 μA

- Single +5 Volt Power Supply
- Class 3 (4,000 volt) ESD Protection
- Programmable Chip and Output Enable Pins for Maximum System Flexibility
- Available in Both Standard Dual In-Line and Surface Mount Packages
- DC Noise Immunity:

Guaranteed	400 mV
Typical	> 1 Volt

- Expandable Design Hierarchy and Common Process Provides Simplified IMP23000 Family Qualification

Block Diagram



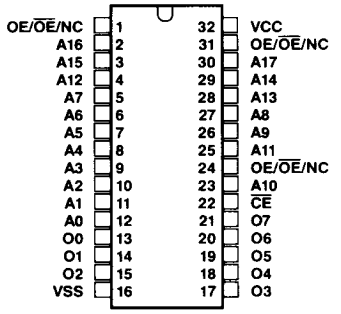
Description

The IMP23208 is a 262,144 word × 8 bits mask programmable read only memory device. The IMP23208 is a byte-wide compatible JEDEC standard pin configuration encapsulated in a plastic 32 pin dual-in-line or 44 pin leaded chip carrier (PLCC) package. IMP23208 devices offer selectable access times including 190, 140, and 110 ns while realizing low power consumption.

The IMP23208 is fabricated using IMP's advanced CMOS™ design and process methodology to achieve superior speed and power performance. IMP's high performance memories are compatible with battery and non-battery operated systems. The IMP23208 memory capacity is ideally suited for storing application program software, printer control and font programs, graphic look-up tables, dictionary/thesaurus software, digital music waveforms, and video game software.

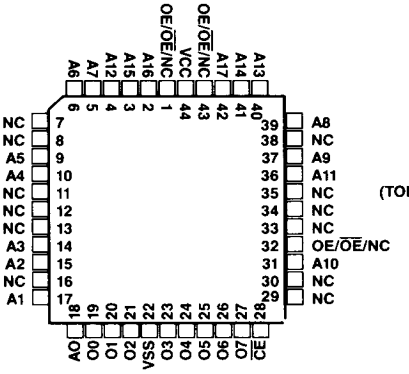
Package Configurations:

Plastic 32 PDIP



(TOP VIEW)

Plastic 44 PLCC or PQFP



(TOP VIEW)

Pin Nomenclature

A_0–A_7	Column Address Inputs	$\overline{OE}$	Output Enable Input (Low)
A_8–A_{17}	Row Address Inputs	$\overline{CE}$	Chip Enable Input (Low)
OE	Output Enable Input (High)	NC	No Connect

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IMP23408 (4096K) BYTE ORGANIZED HIGH PERFORMANCE ROMS

Features

- JEDEC Standard Version
- Fast Access Times:

From Chip Enable	120 ns
From Any Address	110 ns
From Output Enable	50 ns

- Low Power Supply Current (worst case):

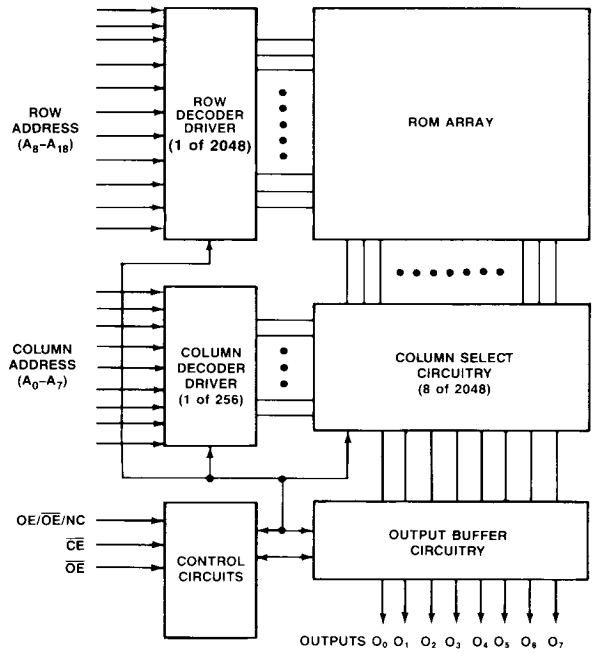
t_{AA} = 110ns	
Operating Current	25 mA
Standby Current	100 μA

- Single +5 Volt Power Supply
- Class 3 (4,000 volt) ESD Protection
- Programmable Chip and Output Enable Pins for Maximum System Flexibility
- Available in Both Standard Dual In-Line and Surface Mount Packages
- DC Noise Immunity:

Guaranteed	400 mV
Typical	> 1 Volt

- Expandable Design Hierarchy and Common Process Provides Simplified IMP23000 Family Qualification

Block Diagram



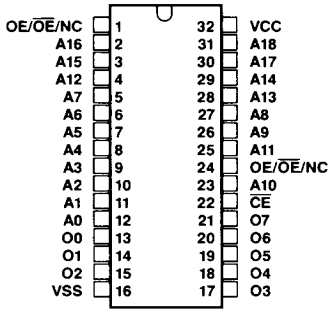
Description

The IMP23408 is a 524,288 word × 8 bits mask programmable read only memory device. The IMP23408 is a byte-wide compatible JEDEC standard pin configuration encapsulated in a plastic 32 pin dual-in-line or 44 pin leaded chip carrier (PLCC) package. IMP23408 devices offer selectable access times including 190, 140, and 110 ns while realizing low power consumption.

The IMP23408 is fabricated using IMP's advanced CMOS™ design and process methodology to achieve superior speed and power performance. IMP's high performance memories are compatible with battery and non-battery operated systems. The IMP23408 memory capacity is ideally suited for storing application program software, printer control and font programs, graphic look-up tables, dictionary/thesaurus software, digital music waveforms, and video game software.

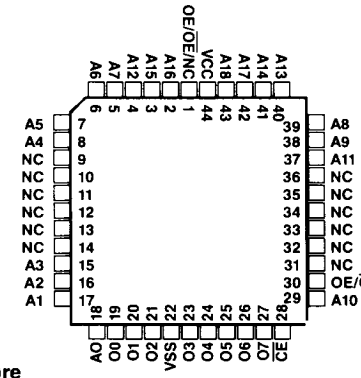
Package Configurations:

Plastic 32 PDIP



(TOP VIEW)

Plastic 44 PLCC or PQFP



(TOP VIEW)

Pin Nomenclature

A_0–A_7	Column Address Inputs	$\overline{OE}$	Output Enable Input (Low)
A_8–A_{18}	Row Address Inputs	$\overline{CE}$	Chip Enable Input (Low)
OE	Output Enable Input (High)	NC	No Connect

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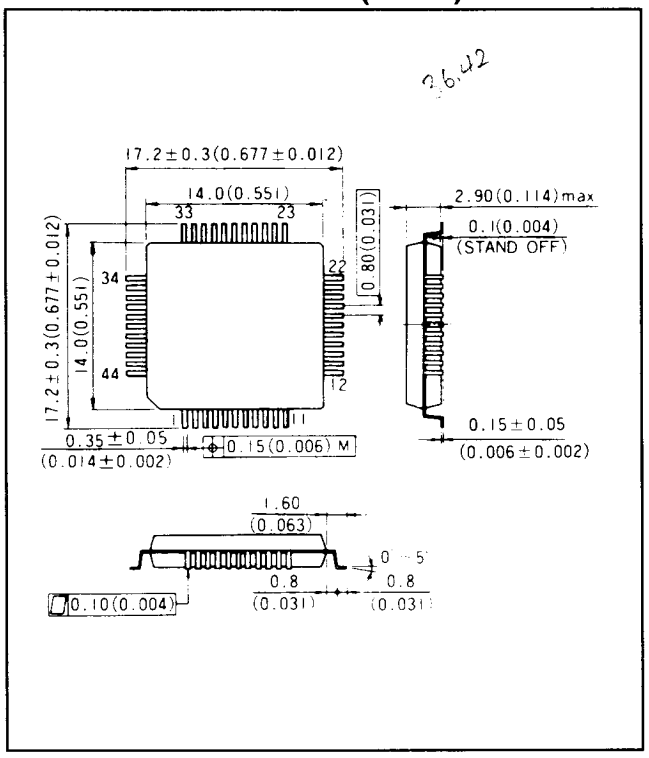
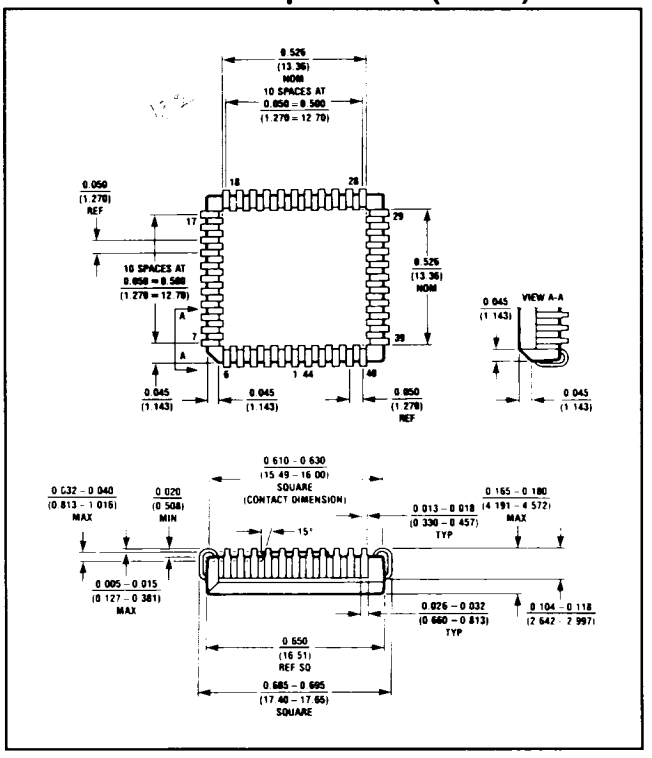
23000 SERIES PACKAGE OUTLINE DRAWINGS

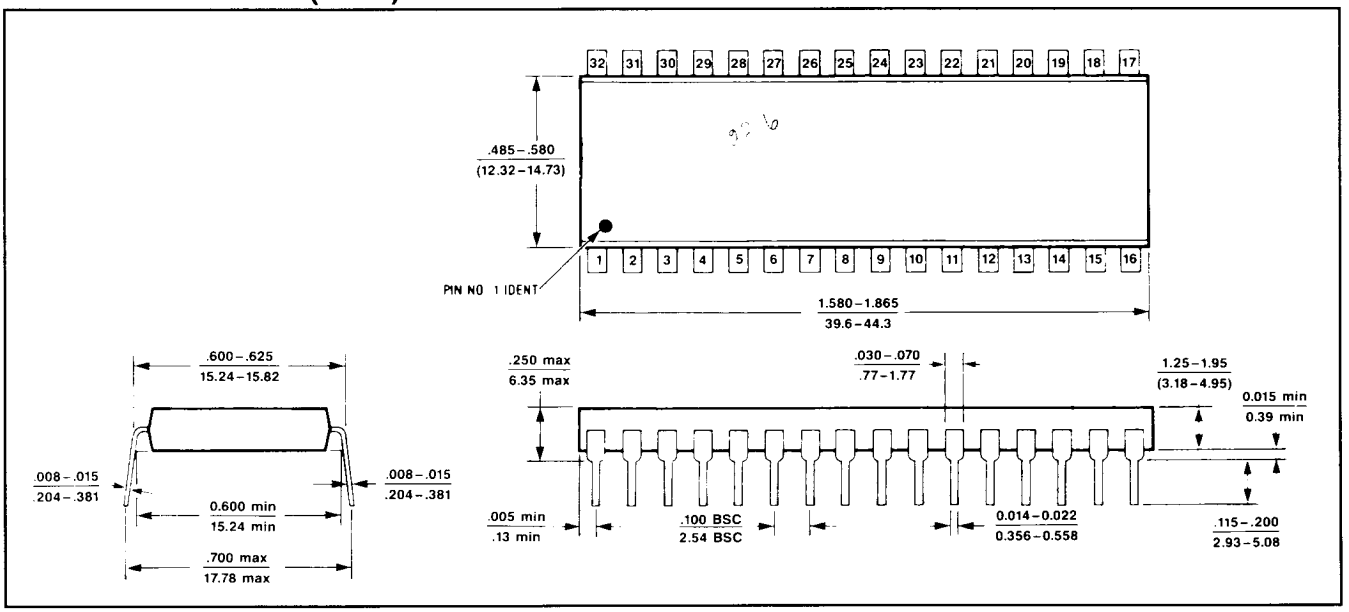
Plastic Quad Flat Pack (PQFP) 44 Pin



Plastic Leaded Chip Carrier (PLCC) 44 Pin



Plastic Dual-In-Line (PDIP) 32 Pin



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