T-46-23-05

September 1990

MATRA M H S

DATA SHEET

HM 65767

16 K x 1
HIGH SPEED CMOS SRAM

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FEATURES

- **FAST ACCESS TIME**
  MILITARY : 25/35/45/55 ns (max)
  COMMERCIAL : 20/25/35/45/55 ns (max)
- **LOW POWER CONSUMPTION**
  ACTIVE : 275 mW (typ)
  STANDBY : 55 mW (typ)
- **WIDE TEMPERATURE RANGE :**
  – 55°C TO + 125°C
- **300 MILS WIDTH PACKAGE**
- **TTL COMPATIBLE INPUTS AND OUTPUTS**
- **ASYNCHRONOUS**
- **CAPABLE OF WITHSTANDING GREATER THAN 2000 V ELECTROSTATIC DISCHARGE**
- **SINGLE 5 VOLT SUPPLY**

DESCRIPTION

The HM 65767 is a high speed CMOS static RAM organized as 16384x1 bit. It is manufactured using MHS's high performance CMOS technology.
Access times as fast as 20 ns are available with maximum power consumption of only 385 mW.
The HM 65767 features fully static operation requiring no external clocks or timing strobes. The automatic power-down feature reduces the power consumption by 70 % when the circuit is deselected.

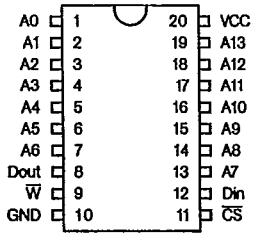
Easy memory expansion is provided by an active low chip select ($\overline{CS}$) and three state drivers.
All inputs and outputs of the HM 65767 are TTL compatible and operate from single 5 V supply thus simplifying system design.
The HM 65767 is processed following the test methods of MIL STD 883C.

PACKAGES

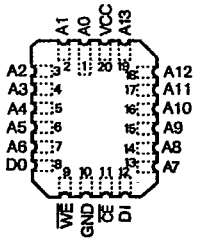
Plastic 300 mils, 20 pins, DIL.
Ceramic 300 mils, 20 pins, DIL.
Tape and Reel Service.

SOIC 300 mils, 20 pins
LCC 20 pins.

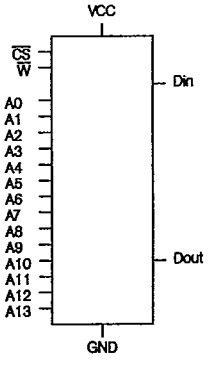
Pinout DIL 20 pins (top view)



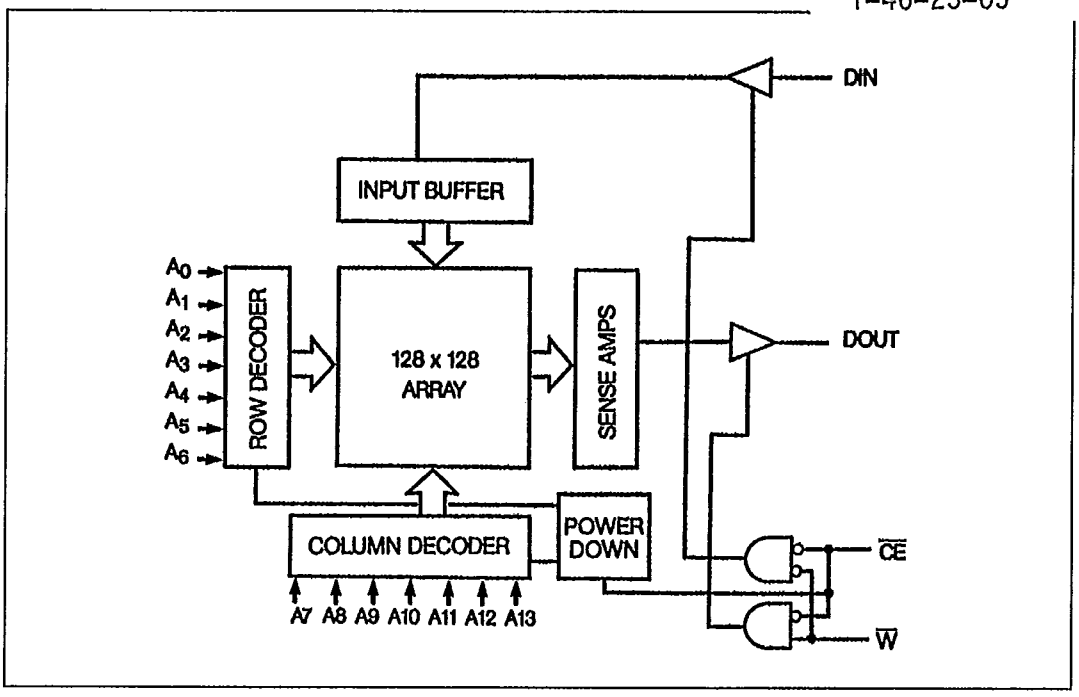
Pinout LCC 20 pins (top view)



LOGIC SYMBOL



BLOCK DIAGRAM



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PIN NAMES

A0-A13	: Address inputs	$\overline{W}$	: Write enable
Din	: Input	Vcc	: Power
Dout	: Output	GND	: Ground
$\overline{CS}$	: Chip Select		

TRUTH TABLE

$\overline{CS}$	$\overline{W}$	DATA-IN	DATA-OUT	MODE
H	X	Z	Z	Deselect
L	H	Z	Valid	Read
L	L	Valid	Z	Write

L = low - H = high - X = H or L, Z = high impedance

ABSOLUTE MAXIMUM RATINGS

Supply voltage to GND potential : – 0.5 V to + 7.0 V
DC input voltage : – 3.0 V to + 7.0 V
DC output voltage in high Z state : – 0.5 V to + 7.0 V

Storage temperature : – 65°C to + 150°C
Output current into outputs (low) : 20 mA

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OPERATING RANGE

		OPERATING VOLTAGE	OPERATING TEMPERATURE
Military	(– 2)	5 V ± 10 %	– 55°C to + 125°C
Commercial	(– 5)	5 V ± 10 %	0°C to + 70°C

RECOMMENDED DC OPERATING CONDITIONS

PARAMETER	DESCRIPTION	MINIMUM	TYPICAL	MAXIMUM	UNIT
Vcc	Supply voltage	4.5	5.0	5.5	V
Gnd	Ground	0.0	0.0	0.0	V
VIL	Input low voltage	– 3.0	0.0	0.8	V
VIH	Input high voltage	2.0	–	5.5	V

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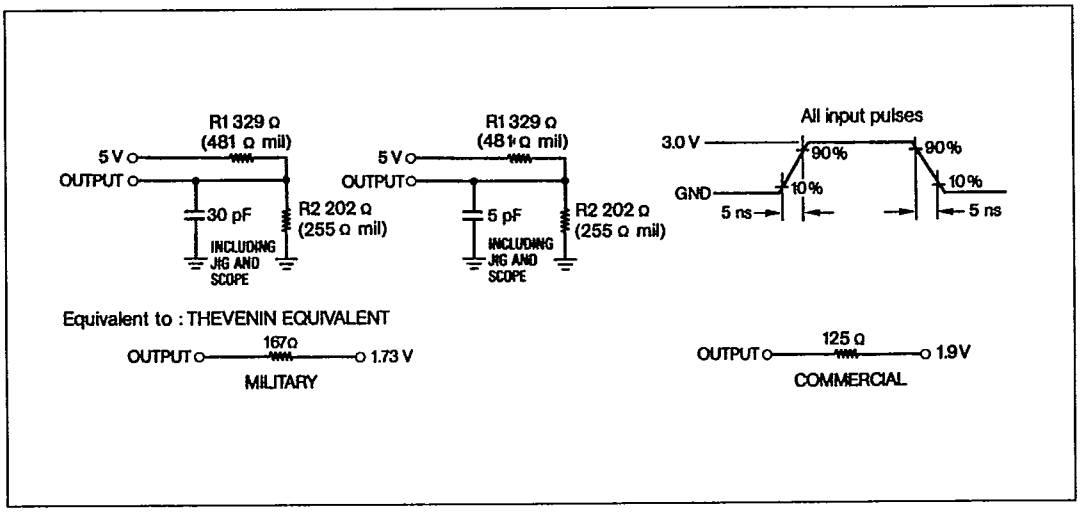
CAPACITANCE

PARAMETER		DESCRIPTION	MINIMUM	TYPICAL	MAXIMUM	UNIT
Cin	(1)	Input capacitance	–	–	4	pF
Cout	(1)	Output capacitance	–	–	7	pF
C CS	(1)	CS capacitance	–	–	5	pF

Note : 1. TA = 25°C, f = 1 MHz, Vcc = 5.0 V.

AC TEST LOADS AND WAVEFORMS



ELECTRICAL CHARACTERISTICS DC PARAMETER

PARAMETER		DESCRIPTION	MINIMUM	TYPICAL	MAXIMUM	UNIT
IIX	(2)	Input leakage current	−10.0	–	10.0	µA
IOZ	(3)	Output leakage current	−50.0	–	50.0	µA
IOS	(3)	Output short circuit current	–	–	−350.0	mA
VOL	(4)	Output low voltage	–	–	0.4	V
VOH	(5)	Output high voltage	2.4	–	–	V

Notes : 2. Gnd < Vin < Vcc, Gnd < Vout < Vcc Output disabled.
3. Vcc = max, Vout = Gnd, duration of the short circuit should not exceed 30 seconds.
4. Vcc min, IOL = 12.0 mA (commercial) 8.0 mA (military).
5. Vcc min, IOH = −4.0 mA.

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Consumption for Commercial specification :

SYMBOL	PARAMETER	65767 F-5	65767 H-5	65767 K-5	65767 M-5	65767 N-5	UNIT	VALUE
ICCSB (6)	Standby supply current	30	20	20	20	30	mA	max
ICCOP (7)	Dynamic operating current	70	70	70	70	90	mA	max

Consumption for Military specification :

SYMBOL	PARAMETER	65767 H-2	65767 K-2	65767 M-2	65767 N-2	UNIT	VALUE
ICCSB (6)	Standby supply current	30	20	20	20	mA	max
ICCOP (7)	Dynamic operating current	80	70	70	70	mA	max

Notes : 6. $\overline{CS} \leq$ VIH, a pull-up resistor to Vcc on the $\overline{CS}$ input is required to keep the device deselected during Vcc power-up otherwise ICCSB will exceed values above.
7. Vcc max, Output current = 0 mA, f = max, Vin = Vcc or Gnd.
* Preliminary specification.

ELECTRICAL CHARACTERISTICS AC PARAMETERS

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AC CONDITIONS :

Input pulse levels : Gnd to 3.0 V
Input rise : 5 ns
Input timing reference levels : 1.5 V
Output loading IOL/IOH : + 30 pF

WRITE CYCLE : Commercial specification

SYMBOL	PARAMETER	65767 F-5	65767 H-5	65767 K-5	65767 M/N-5	UNIT	VALUE
TAVAV	Write cycle time	20	25	30	40	ns	min
TAVWL	Address set-up time	0	0	0	0	ns	min
TAVWH	Address valid to end of write	20	25	30	40	ns	min
TDVWH	Data set-up time	15	15	15	15	ns	min
TELWH	$\overline{CS}$ low to write end	20	25	30	40	ns	min
TWLQZ (8)	Write low to high Z	10	25	30	20	ns	max
TWLWH	Write pulse width	15	15	20	20	ns	min
TWHAX	Address hold to end of write	2	2	2	2	ns	min
TWDHX	Data hold time	0	0	0	0	ns	min
TWHQX (8)	Write high to low Z	3	0	0	0	ns	min
TEHAX	Address hold end $\overline{CS}$	3	3	3	3	ns	min

WRITE CYCLE : Military specification

SYMBOL	PARAMETER	65767 H-2	65767 K-2	65767 M-2	65767 N-2	UNIT	VALUE
TAVAV	Write cycle time	25	30	40	40	ns	min
TAVWL	Address set-up time	0	0	0	0	ns	min
TAVWH	Space !	25	30	40	40	ns	min
TDVWH	Data set-up time	15	15	15	15	ns	min
TELWH	$\overline{CS}$ low to write end	25	30	40	40	ns	min
TWLQZ (8)	Write low to high Z	15	20	20	20	ns	max
TWLWH	Write pulse width	15	20	20	20	ns	min
TWHAX	Address hold to end of write	0	0	0	0	ns	min
TWHDX	Data hold time	0	0	0	0	ns	min
TWHQX (8)	Write high to low Z	3	0	0	0	ns	min
TEHAX	Address hold end $\overline{CS}$	3	3	3	3	ns	min

Note : 8. The data input set-up and hold timing should be referenced to the rising edge of the signal that terminates the write.

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WRITE CYCLE 1 ($\overline{W}$ CONTROLLED)

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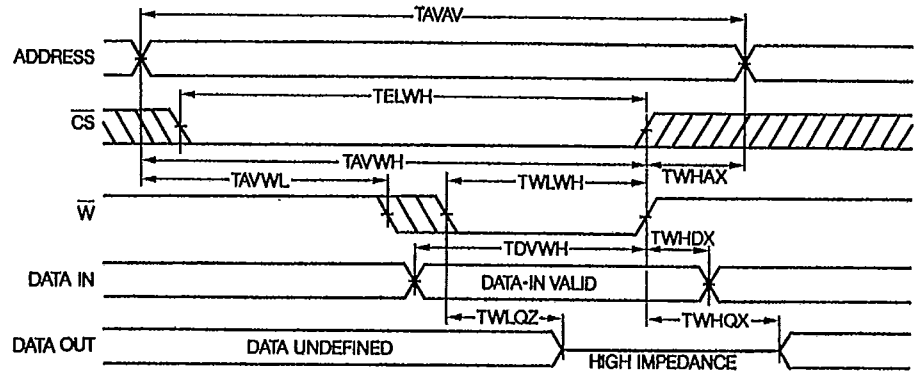

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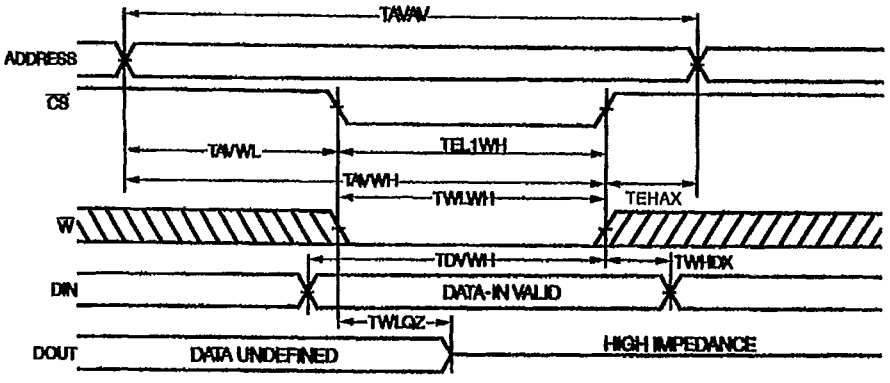
WRITE CYCLE 2 ($\overline{CS}$ CONTROLLED)



READ CYCLE : Commercial specification

SYMBOL	PARAMETER	65767 F-5	65767 H-5	65767 K-5	65767 M-5	65767 N-5	UNIT	VALUE
TAVAV	READ cycle time	20	25	30	40	50	ns*	min
TAVQV	Address access time	20	25	30	40	50	ns	max
TAVQX	Address valid to low Z	2	3	3	3	3	ns	min
TELQV	Chip-select access time	20	25	35	45	55	ns	max
TELQX	$\overline{CS}$ low to low Z	3	5	5	5	5	ns	min
TEHQZ	$\overline{CS}$ high to high Z	15	15	20	25	25	ns	max
TELIC	$\overline{CS}$ low to power up	0	0	0	0	0	ns	min
TEHICL	$\overline{CS}$ high to power down	20	20	25	30	30	ns	max

READ CYCLE : Military specification

SYMBOL	PARAMETER	65767 H-2	65767 K-2	65767 M-2	65767 N-2	UNIT	VALUE
TAVAV	READ cycle time	25	35	40	50	ns	min
TAVQV	Address access time	25	35	40	50	ns	max
TAVQX	Address valid to low Z	2	3	3	3	ns	min
TELQV	Chip-select access time	25	35	45	55	ns	max
TELQX	$\overline{CS}$ low to low Z	3	5	5	5	ns	min
TEHQZ	$\overline{CS}$ high to high Z	10	20	25	25	ns	max
TELIC	$\overline{CS}$ low to power up	0	0	0	0	ns	min
TEHICL	$\overline{CS}$ high to power down	20	25	30	30	ns	max

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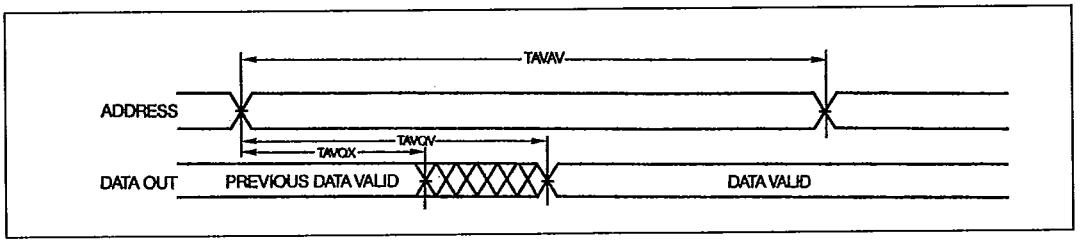
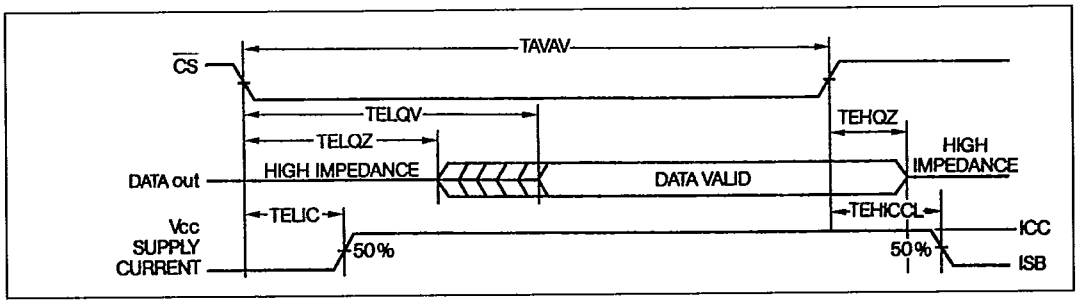
* Preliminary specification.

READ CYCLE nb 1



READ CYCLE nb 2



ORDERING INFORMATION

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Package	Device type	Grade	Level
HM1	65767 (A)	H	-5 : R

- Package: 0 - Chip form; 1 - Ceramic 20 pins; 3 - Plastic 20 pins 300 mils; 4 - LCC 20 pins; T - SOIC 20 pins
- Device type: 16 k x 1 high speed power static RAM
- Grade: F = 20 ns; H = 25 ns; K = 35 ns; M = 45 ns; N = 55 ns
- Level: -5 : Commercial; -2 : Military; -8 : Military with B.I. (B.I. = Burn-In)
- R : Tape and Reel Service

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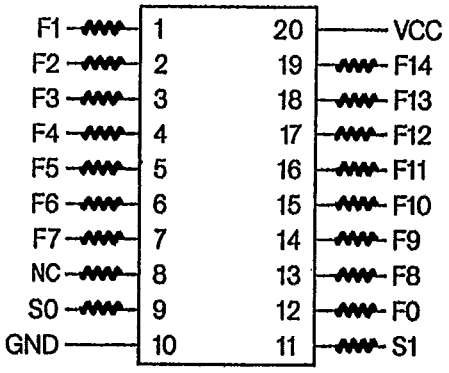
PACKAGE OUTLINE

For the packaging information, refer to chapter 10.

Package reference : Plastic DIL, 300 mils, 20 pins
SOIC DIL, 300 mils, 20 pins
Ceramic, 300 mils, 20 pins
LCC rectangular, 20 pins.

BURN-IN SCHEMATICS



R = 220 Ω per row
FO = 50 KHz ± 20 %
Fn = 1/2 F n-1

S0, S1 : programmable signals for write / read cycles

Vcc = 5.5 V

NC = Not connected