CT1698 10 MHZ TRANSCEIVER/ENCODER-DECODER

CIRCUIT DESCRIPTION:

The CT1698 is a single hybrid micro-circuit which incorporates a serial encoder, transceiver, and Manchester decoder in one package. The encoder accepts serial NRZ data in conjunction with two synchronous clocks. This data stream is then Manchester encoded and transformer coupled to a 50 ohm Tri-axial cable for transmission through up to 1000 feet of cable.

The CT1698 receiver section accepts bipolar Manchester encoded signals and passes level detected signals to the serial decoder. The serial decoder reconstructs an NRZ data stream with derived clock. This allows the data to be stored in external registers as required by the specific application.

The CT1698 has a power management function and a variable drive level option. A transmitter standby mode is available to reduce the overall power consumption of the CT1698. The variable drive level output is externally programmable for testing purposes.

FEATURES

- OPTIONAL TRANSFORMER ISOLATION

- INTERNALLY SET THRESHOLD

- MATCHED TO 50 OHM SYSTEM IMPEDANCE POWER ON AND OFF

- OPERATES WITH $\pm$ 5 VOLT SUPPLIES

- POWER MANAGEMENT

- EXTERNAL OUTPUT LEVEL ADJUSTMENT

- ACCEPTS SYNCHRONOUS INPUT DATA

- UNIQUE MANCHESTER DECODER REQUIRES NO CLOCK

- GENERATES ONE CLOCK PER RECEIVED BIT

- MAY BE USED FOR SERIAL DECODING OF INDEFINITE WORD LENGTHS

- BIPOLAR CONSTRUCTION

TRANSMISSION

The CT1698 accepts synchronous NRZ Data in conjunction with two clock signals. The NRZ data stream is then converted to Manchester code which is transformer coupled to a 50 ohm Tri-axial cable for transmission up to 1000 ft. The synchronous transfer of data allows the seperation of the CT1698 from the parallel to serial data buffer circuitry.

The transmitter may be placed into a standby condition. This reduces power consumption by approximately 600 mW. Power management is made available via two standard TTL input pins. The Receiver is always active and is not affected by the power management circuitry.

The drive level of the transmitter may be changed by adding external resistors to the drive pins. These pins allow the designer to externallly program the transmitter output level from 0.7 to 2.8 Volts peak to peak.

The transceiver is matched for 50 ohm operation over a wide band of frequencies. This condition is maintained with power on and off.

RECEPTION

The CT1698 receiver section accepts a bipolar signal which is level detected and passed to the serial decoder. The decoder section reconstructs the data and strips the clock from the serial stream. An NRZ decoded data stream is then produced synchronously with a recovered clock. The receiver is designed to meet the MIL-STD-1397 Type E requirements.
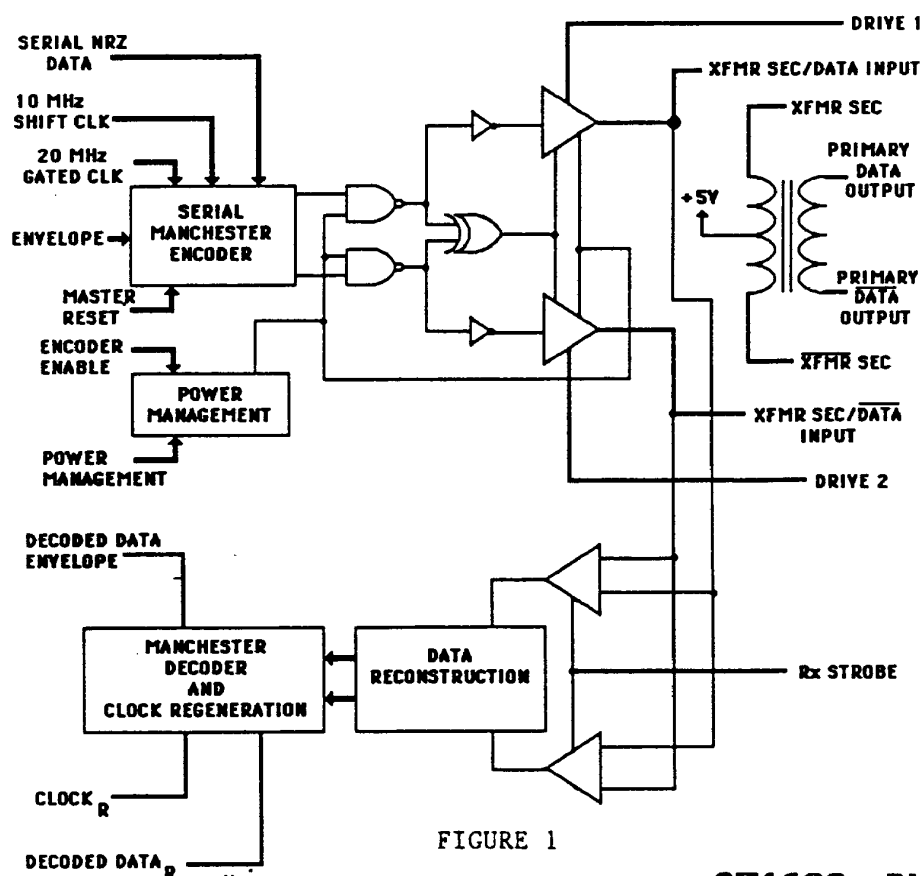

FIGURE 1

CT1698 BLOCK DIAGRAM

2

1.0 GENERAL DESCRIPTION

The specification detailed herein encompasses a hybrid Transceiver/Encoder-Decoder designed to meet the requirements of MIL-STD-1397 Type E. The transceiver is transformer coupled to the specified triaxial cable and is screened to MIL-STD-883 Method 5008.1.

2.0 ELECTRICAL REQUIREMENTS

See Figure 1 for Block Diagram. Inputs and Outputs are all Synchronous NRZ DATA STREAMS. The transformer is Internal to the package with its use being optional.
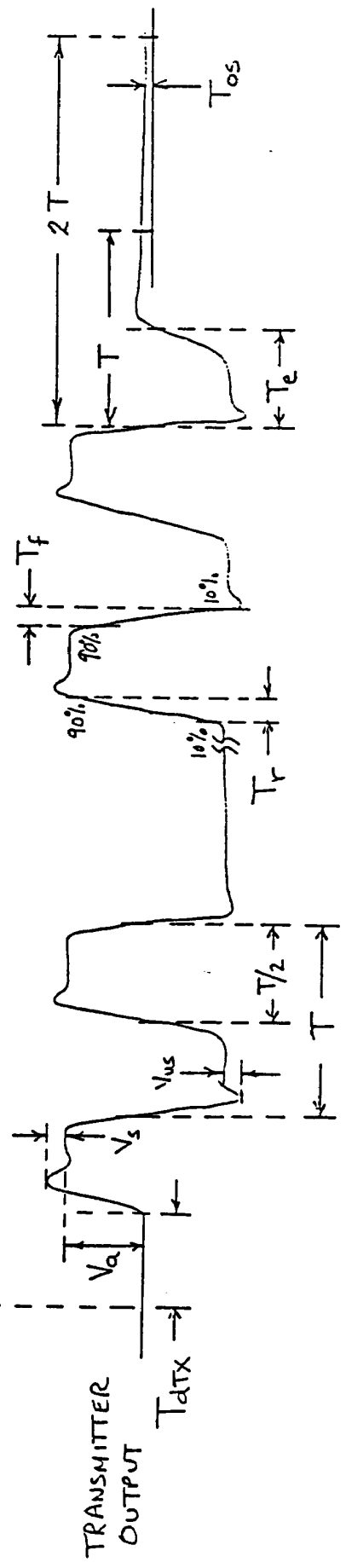
2.1 ENCODER TIMING

SYMBOL	PARAMETER/CONDITION	MIN	TYP	MAX	UNIT
ENCODE TIMING					
t_1	INPUT DATA SET-UP TIME	15		45	ns
t_2	ENCODE CLOCK SET-UP TIME	15		45	ns
t_3	ENCODE ENVELOPE SET-UP TIME	15		45	ns
t_4	ENCODE ENVELOPE TURN-OFF TIME	10		35	ns
t_5	TRANSMITTER ACTIVATION SET-UP TIME	100			ns
t_6	TRANSMITTER DEACTIVATION HOLD-TIME	50			ns
t_{w1}	20 MHZ GATED CK PULSE WIDTH HIGH	20		30	ns
t_{w2}	ENCODER SHIFT CK PULSE WIDTH HIGH	45		55	ns

ENCODER/TRANSMITTER SPECIFICATIONS CONTINUED

SYMBOL	PARAMETER/CONDITION	MIN	TYP	MAX	UNIT
OUTPUT SIGNALS					
Va	OUTPUT AMPLITUDE (SEE FIGURE 2)	0.45	0.7	0.8	VOLTS
T	PULSE PERIOD	97	100	103	ns
Ts	WIDTH OF 1ST POSITIVE HALF BIT	45		65	ns
Te	WIDTH OF LAST HALF BIT	47		65	ns
T/2	HALF PULSE PERIOD	47	50	53	ns
Tr	PULSE RISE TIME	0.05		0.3	V/ns
Tf	PULSE FALL TIME	0.05		0.3	V/ns
Vs	VOLTAGE OVERSHOOT			100	mV
Tos	OFFSET VOLTAGE 2T AFTER LAST ZERO CROSSING			30	mV
Tdtx	DELAY FROM 20 MHZ CLOCK INPUT TO DATA OUTPUT ON TXFMR. SECONDARY		20	55	ns
Zo	OUTPUT IMPEDANCE	45	50	55	ohms

ENCODER - TRANSMITTER TIMING

P1 = 50 ns ± 0.1%
P2 = 100 ns ± 0.1%
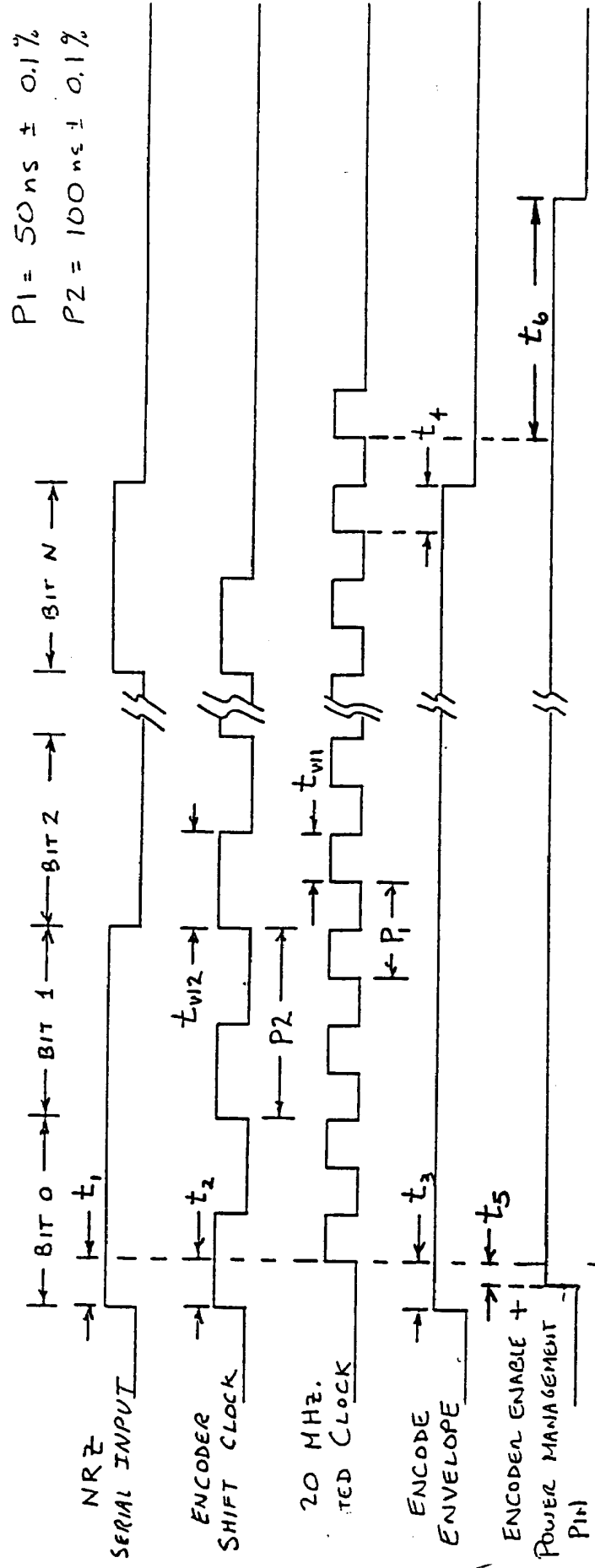
RECEIVE / DECODE TIMING   CT-1698   5/15/85

1ST DATA BIT | 2nd DATA BIT | 3rd DATA BIT | 4th DATA BIT | 5th DATA BIT

MANCHESTER II
Receiver DATA

DECODED DATA

ENVELOPE t_1 t_6

R_x STROBE t_7 t_2 t_5

DATA R

CK_R t_3 t_4 t_5
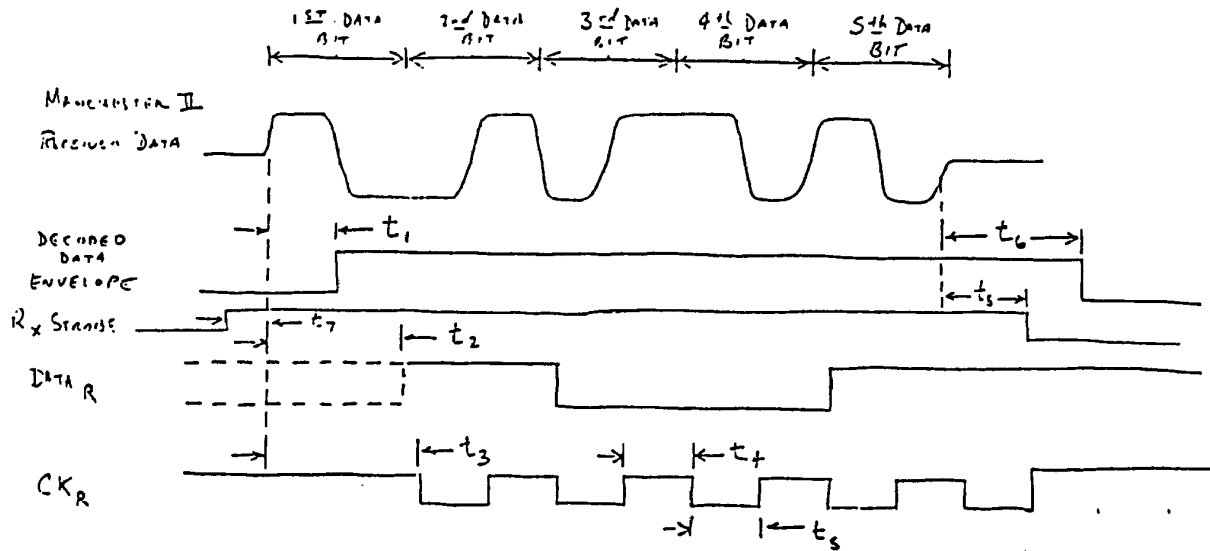
FIG 3

SYMBOL	PARAMETER/CONDITION	MIN	NOM	MAX	UNITS
t_1	ENVELOPE DELAY TIME	–	45	60	nsec
t_2	DATA DECODE DELAY	–	115	125	nsec
t_3	CLOCK LOW TRANSISTION DELAY	–	130	–	nsec
t_4	CLOCK R HIGH TIME	35	50	65	nsec
t_5	CLOCK R LOW TIME	35	50	65	nsec
t_6	TRANSMISSION ENEVELOPE OFF DELAY	120	–	270	nsec
t_7	RECEIVER STROBE ENABLE TO INPUT DATA SET-UP TIME	5			nsec
t_8	RECEIVER STROBE DISABLE TO INPUT DATA HOLD-TIME	20			

3.0 POWER MANAGEMENT FUNCTIONAL TABLE

ENCODER ENABLE (PIN 10)	POWER MANAGEMENT INPUT (PIN 9)	RECEIVER STATUS	TRANSMITTER STATUS
0	0	ACTIVE	STANDBY
X	1	ACTIVE	ACTIVE
1	X	ACTIVE	ACTIVE

POWER MANAGEMENT TIMING SEE FIGURE 2.

4.0 DRIVE LEVEL CONTROL PINS

External Resistors may be connected from pins 5 and 6 to V_{EE} or GND to change the Transmitter Output Level. If pins 5 and 6 are left open the CT1698 operates within the MIL-STD-1397 Type E specification. Resistors connected from pins 5 and 6 to V_{EE} or Ground must be equal. Unequal resistors will result in a transmitter output offset level.

The formula for peak to peak transmitter output swing with resistors connected between pins 5 and 6 to V_{ee} is:

$$V_{OUT_{pk-pk}} = 1.39 + \frac{125}{R_{EXT}} \pm 15\% \text{ VOLTS} \quad R_{EXT} \geq 90 \text{ ohms}$$

The formula for peak to peak transmitter output swing with resistors connected between pins 5 and 6 to ground is:

$$V_{OUT_{pk-pk}} = 1.39 - \frac{50 \ (V_{EE} - 2.5)}{R_{EXT}} \pm 15\% \text{ VOLTS} \geq 180 \text{ ohms}$$

5.0 FUNCTIONAL DESCRIPTION AND PINOUTS

PIN #	PIN NAME	FUNCTION	LOAD OR DRIVE
1	XFMR PRIMARY/TX DATA OUPUT	TRANSFORMER LEAD FOR CONNECTION TO CENTER CONDUCTOR OF TRI-AXIAL CABLE	
2	XFMR SECONDARY	SECONDARY ISOLATED WINDING, SAME PHASE AS CENTER CONDUCTOR.	
3	XFMR SECONDARY/ RX DATA INPUT	TRANSMITER-RECIEVER I/O PIN	
4	NO CONNECTION		
5	DRIVE 2	OUTPUT LEVEL ADJUSTMENT SELECTED BY RESISTOR TO GND OR V_{EE}	
6	DRIVE 1	OUTPUT LEVEL ADJUSTMENT SELECTED BY RESISTOR TO GND OR V_{EE}	
7	-5 VOLTS		
8	R_X STROBE	LOW LEVEL DISABLES RECEIVER	3 S LOADS
9	POWER MANAGEMENT INPUT	CONTROLS TRANSMITTER POWER CONSUMPTION IN CONJUNCTION WITH PIN 10	1 S LOAD
10	ENCODER ENABLE	CONTROLS TRANSMITTER POWER CONSUMPTION IN CONJUNCTION WITH PIN 9	1 S LOAD
11	CASE/SIGNAL GND		
12	CASE/SIGNAL GND		
13	DECODED DATA ENVELOPE	HIGH AFTER RECEPTION OF FIRST HALF BIT; GOES LOW AFTER RECEPTION OF LAST HALF BIT (NORMALLY LOW IN INACTIVE STATE).	4 S DRIVE
14	TP3 TEST POINT	ALINGMENT POINT: NO ELECTRICAL CONNECTION PERMITTED	
15	TP1 TEST POINT	ALINGMENT POINT: NO ELECTRICAL CONNECTION PERMITTED	
16	TP2 TEST POINT	ALINGMENT POINT: NO ELECTRICAL CONNECTION PERMITTED	
17	-5 VOLTS		
18	TP4 TEST POINT	ALINGMENT POINT: NO ELECTRICAL CONNECTION PERMITTED	
19	$CLOCK_R$	RECONSTRUCTED CLOCK; ONE CLOCK PULSE PER INPUT BIT RECEIVED	3 S DRIVE

5.0 FUNCTIONAL DESCRIPTION AND PINOUTS CONTINUED

PIN #	PIN NAME	FUNCTION	DRIVE
20	NO CONNECTION		
21	DECODED DATA$_R$	NRZ RECONSTRUCTED DATA. SAMPLED ON CLOCK$_R$ RISING EDGE.	3 S DRIVE
22	NO CONNECTION		
23	+5 VOLTS		
24	+5 VOLTS		
25	10MHz ENCODER SHIFT CLOCK	ONE CYCLE REQUIRED PER DATA BIT. MUST BE HIGH IN FIRST HALF OF BIT CELL.	1 S LOAD
26	NRZ SERIAL INPUT DATA	SERIAL INPUT TO BE MANCHESTER ENCODED WITH THE 20 MHz GATED CK.	1 S LOAD
27	INPUT DATA ENVELOPE	MUST BE HIGH TO ENABLE TRANSMISSION MUST GO LOW BEFORE RECEPTION OF LAST 20 MHz POSITIVE EDGE TO COMPLETE TRANSMISSION.	1 S LOAD
28	20 MHz GATED CLOCK (ENCODER)	EACH BIT TO BE ENCODED REQUIRES TWO POSITIVE EDGES OF THE 20 MHz CK. THESE EDGES MUST OCCUR AT 25 ns AND 75 ns INTO THE BIT CELL. THE END OF TRANSMISSION REQUIRES AN ADDITIONAL EDGE IN CONJUNCTION WITH A LOGIC LOW ON THE ENCODE ENVELOPE. t_R, $t_F \leq 5$ nsec.	1 S LOAD
29	MASTER $\overline{\text{RESET}}$	LOGIC LOW RESETS ENCODER RESET PULSE $\geq$ 15 nsec.	2 S LOAD
30	NO CONNECTION		
31	NO CONNECTION		
32	$\overline{\text{XFMR}}$ SECONDARY/RX $\overline{\text{DATA}}$ INPUT	TRANSMITTER-RECEIVER I/O PIN	
33	$\overline{\text{XFMR}}$ SECONDARY	SECONDARY ISOLATED WINDING, SAME PHASE AS OUTER CONDUCTER	
34	$\overline{\text{XFMR}}$ PRIMARY/TX $\overline{\text{DATA}}$ OUTPUT	TRANSFORMER LEAD FOR CONNECTION TO OUTER CONDUCTOR OF TRI-AXIAL	

5.1 LOAD AND DRIVE DEFINITIONS:

1 S LOAD: REQUIRES I_{IL} = -2mA MAX., V_{IL} = 0.8V MAX

I_{IH} = 50 uA MAX., V_{IH} = 2.5V MIN C_{IN} < 15 pf

1 S DRIVE: I_{OH} = 50 uA MIN., V_{OH} = 2.5V MIN

I_{OL} = -2 mA MIN., V_{OL} = 0.5V MAX

6.0 1698 POWER CONSUMPTION

	CURRENT (mA)	
	TYP	MAX
I_{CC} STANDBY MODE	325	450
I_{EE} STANDBY MODE	85	105
I_{CC} 100% TRANSMISSION	380	510
I_{EE} 100% TRANSMISSION	125	160

7.0 ABSOLUTE MAXIMUM RATINGS

V_{CC} (Pins 23, 24)   + 7 Volts Max

V_{EE} (Pins 7, 17)   - 7 Volts Max

Logic Input Voltage Applied:

Logic Low   -1.2V @ 10mA Max

Logic High   +5.5 Volts

Damage will not result from the following faults to the transformer secondary:

- Short circuit line to line

- Short circuit to ground

- Short circuit to Vs when $-50 \leq V_S \leq +50V$

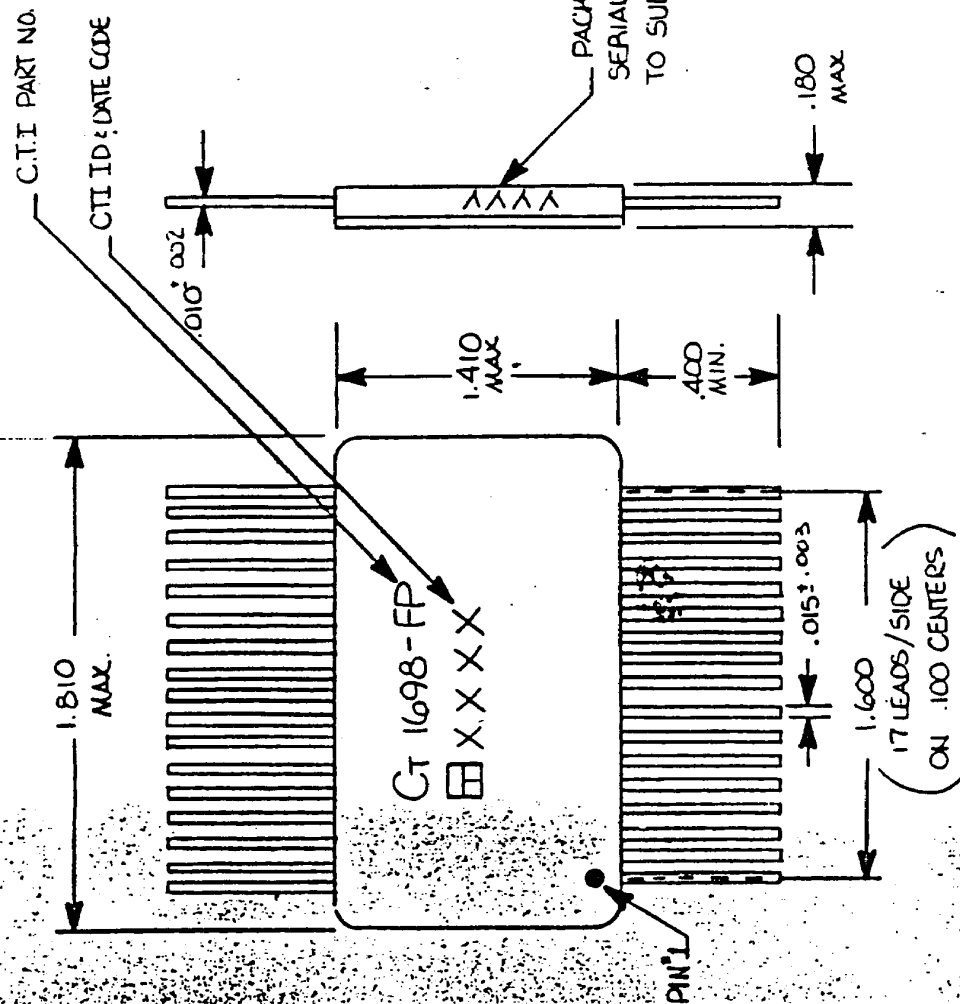- 120 VAC 60 HZ Common Mode Signal

7.1 ENVIRONMENTAL PARAMETERS

OPERATING TEMPERATURE -55°C to +100°C

STORAGE TEMPERATURE   -65°C to +150°C

Screned per MIL-STD-883B METHOD 5008 except as outlined here.

Burn-in: 168 Hours at +100°C case temperature.

(11)

NOTES:

1. PACKAGE LEADS TO BE OF AN IRON-NICKEL ALLOY AS PER MIL-I-23011, CLASS I.
2. LEAD SEALS TO BE OF BOROSILICATE GLASS, OPAQUE.
3. ALL TOLERANCES TO BE ±.005 UNLESS OTHERWISE NOTED.
4. PACKAGE MUST MEET C.T.I. SPEC 07-1000.
5. PLATING
   A. GOLD 50-225 μINCHES OVER ELECTROLYTIC NICKEL 50-150 μINCHES
   B. ELECTROLYTIC NICKEL 50-150 μINCHES
6. TOP SURFACE OF PINS SHALL LIE IN THE SAME PLANE AS 'X' WITHIN ±.005 AND 80% OF TOP SURFACE ON EACH PIN SHALL BE FLAT WITHIN 3°

FIG 4

SECTION A-A

DASH	A	B	C	D	PLATING BODY	LEADS
1	.030	.270	.160	.120	NOTE 5B	NOTE 5A
2	.030	.270	.160	.120	NOTE 5A	NOTE 5A

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REV	DATE	ECN		DRW	DES	MFG	EE	QC
A	4·4·85	⁄⁄	RELEASE	⁒·⁒	⁒·⁒	PK	⁑	JV

CTI PKG: 02-1135-1
C.T.I LID : 08-1052 83

PACKAGES TO BE
SERIALIZED PRIOR
TO SUBSTRATE ATTACH.

.180
MAX

C.T.I PART NO.

CTI ID & DATE CODE

.010±.002

1.410
MAX

.400
MIN.

Cτ 1698-FP
⊞ XXXX

1.810
MAX.

1.600
(17 LEADS/SIDE
ON .100 CENTERS)

.015±.003

PIN"1

ITEM	QTY	MATERIAL		DWG NO.

COMPONENTS LIST

Circuit Technology Incorporated
FARMINGDALE, NEW YORK

	NAME	DATE		
APPROVAL			SIZE A	FSCM NO. 3116
DWN				
DES	GVS	4-11-85	SCALE ½	PART NO.
MFG	PK	4-17-85		Cτ 1698-FP
EE	·A	4/11/14	SHEET 1 OF 1	DWG. NO. 21-2051
QC	JV	5/28/85		REV A

TITLE 1.800 X 1.400
34 LEAD FLAT PACK

CTI
Circuit Technology Incorporated