

T1/E1 Line Interface

Features

- Provides Analog Transmission Line Interface for T1 and E1 Applications
- Provides Line Driver, and Clock and Data Recovery Functions
- Internal Generation of Transmitted Pulse Width and Pulse Shape
- Low Power Consumption (typically 175 mW)
- Minimum External Components (no external crystal required)
- 14 dB of Transmitter Return Loss

General Description

The CS6158 and CS6158A combine the complete analog transmit and receive line interface for T1 or E1 applications in a low power, 28-pin device operating from a +5V supply.

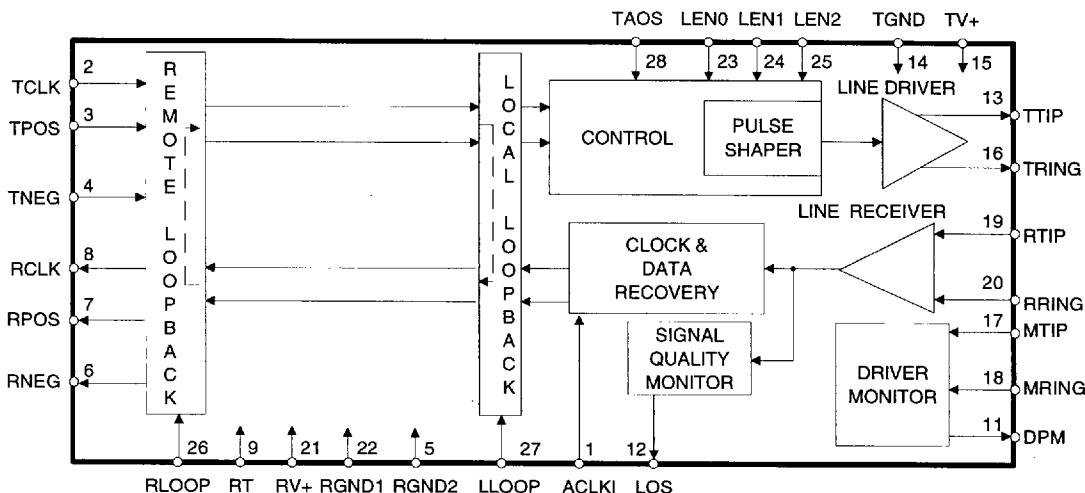
The receiver uses a digital Delay-Locked-Loop which is continuously calibrated from an external reference to provide excellent stability and jitter tolerance. The transmitter features internal pulse shaping. The CS6158A provides a matched, constant impedance output stage to insure signal quality on mismatched, poorly terminated lines.

Applications

- Central Office Exchanges
- Digital Access and Cross Connect Systems
- Large PABX's

ORDERING INFORMATION

CS6158A-IP1	28 Pin Plastic DIP
CS6158A-IL1	28 Pin Plastic PLCC
CS6158-IP1	28 Pin Plastic DIP
CS6158-IL1	28 Pin Plastic PLCC



ABSOLUTE MAXIMUM RATINGS

Parameter	Symbol	Min	Max	Units
DC Supply (referenced to GND)	RV+ TV+	- -	6.0 (RV+) + 0.3	V V
Input Voltage, Any Pin (Note 1)	V _{in}	RGND - 0.3	(RV+) + 0.3	V
Input Current, Any Pin (Note 2)	I _{in}	-10	10	mA
Ambient Operating Temperature	T _A	-40	85	°C
Storage Temperature	T _{stg}	-65	150	°C

WARNING: Operations at or beyond these limits may result in permanent damage to the device.

Normal operation is not guaranteed at these extremes.

Notes: 1. Excluding RTIP, RRING, which must stay within -6V to (RV+) + 0.3V.

2. Transient currents of up to 100 mA will not cause SCR latch-up. Also TTIP, TRING, TV+ and TGND can withstand a continuous current of 100 mA.

RECOMMENDED OPERATING CONDITIONS

Parameter	Symbol	Min	Typ	Max	Units
DC Supply (Note 3)	RV+, TV+	4.75	5.0	5.25	V
Ambient Operating Temperature	T _A	-40	25	85	°C
Power Consumption CS6158 (Notes 4, 5)	P _C	-	620	760	mW
CS6158A (Notes 4, 5)	P _C	-	290	350	mW
Power Consumption CS6158 (Notes 4, 6)	P _C	-	400	-	mW
CS6158A (Notes 4, 6)	P _C	-	175	-	mW

Notes: 3. TV+ must not exceed RV+ by more than 0.3V.

4. Power consumption while driving the load over operating temperature range. Includes IC and load. Digital input levels are within 10% of the supply rails and digital outputs are driving a 50 pF capacitive load.

5. Assumes 100% ones density and maximum line length at 5.25V.

6. Assumes 50% ones density and 300ft. line length at 5.0V.

DIGITAL CHARACTERISTICS (T_A = -40°C to 85°C; TV+, RV+ = 5.0V ±5%; GND = 0V)

Parameter	Symbol	Min	Typ	Max	Units
High-Level Input Voltage (Note 7) PINS 1-4, 23-28	V _{IH}	2.0	-	-	V
Low-Level Input Voltage (Note 7) PINS 1-4, 23-28	V _{IL}	-	-	0.8	V
High-Level Output Voltage (Notes 7, 8) CS6158 I _{OUT} = -40 μA PINS 6-8, 11, 12	V _{OH}	2.4	-	-	V
CS6158A I _{OUT} = -40 μA PINS 6-8, 11, 12	V _{OH}	4.0	-	-	V
Low-Level Output Voltage (Notes 7, 8) I _{OUT} = 1.6 mA PINS 6-8, 11, 12	V _{OL}	-	-	0.4	V
Input Leakage Current Except Pin 5		-	-	±10	μA

Notes: 7. This specification guarantees TTL compatibility (V_{OH} = 2.4V @ I_{OUT} = -40μA).

8. Output drivers will output CMOS logic levels into a CMOS load.

ANALOG SPECIFICATIONS (TA = -40°C to 85°C; TV+, RV+ = 5.0V ±5%; GND = 0V)

Parameter	Min	Typ	Max	Units
Transmitter				
AMI Output Pulse Amplitudes (Note 9)				
E1, 75 Ω (Note 10)	2.14	2.37	2.6	V
E1, 120 Ω (Note 11)	2.7	3.0	3.3	V
T1, FCC Part 68 (Note 12)	2.7	3.0	3.3	V
T1, DSX-1 (Note 13)	2.4	3.0	3.6	V
E1 Zero (space) level (LEN2/1/0 = 0/0/0)				
75Ω application (Note 10)	-0.237	-	0.237	V
120Ω application (Note 11)	-0.3	-	0.3	V
Load Presented To Transmitter Output (Note 9)				
CS6158	-	25	-	Ω
CS6158A	-	75	-	Ω
Jitter Added by the Transmitter (Note 14)				
10Hz - 8kHz	-	0.005	0.02	UI
8kHz - 40kHz	-	0.008	0.025	UI
10Hz - 40kHz	-	0.010	0.025	UI
Broad Band	-	0.015	0.05	UI
Power in 2kHz band about 772kHz (Notes 9, 15)	12.6	15	17.9	dBm
Power in 2kHz band about 1.544MHz (Notes 9, 15)	-29	-38	-	dB
(referenced to power in 2kHz band at 772kHz)				
Positive to Negative Pulse Imbalance (Notes 9, 15)				
T1, DSX-1	-	0.2	0.5	dB
E1 amplitude at center of pulse	-5	-	5	%
E1 pulse width at 50% of nominal amplitude	-5	-	5	%
CS6158A Transmitter Return Loss (Notes 9, 15, 16)				
51 kHz to 102 kHz	8	-	-	dB
102 kHz to 2.048 MHz	14	-	-	dB
2.048 MHz to 3.072 MHz	10	-	-	dB
CS6158A Transmitter Short Circuit Current (Notes 9, 17)	-	-	50	mA RMS

Notes: 9. Using a 0.47 μF capacitor in series with the primary of a transformer recommended in the Applications Section.

- Amplitude measured at the transformer (CS6158A-1:1 or 1:1.26, CS6158-1:2) output across a 75 Ω load for line length setting LEN2/1/0 = 0/0/0. The CS6158 requires a 4.4Ω resistor in series with the TTIP or TRING pin for this application only.
- Amplitude measured at the transformer (CS6158A-1:1.26, CS6158-1:2) output across a 120 Ω load for line length setting LEN2/1/0 = 0/0/0.
- Amplitude measured at the transformer (CS6158A-1:1.15, CS6158-1:2) output across a 100 Ω load for line length setting LEN2/1/0 = 0/1/0.
- Amplitude measured across a 100 Ω load at the DSX-1 Cross-Connect for line length settings LEN2/1/0 = 0/1/1, 1/0/0, 1/0/1, 1/1/0 and 1/1/1 after the length of #22 AWG ABAM equivalent cable specified in Table 1. The CS6158A requires a 1:1.15 transformer and the CS6158 requires a 1:2.
- Input signal to RTIP/RRING is jitter free. Values will reduce slightly if jitter free clock is input to TCLK.
- Not production tested. Parameters guaranteed by design and characterization.
- Return loss = $20 \log_{10} \left(\frac{z_1 + z_0}{z_1 - z_0} \right)$ where z_1 = impedance of the transmitter, and z_0 = impedance of line load. Measured with a repeating 1010 data pattern with LEN2/1/0 = 0/0/0 and a 1:1 transformer terminated with a 75Ω load, or a 1:1.26 transformer terminated with a 120Ω load.
- Measured broadband through a 0.5 Ω resistor across the secondary of a 1:1.26 transformer during the transmission of an all ones data pattern for LEN2/1/0 = 0/0/0.

ANALOG SPECIFICATIONS (TA = -40°C to 85°C; TV+, RV+ = 5.0V ±5%; GND = 0V)

Parameter	Min	Typ	Max	Units
Receiver				
CS6158A RTIP/RRING Input Impedance	-	50k	-	Ω
Sensitivity Below DSX (0dB = 2.4V)				
CS6158	-10	-	-	dB
CS6158A	-13.6	-	-	dB
CS6158A Data Decision Threshold				
T1, DSX-1 (Note 18)	60	65	70	% of peak
T1, DSX-1 (Note 19)	53	65	77	% of peak
T1, FCC Part 68 and E1 (Note 20)	45	50	55	% of peak
CS6158 Data Decision Threshold				
T1	-	65	-	% of peak
E1	-	50	-	% of peak
Allowable Consecutive Zeros before LOS (Note 21)	160	175	190	bits
Receiver Input Jitter Tolerance (Note 22)				
10kHz - 100kHz	0.4	-	-	UI
2kHz	6.0	-	-	UI
10Hz and below	300	-	-	UI
Loss of Signal Threshold				
CS6158A (Note 21)	0.25	0.30	0.50	V
CS6158	-	0.30	-	V
Driver Performance Monitor				
CS6158A MTIP/MRING Sensitivity:				
Differential Voltage Required for Detection	-	0.6	-	V

Notes: 18. For input amplitude of 1.2 V_{pk} to 4.14 V_{pk}.

19. For input amplitude of 0.5 V_{pk} to 1.2 V_{pk} and from 4.14 V_{pk} to RV+.

20. For input amplitude of 1.05 V_{pk} to 3.3 V_{pk}.

21. LOS goes high after 160 to 190 consecutive zeros are received. A zero is output on RPOS and RNEG for each bit period where the input signal amplitude remains below the data decision threshold. The analog input squelch circuit operates when the input signal amplitude above ground on the RTIP and RRING pins falls within the range of 0.25V to 0.50V long enough for the internal slicing threshold to decay within this range. Operation of the squelch causes zeros to be output on RPOS and RNEG as long as the input amplitude remains below 0.25V. During receive LOS, pulses greater than 0.25V in amplitude may be output on RPOS and RNEG. LOS returns low after the ones density reaches 12.5% (based upon 175 bit periods starting with a one and containing less than 100 consecutive zeros) as prescribed in ANSI T1.231-1993.

22. Jitter tolerance increases at lower frequencies. See Figure 7.

T1 SWITCHING CHARACTERISTICS

(TA = -40°C to 85°C; TV+, RV+ = 5.0V ±5%;
GND = 0V; Inputs: Logic 0 = 0V, Logic 1 = RV+; See Figures 1, 2, & 3)

Parameter			Symbol	Min	Typ	Max	Units
TCLK Frequency			f _{tclk}	-	1.544	-	MHz
TCLK Pulse Width			t _{pwh2}	150	-	500	ns
ACLKI Duty Cycle			t _{pwh3} /t _{pw3}	40	-	60	%
ACLKI Frequency (Note 23)			f _{ackli}	-	1.544	-	MHz
RCLK Duty Cycle	CS6158	(Notes 24, 25, 26)	t _{pwh1} /t _{pw1}	-	78	-	%
	CS6158A	(Notes 24, 25, 26)		-	29	-	%
RCLK Cycle Width (Notes 24, 25, 26)			t _{pw1}	320	648	980	ns
RCLK High Time	CS6158	(Notes 24, 25, 26)	t _{pwh1}	-	508	-	ns
	CS6158A	(Notes 24, 25, 26)		130	190	240	ns
RCLK Low Time	CS6158	(Notes 24, 25, 26)	t _{pw1}	100	140	-	ns
	CS6158A	(Notes 24, 25, 26)		100	458	850	ns
Rise Time, All Digital Outputs (Note 27)			t _r	-	-	85	ns
Fall Time, All Digital Outputs (Note 27)			t _f	-	-	85	ns
TPOS/TNEG to TCLK Falling Setup Time			t _{su2}	25	-	-	ns
TCLK Falling to TPOS/TNEG Hold Time			t _{h2}	25	-	-	ns
RPOS/RNEG Valid Before RCLK Rising (Notes 25, 26)			t _{su1}	50	-	-	ns
RPOS/RNEG Valid After RCLK Rising (Notes 25, 26)			t _{h1}	50	-	-	ns

Notes: 23. ACLKI may be provided by an external source or TCLK, but *not* RCLK.

24. RCLK cycle width will vary with extent by which received pulses are displaced by jitter.

25. Max and Min RCLK duty cycles and pulse widths are for worst case jitter conditions: i.e. 0.4 UI AMI data displacement for T1 or 0.2 UI AMI data displacement for E1. See text section on *Jitter and Recovered Clock*.

26. Not production tested. Guaranteed by design and/or characterization.

27. At max load of 1.6 mA and 50 pF.

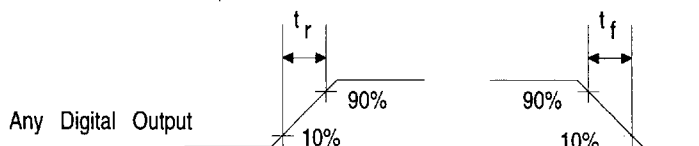


Figure 1. Signal Rise and Fall Characteristics

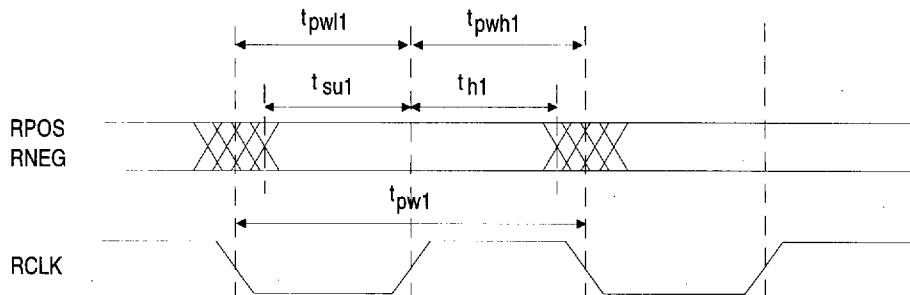


Figure 2. Recovered Clock and Data Switching Characteristics

E1 SWITCHING CHARACTERISTICS (TA = -40°C to 85°C; TV+, RV+ = 5.0V ±5%; GND = 0V; Inputs: Logic 0 = 0V, Logic 1 = RV+; See Figures 1, 2, & 3)

Parameter			Symbol	Min	Typ	Max	Units
TCLK Frequency			f_{clk}	-	2.048	-	MHz
TCLK Pulse Width	CS6158	(Note 28)	t_{pwh2}	215	-	258	ns
	CS6158A			150	-	340	ns
ACLKI Duty Cycle			$t_{\text{pwh3}}/t_{\text{pw3}}$	40	-	60	%
ACLKI Frequency			f_{ackli}	-	2.048	-	MHz
RCLK Duty Cycle	CS6158	(Notes 24, 25, 26)	$t_{\text{pwh1}}/t_{\text{pw1}}$	-	71	-	%
	CS6158A	(Notes 24, 25, 26)		-	29	-	%
RCLK Cycle Width	CS6158	(Notes 24, 25, 26)	t_{pw1}	320	488	670	ns
	CS6158A	(Notes 24, 25, 26)		310	488	670	ns
RCLK High Time	CS6158	(Notes 24, 25, 26)	t_{pwh1}	-	348	-	ns
	CS6158A	(Notes 24, 25, 26)		90	140	190	ns
RCLK Low Time	CS6158	(Notes 24, 25, 26)	t_{pwl1}	100	140	-	ns
	CS6158A	(Notes 24, 25, 26)		120	348	500	ns
Rise Time, All Digital Outputs			t_r	-	-	85	ns
Fall Time, All Digital Outputs			t_f	-	-	85	ns
TPOS/TNEG to TCLK Falling Setup Time			t_{su2}	25	-	-	ns
TCLK Falling to TPOS/TNEG Hold Time			t_{h2}	25	-	-	ns
RPOS/RNEG Valid Before RCLK Rising			t_{su1}	50	-	-	ns
RPOS/RNEG Valid After RCLK Rising			t_{h1}	50	-	-	ns

Notes: 28. The transmitted pulse width of LEN2/1/0 = 0/0/0 is tied to the high cycle of TCLK for the CS6158 only.

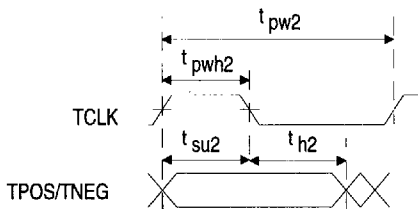


Figure 3a. Transmit Clock and Data Switching Characteristics

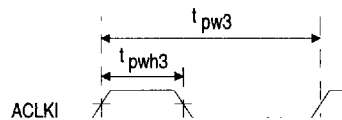


Figure 3b. Alternate External Clock Characteristics

THEORY OF OPERATION

Enhancements in CS6158A

The CS6158A provides higher performance and more features than the CS6158 including:

- 50% reduction in power consumption
- 14 dB of transmitter return loss (during marks and spaces) improves signal quality.
- The E1 transmitted pulse width is set internally by the CS6158A (and not by the TCLK input duty cycle).
- Upon power up, RCLK immediately starts and LOS (loss of signal) is set high.
- When the transmitter senses the absence of a signal on TCLK, TTIP and TRING are forced to zero.
- ANSI T1.231-1993 compliant receiver LOS (Loss Of Signal) handling.
- The driver performance monitor operates over a wider range of input signal levels.

CS6158 designs can be converted to the higher performance, pin-compatible CS6158A if the transmit transformer is replaced by a pin-compatible transformer with a new turns ratio.

Transmitter

The transmitter takes data from a T1 (or E1) terminal and produces pulses of appropriate shape. The transmit clock (TCLK) and transmit data (TPOS & TNEG) are supplied synchronously. Data is sampled on the falling edge of the input clock.

Either T1 (DSX-1 or Network Interface) or CCITT G.703 pulse shapes may be selected. Pulse shaping and signal level are determined by "line length select" inputs as shown in Table 1. The CS6158A line driver is designed to drive a 75 Ω equivalent load. The CS6158 drives a 25 Ω load.

LEN2	LEN1	LEN0	Option Selected	Application
0	1	1	0-133 FEET	DSX-1 ABAM (AT&T 600B or 600C)
1	0	0	133-266 FEET	
1	0	1	266-399 FEET	
1	1	0	399-533 FEET	
1	1	1	533-655 FEET	RESERVED
0	0	1		
0	0	0	75 Ω and 120 Ω	E1 CCITT G.703
0	1	0	FCC PART 68, OPT. A	T1 NETWORK INTERFACE
0	1	1	ANSI T1.403	

Table 1. Line Length Selection

For E1 applications, the CS6158A driver provides 14 dB of return loss during the transmission of both marks and spaces. This improves signal quality by minimizing reflections off the transmitter. Similar levels of return loss are provided for T1 applications.

For T1 DSX-1 applications, line lengths from 0 to 655 feet (as measured from the IC to the DSX-1 cross connect) are selectable. The five partition arrangement meets CB-119 requirements when using ABAM cable. A typical output pulse is shown in Figure 4. These pulse settings can also be used to meet CCITT pulse shape requirements for 1.544 MHz operation.

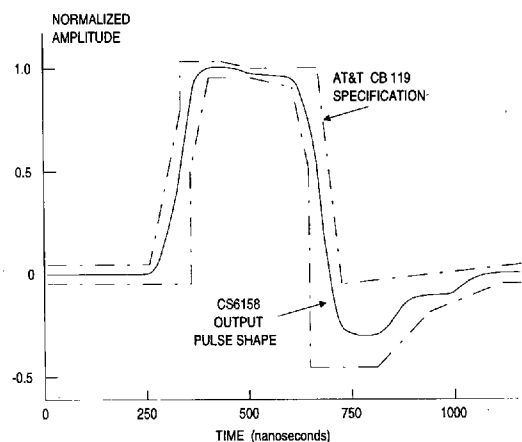


Figure 4 - Typical Pulse Shape at DSX-1 Cross Connect

	For coaxial cable, 75 Ω load and transformer specified in Application Section.	For shielded twisted pair, 120 Ω load and transformer specified in Application Section.
Nominal peak voltage of a mark (pulse)	2.37 V	3 V
Peak voltage of a space (no pulse)	0 \pm 0.237 V	0 \pm 0.30 V
Nominal pulse width	244 ns	
Ratio of the amplitudes of positive and negative pulses at the center of the pulse interval	0.95 to 1.05*	
Ratio of the widths of positive and negative pulses at the nominal half amplitude	0.95 to 1.05*	

* When configured with a 0.47 μ F nonpolarized capacitor in series with the TX transformer primary as shown in Figure A1.

Table 2. CCITT G.703 Specifications

For T1 Network Interface applications, additional options are provided. Note that the optimal pulse width for Part 68 (324 ns) is narrower than the optimal pulse width for DSX-1 (350 ns). The CS6158A automatically adjusts the pulse width based upon the "line length" selection made.

The E1 CCITT G.703 pulse shape is supported with line length selection LEN2/1/0=0/0/0. The

pulse width will meet the G.703 pulse shape template shown in Figure 5, and specified in Table 2.

Only in the case of CS6158 and LEN2/1/0=0/0/0, the width of this pulse is determined by the high cycle of TCLK. The pulse will meet the CCITT pulse shape template shown in Figure 5 assuming the TCLK duty cycle and frequency are appropriate. The rising and falling edge of TCLK control the time at which the rising and falling edges of the output pulse occur.

The CS6158A transmitter will detect a failed TCLK, and will insure that neither TTIP nor TRING gets stuck high. If the clock signal is removed from TCLK on the CS6158, TPOS and TNEG should both be low during the last falling edge of TCLK. This places the CS6158 in a low-power dissipation mode.

When any transmit control pin (TAOS, LEN0-2 or LLOOP) is toggled, the transmitter stabilizes within 22 bit periods. The transmitter will take longer to stabilize when RLOOP is selected because the timing circuitry must adjust to the new frequency.

Transmit All Ones Select

The transmitter provides for all ones insertion at the frequency of TCLK. Transmit all ones is selected when TAOS goes high, and causes

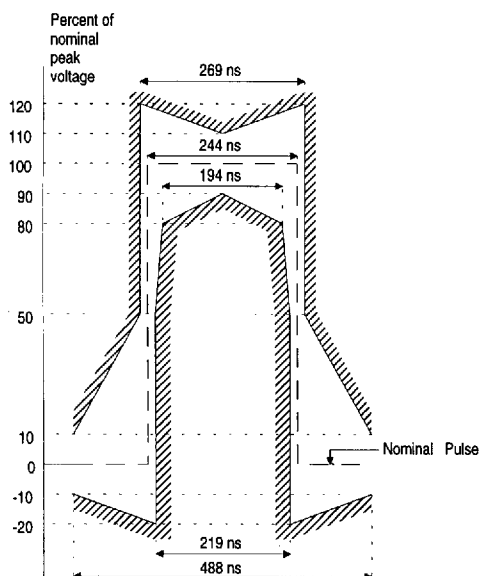


Figure 5 - Mask of the Pulse at the 2048 kbps Interface

continuous ones to be transmitted on the line (TTIP and TRING). In this mode, the TPOS and TNEG inputs are ignored. If Remote Loopback is in effect, any TAOS request will be ignored.

Receiver

The receiver extracts data and clock from an AMI (Alternate Mark Inversion) coded signal and outputs clock and synchronized data. The receiver is sensitive to signals down to approximately 300 mV in amplitude and requires no equalization or ALBO (Automatic Line Build Out) circuits. The signal is received on both ends of a center-tapped, center-grounded transformer. The transformer is center tapped on the CS6158A or CS6158 side. The clock and data recovery circuit exceeds the jitter tolerance specifications of Publications 43802, 43801, 62411 amended, TR-TSY-000170, and CCITT REC. G.823.

A block diagram of the receiver is shown in Figure 6. The two leads of the transformer (RTIP and RRING) have opposite polarity allowing the receiver to treat RTIP and RRING as unipolar signals. Comparators are used to detect pulses on

RTIP and RRING. The comparator thresholds are dynamically established at a percent of the peak level (50% of peak for E1, 65% of peak for T1; with the slicing level selected by LEN2/1/0 inputs).

The receiver uses an edge detector and a continuously calibrated delay line to generate the recovered clock. The delay line divides its reference clock, ACLKI, into 13 equal divisions of phases. Continuous calibration ensures timing accuracy, even if temperature or power supply voltage fluctuate.

The leading edge of an incoming data pulse triggers the clock phase selector. The phase selector chooses one of the 13 available phases which the delay line produces for each bit period. The output from the phase selector feeds the clock and data recovery circuits which generate the recovered clock and sample the incoming signal at appropriate intervals to recover the data. The jitter tolerance of the receiver exceeds that plot shown in Figure 7.

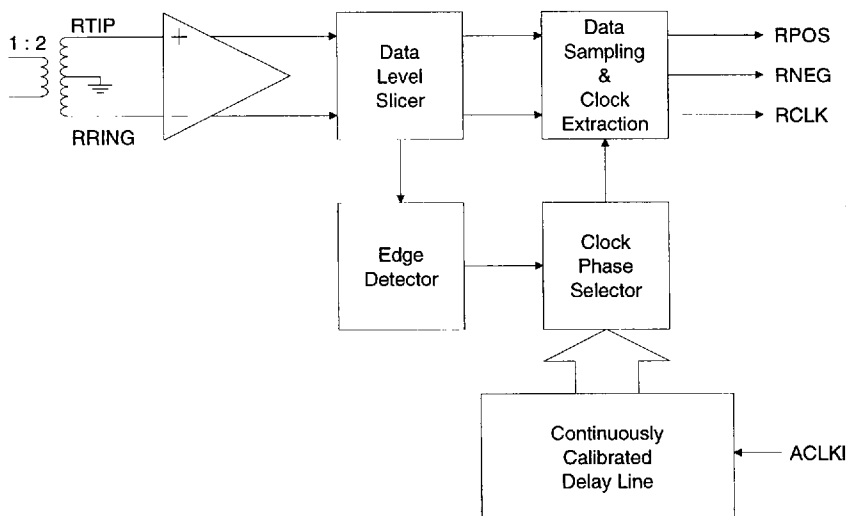


Figure 6. - Receiver Block Diagram

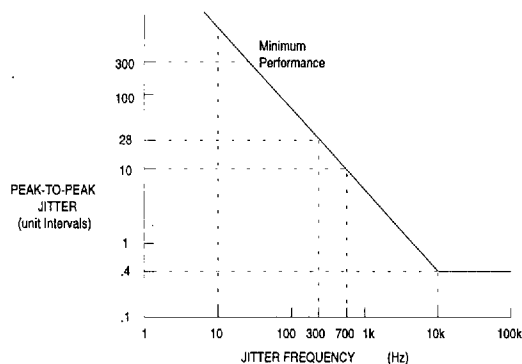


Figure 7. - Input Jitter Tolerance of Receiver

The CS6158 device outputs a clock at RCLK after the first signal is input to RTIP/RRING. The CS6158A outputs a clock on RCLK immediately upon power-up. In either case, the clock recovery circuit is calibrated, and the device will lock onto the AMI data input immediately. If loss of signal occurs, the RCLK frequency will equal the ACLKI frequency.

Data on RPOS and RNEG is stable and may be sampled on the rising edge of RCLK, the recovered clock.

Jitter and Recovered Clock

The CS6158A and CS6158 are designed for error free clock and data recovery from an AMI encoded data stream in the presence of more than 0.4 unit intervals of jitter at high frequency. The clock recovery circuit is also tolerant of long strings of zeros. The edge of an incoming data bit causes the circuitry to choose a phase from the delay line which most closely corresponds with the arrival time of the data edge, and that clock phase triggers a pulse which is typically 140 ns in duration. This phase of the delay line will continue to be selected until data bit arrives which is closer to another of the 13 phases, causing a new

phase to be selected. The largest jump allowed along the delay line is six phases.

When an input signal is jitter free, the phase selection will occasionally jump between two adjacent phases resulting in RCLK jitter with an amplitude of 1/13 UI. These single phase jumps are due to differences in frequency of the incoming data and the calibration clock input to ACLKI. For T1 operation of the CS6158A and CS6158, the instantaneous period can be $14/13 * 648 \text{ ns} = 698 \text{ ns}$ (1,662,769 Hz) or $12/13 * 648 \text{ ns} = 598 \text{ ns}$ (1,425,231 Hz) when adjacent clock phases are chosen. As long as the same phase is chosen, the period will be 648 ns. Similar calculations hold for the 2.048 MHz rate.

The clock recovery circuit is designed to accept at least 0.4 UI of jitter at the receiver. Since the data stream contains information only when ones are transmitted, a clock/data recovery circuit must assume a zero when no signal is measured during a bit period. Likewise, when zeros are received, no information is present to update the clock recovery circuit regarding the trend of a signal which is jittered. The result is that two ones that are separated by a string of zeros can exhibit maximum deviation in pulse arrival time. For example, one half of a period of jitter at 100 kHz occurs in 5 μs , which is 7.7 T1 bit periods. If the jitter amplitude is 0.4 UI, then a one preceded by seven zeros can have maximum displacement in arrival time, i.e. either 0.4 UI too early or 0.4 UI too late. For the CS6158A and CS6158, the data recovery circuit correctly assigns a received bit to its proper clock period if it is displaced by less than 6/13 of a bit period from its optimal location. Theoretically, this would give a jitter tolerance of 0.46 UI. The actual jitter tolerance of the CS6158A and CS6158 is only slightly less than the ideal.

In the event of a maximum jitter hit, the RCLK clock period immediately adjusts to align itself with the incoming data and prepare to accurately place the next one, whether it arrives one period

later, or after another string of zeros and is displaced by jitter. For a maximum early jitter hit, RCLK will have a period of $7/13 * 648 \text{ ns} = 349 \text{ ns}$ (2,865,961 Hz). For a maximum late jitter hit, RCLK will have a period of $19/13 * 648 \text{ ns} = 947 \text{ ns}$ (1,055,880 Hz).

Loss of Signal

Receiver loss of signal is indicated upon receiving 175 consecutive zeros. A digital counter counts received zeros based on RCLK cycles. A zero input is determined either when zeros are received, or when the received signal amplitude drops below a 0.3 V peak threshold.

The receiver reports loss of signal by setting the Loss of Signal pin, LOS, high. In a loss of signal state, the RCLK frequency will be equal to the ACLKI frequency since ACLKI is being used to calibrate the clock recovery circuit. Received data is output on RPOS/RNEG regardless of LOS status. In the CS6158, LOS returns to a logic zero upon receipt of the first bit at the RTIP/RRING inputs. In the CS6158A, LOS returns to logic zero after the ones density reaches 12.5% (based upon 175 bit periods starting with a one and containing less than 100 consecutive zeros) as prescribed in ANSI T1.231-1993.

Also in the CS6158A, a power-up or manual reset will set LOS high.

Local Loopback

The local loopback mode takes clock and data presented on TCLK, TPOS, and TNEG, and outputs it at RCLK, RPOS and RNEG. Receiver inputs are ignored when local loopback is in effect. Local loopback is selected by taking LLOOP, pin 27, high.

Remote Loopback

In remote loopback, the recovered clock and data input on RTIP and RRING are sent back out on the line via TTIP and TRING. The recovered incoming signals are also sent to RCLK, RPOS and RNEG. A remote loopback occurs in response to RLOOP going high. Simultaneous selection of local and remote loopback modes is not valid (see Reset).

In remote loopback, the recovered clock is used to calibrate the transmitter delay line. Because RCLK cycle times vary, selecting RLOOP will result in adding jitter to the transmitted data. *Therefore selection of the RLOOP function on a functioning link is not recommended.* Rather, it is recommended that remote loopbacks be implemented external to the CS6158A and CS6158, for example, by using a frame buffer in the data path between the CS6158A and CS6158 receiver and transmitter.

Driver Performance Monitor

To aid in early detection and easy isolation of nonfunctioning links, the CS6158A and CS6158 are able to monitor transmit drive performance and report when the driver is no longer operational. This feature can be used to monitor either the device's performance or the performance of a neighboring driver. The driver performance monitor indicator is normally at a low (zero) logic level, and goes to high level upon detecting driver failure.

The driver performance monitor consists of an activity detector that monitors the transmitted signal when MTIP is connected to TTIP and MRING is connected to TRING. DPM will go high if the absolute difference between MTIP and MRING does not transition above or below a threshold level within a time-out period.

Whenever more than one line interface IC resides on the same circuit board, the effectiveness of the driver performance monitor can be maximized by having each IC monitor performance of a neighboring IC, rather than having it monitor its own performance. Note that a CS6158A can not be used to monitor a CS6158 due to output stage differences.

For the CS6158 only, DPM should be averaged externally in hardware or software for approximately 500 ms to filter short assertions caused by very low ones density before action is taken to respond to the driver failure.

Power On Reset / Reset

Upon power-up, the CS6158A and CS6158 are held in a static state until the supply crosses a threshold of approximately three volts. When this threshold is crossed, the device will delay for about 10 ms to allow the power supply to reach operating voltage. After this delay, calibration of the delay lines used in the transmit and receive sections commences. The delay lines can be calibrated only if a reference clock is present. The reference clock for the receiver is provided by ACLKI. The reference clock for the transmitter is provided by TCLK. The initial calibration should take less than 20 ms.

In operation, the delay lines are continuously calibrated, making the performance of the device independent of power supply or temperature variations. The continuous calibration function foregoes any requirement to reset the line interface when in operation. However, a reset function is available which will clear the internal logic.

A reset request is made by simultaneously setting both RLOOP and LLOOP high for at least 200 ns. Reset will initiate on the falling edge of the reset request (falling edge of RLOOP or LLOOP).

A reset will set LOS high on the CS6158A.

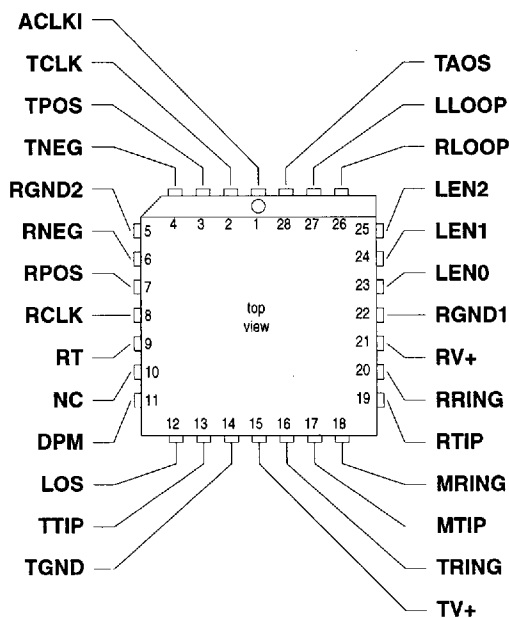
Power Supply

The device operates from a single +5 Volt supply. Separate pins for transmit and receive supplies provide internal isolation. These pins should be connected externally near the device and decoupled to their respective grounds. TV+ must not exceed RV+ by more than 0.3V.

Decoupling and filtering of the power supplies is crucial for the proper operation of the analog circuits in both the transmit and receive paths. A 1.0 μ F capacitor should be connected between TV+ and TGND, and a 0.1 μ F capacitor should be connected between RV+ and RGND. Use mylar or ceramic capacitors and place them as closely as possible to their respective power supply pins. A 68 μ F tantalum capacitor should be added close to the RV+/RGND supply. Wire-wrap breadboarding of the line interface is not recommended because lead resistance and inductance serve to defeat the function of the decoupling capacitors.

PIN DESCRIPTIONS

ACLKI	1	28	TAOS
TCLK	2	27	LLOOP
TPOS	3	26	RLOOP
TNEG	4	25	LEN2
RGND2	5	24	LEN1
RNEG	6	23	LEN0
RPOS	7	22	RGND
RCLK	8	21	RV+
RT	9	20	RRING
NC	10	19	RTIP
DPM	11	18	MRING
LOS	12	17	MTIP
TTIP	13	16	TRING
TGND	14	15	TV+



Power Supplies

TV+ - Positive Power Supply, Transmit Drivers, Pin 15.

Positive power supply for the transmit drivers; typically +5 Volts. TV+ must not exceed RV+ by more than 0.3V.

TGND - Ground, Transmit Drivers, Pin 14.

Power supply ground for the transmit drivers; typically 0 Volts.

RV+ - Positive Power Supply, Pin 21.

Positive power supply for the device, except transmit drivers; typically +5 Volts.

RGND1, RGND2 - Ground, Pins 22 and 5

Power supply grounds for the device, except transmit drivers; typically 0 Volts.

Control**LLOOP - Local Loopback, Pin 27.**

Setting LLOOP to a logic 1 routes the transmit clock and data to the receive clock and data pins. TCLK and TPOS/TNEG are still transmitted. Inputs on RTIP and RRING are ignored.

RLOOP - Remote Loopback, Pin 26.

Setting RLOOP to a logic 1 causes the recovered clock and data to be sent through the driver back to the line. The recovered signal is also sent to RCLK and RPOS/RNEG.

Simultaneously taking RLOOP and LLOOP high for at least 200 ns initiates a device reset.

LEN0, LEN1, LEN2 - Line Length Selection, Pins 23, 24 and 25.

Determines the shape and amplitude of the transmitted pulse to accommodate several cable types and lengths. See Table 1 for information on line length selection.

TAOS - Transmit All Ones select, Pin 28.

Setting TAOS to logic 1 causes continuous ones to be transmitted at the frequency selected by TCLK.

Inputs**ACLKI - Alternate External Clock Input, Pin 1.**

Either a 1.544 MHz (or 2.048 MHz for E1) clock must be input to ACLKI, which is used to calibrate the receiver delay line. Since ACLKI is used to calibrate the receiver, RCLK will equal ACLKI upon loss of signal.

TCLK, TPOS, TNEG - Transmit Clock, Transmit Positive Data, Transmit Negative Data - Pins 2, 3 and 4.

Inputs for clock and data to be transmitted. The signal is driven on to the line through TTIP and TRING. TPOS and TNEG are sampled on the falling edge of TCLK. A TPOS input causes a positive pulse to be transmitted, while a TNEG input causes a negative pulse to be transmitted.

RTIP, RRING - Receive Tip, Receive Ring, Pins 19 and 20.

The AMI receive signal is input to these pins. A center-tapped, center-grounded, 2:1, step-up transformer is required on these inputs, as shown in Figure A1 in the *Applications* section. Data and clock are recovered and output on RPOS/RNEG and RCLK.

RT - Resistor Termination, Pin 9.

This pin should be connected to the RV+ power supply through a 1k Ω resistor.

MTIP, MRING - Monitored Tip, Monitored Ring, Pins 17 and 18.

These pins are normally connected to TTIP and TRING and monitor the transmitter output. If the monitor is not used, tying MTIP low and MRING high through a resistor will reduce power consumption slightly.

Status**LOS - Loss of Signal, Pin 12.**

LOS goes to a logic 1 when 175 consecutive zeros have been detected. In the CS6158, LOS returns to logic 0 on the first bit received. When in the loss of signal state, received ones are output at RPOS/RNEG. In the CS6158A, LOS returns to a logic 0 after the ones density reaches 12.5% (based upon 175 bit periods starting with a one and containing less than 100 consecutive zeros) as prescribed in ANSI T1.231-1993.

DPM - Driver Performance Monitor, Pin 11.

If no signal is present on MTIP and MRING, DPM goes to a logic 1.

Outputs**RCLK, RPOS, RNEG - Recovered Clock, Receive Positive Data, Receive Negative Data - Pins 8, 7 and 6.**

The receiver recovered clock and NRZ digital data is output on these pins. RPOS and RNEG are stable and valid on the rising edge of RCLK. A positive pulse (with respect to ground) received on the RTIP pin generates a logic 1 on RPOS, and a positive pulse received on the RRING pin generates a logic 1 on RNEG.

TTIP, TRING - Transmit Tip, Transmit Ring, Pins 13 and 16.

The AMI signal is driven to the line through these pins.

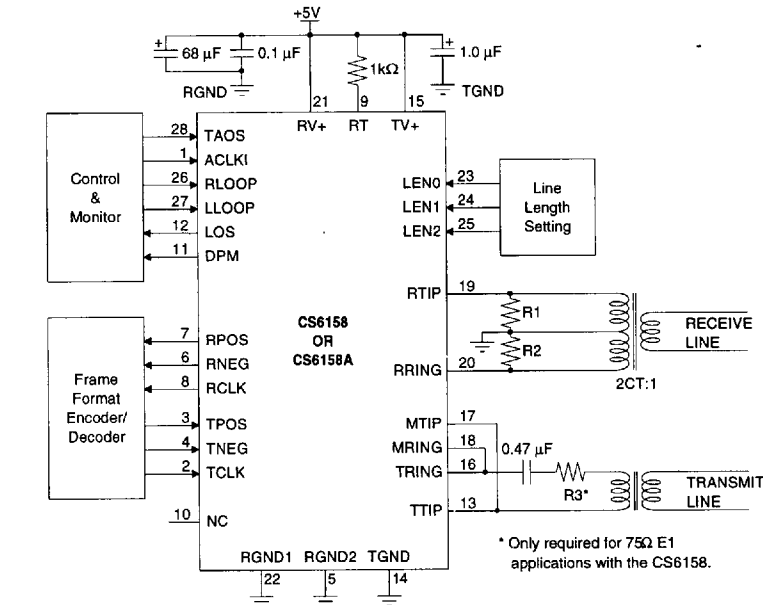
For the CS6158A, this output is designed to drive a 75 Ω ohm load. A transformer is required as shown in Figure A1.

For the CS6158, this output is designed to drive a 25 Ω load. A 2:1 step-up transformer is required as shown in Figure A1. When driving 75 Ω coax cable, 4.4 Ohms of resistance should be added in series with the transformer primary. The transmitter will drive twisted-shielded pair cable, terminated with 120 Ω , without additional components.

Miscellaneous**NC - No Connect, Pin 10**

Pin 10 may be left floating (recommended for new designs), or may be tied to ground.

APPLICATIONS



DEVICE	FREQUENCY MHz	CABLE Ω	R1&2 Ω	R3 Ω	Transmit Transformer
CS6158	1.544	100	200	0	1:2
	2.048	120	240	0	1:2
	2.048	75	150	4.4	1:2
CS6158A	1.544	100	200	0	1:1.15
	2.048	120	240	0	1:1.26
	2.048	75	150	0	1:1

Figure A1. - Typical Connection Diagram

Line Interface

Figure A1 shows the typical configuration for the CS6158A and CS6158. Note that CS6158A transmitter transformer requirements have changed from those of the CS6158. This new transformer allows the CS6158A's lower power driver to be implemented.

For T1 applications, the receiver transformer is center-tapped and center-grounded with 200 Ω re-

sistors between the center tap and each leg on the IC side. These resistors provide the 100 Ω termination for the T1 line. When terminating 2.048 MHz twisted-shielded pair cable, 240 Ω resistors will provide the required 120 Ω load. For transmitting data at 2.048 MHz onto a 75 Ω coax cable, the terminating resistors should be 150 Ω to provide the necessary 75 Ω termination to the line.

Figure A1 shows a 0.47 μF capacitor in series

with the transmit transformer primary. This capacitor is needed to prevent any output stage imbalance from resulting in a DC current through the transformer primary. This current might saturate the transformer producing an output offset level shift.

Transformers

Recommended transmitter and receiver transformer specifications for the CS6158 and CS6158A are shown in Table A1. The transformers in Table A2 have been tested and recommended for use with the CS6158. The transformers in Table A3 have been tested and recommended for use with the CS6158A. Refer to the "Telecom Transformer Selection Guide" for detailed schematics which show how to connect the line interface IC with a particular transformer.

In applications with the CS6158A where it is advantageous to use a single transmitter transformer for both 75Ω and 120Ω E1 applications, a 1:1.26 transformer may be used. Although transmitter return loss will be reduced for 75Ω applications, the pulse amplitude will be correct.

Interfacing the CS6158A with CS2180B T1 Transceiver

To interface with the CS2180B, connect the devices as shown in Figure A2.

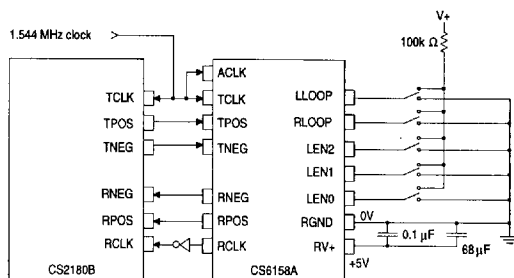


Figure A2. - Interfacing the CS6158A with a CS2180B

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Parameter	CS6158 Receiver & Transmitter CS6158A Receiver	CS6158A Transmitter
Turns Ratio	1:2 CT $\pm 5\%$	1:1 $\pm 1.5\%$ for 120 Ω E1 1:1.15 $\pm 5\%$ for 100 Ω T1 1:1.26 $\pm 1.5\%$ for 75 Ω E1
Primary Inductance	600 μ H min. @ 772 kHz	1.5 mH min. @ 772 kHz
Primary Leakage Inductance	1.3 μ H max. @ 772 kHz	0.3 μ H max. @ 772 kHz
Secondary Leakage Inductance	0.4 μ H max. @ 772 kHz	0.4 μ H max. @ 772 kHz
Interwinding Capacitance	23 pF max.	18 pF max.
ET-constant	16 V- μ s min. for T1 12 V- μ s min. for E1	16 V- μ s min. for T1 12 V- μ s min. for E1

Table A1. Transformer Specifications

Turns Ratio(s)	Manufacturer	Part Number	Package Type
1:2CT	Pulse Engineering	PE-65351	1.5 kV through-hole, single
	Schott	67129300	
	Bel Fuse	0553-0013-HC	
dual 1:2CT	Pulse Engineering	PE-64951	1.5 kV through-hole, dual
	Bel Fuse	0553-0013-1J	
dual 1:2CT	Pulse Engineering	PE-65761	1.5 kV surface-mount, dual
	Bel Fuse	S553-0013-03	
1:2CT	Pulse Engineering	PE-65835	3 kV through-hole, single EN60950, EN41003 approved

Table A2. Recommended Transformers For The CS6158

Application	Turns Ratio(s)	Manufacturer	Part Number	Package Type
RX: T1 & E1	1:2CT	Pulse Engineering	PE-65351	1.5 kV through-hole, single
		Schott	67129300	
		Bel Fuse	0553-0013-HC	
TX: T1	1:1.15	Pulse Engineering	PE-65388	1.5 kV through-hole, single
		Schott	67129310	
		Bel Fuse	0553-0013-RC	
TX: E1 (75 & 120 Ω)	1:1.26 1:1	Pulse Engineering	PE-65389	1.5 kV through-hole, single
		Schott	67129320	
		Bel Fuse	0553-0013-SC	
RX & TX: T1	1:2CT 1:1.15	Pulse Engineering	PE-65565	1.5 kV through-hole, dual
		Bel Fuse	0553-0013-7J	
RX & TX: E1 (75 & 120 Ω)	1:2CT 1:1.26 1:1	Pulse Engineering	PE-65566	1.5 kV through-hole, dual
		Bel Fuse	0553-0013-8J	
RX & TX: T1	1:2CT 1:1.15	Pulse Engineering	PE-65765	1.5 kV surface-mount, dual
		Bel Fuse	S553-0013-06	
RX & TX: E1 (75 & 120 Ω)	1:2CT 1:1.26 1:1	Pulse Engineering	PE-65766	1.5 kV surface-mount, dual
		Bel Fuse	S553-0013-07	
RX : T1 & E1	1:2CT	Pulse Engineering	PE-65835	3 kV through-hole, single EN60950, EN41003 approved
TX: E1 (75 & 120 Ω)	1:1.26 1:1	Pulse Engineering	PE-65839	3 kV through-hole, single EN60950, EN41003 approved

Table A3. Recommended Transformers For The CS6158A