CIRRUS LOGIC®

CS4265

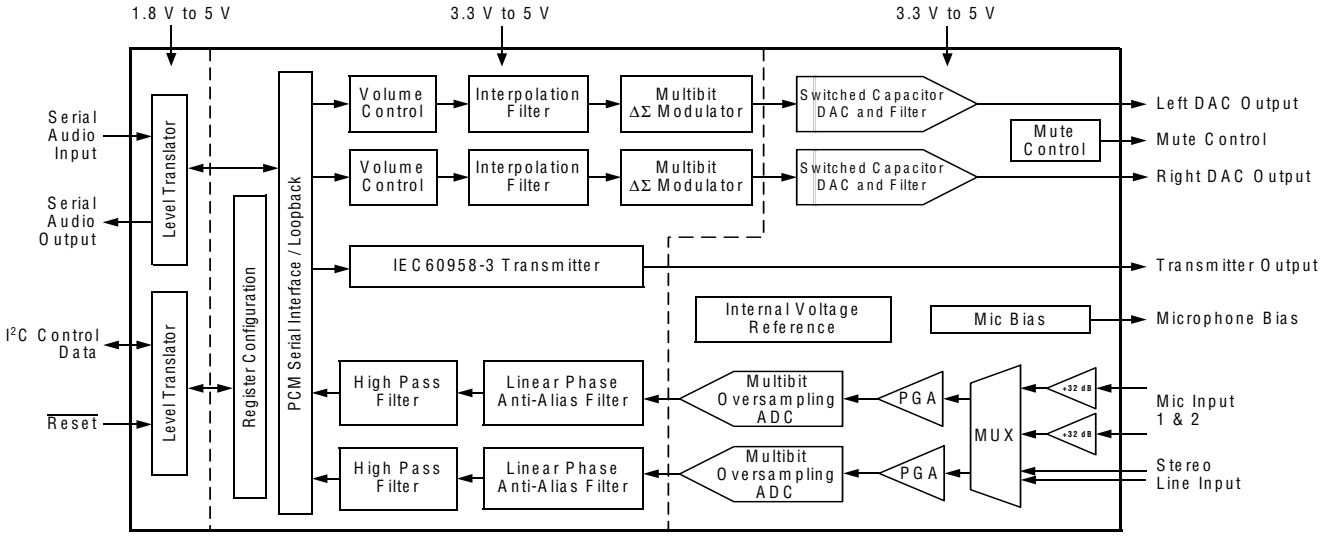
105 dB, 24-Bit, 192 kHz Stereo Audio CODEC

D/A Features

- Multi-bit Delta Sigma modulator
- 105 dB Dynamic Range
- -95 dB THD+N
- Up to 192 kHz Sampling Rates
- Single-ended Analog Architecture
- Volume Control with Soft Ramp
  - 0.5 dB Step Size
  - Zero Crossing Click-free Transitions
- Popguard™ Technology
  - Minimizes the effects of output transients.
- Filtered Line-level Outputs
- Selectable Serial Audio Interface Formats
  - Left Justified up to 24-bit
  - I²S up to 24-bit
  - Right Justified 16, 18, 20 and 24-bit
- Selectable 50/15 µs De-emphasis

A/D Features

- Multi-bit Delta Sigma Modulator
- 105 dB Dynamic Range
- -95 dB THD+N
- Stereo 2:1 Input Multiplexer
- Programmable Gain Amplifier (PGA)
  - +/- 12 dB gain, 0.5 dB Step Size
  - Zero Crossing, Click-free Transitions
- Pseudo-differential Stereo Line Inputs
- Stereo Microphone Inputs
  - +32 dB Gain Stage
  - Low-noise Bias Supply
- Up to 192 kHz Sampling Rates
- Selectable Serial Audio Interface Formats
  - Left Justified up to 24-bit
  - I²S up to 24-bit
- High-pass Filter or DC Offset Calibration



Advance Product Information

This document contains information for a new product.
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System Features

- Synchronous IEC60958-3 Transmitter
  - Up to 192 kHz Sampling Rates
  - 75 Ω Drive Capability
- Serial Audio Data Input Multiplexer
- Internal Digital Loopback
- Supports Master or Slave Operation
- Mute Output Control
- Power Down Mode
  - Available for A/D, D/A, CODEC, Mic Preamplifier
- +3.3 V to +5 V Analog Power Supply
- +3.3 V to +5 V digital Power Supply
- Direct Interface with 1.8 V to 5 V Logic Levels
- Supports I²C Control Port Interface

General Description

The CS4265 is a highly integrated stereo audio CODEC. The CS4265 performs stereo analog-to-digital (A/D) and digital-to-analog (D/A) conversion of up to 24-bit serial values at sample rates up to 192 kHz.

A 2:1 stereo input multiplexer is included for selecting between line level or microphone level inputs. The microphone input path includes a +32 dB gain stage and a low noise bias voltage supply. The PGA is available for line or microphone inputs and provides gain or attenuation of ±12 dB in 0.5 dB steps.

The output of the PGA is followed by an advanced 5th-order, multi-bit delta sigma modulator and digital filtering/decimation. Sampled data is transmitted by the serial audio interface at rates from 4 kHz to 192 kHz in either slave or master mode.

The D/A converter is based on a 4th-order multi-bit delta sigma modulator with an ultra-linear low pass filter and offers a volume control that operates with a 0.5 dB step size. It incorporates selectable soft ramp and zero crossing transition functions to eliminate clicks and pops.

Standard 50/15 µs de-emphasis is available for a 44.1 kHz sample rate for compatibility with digital audio programs mastered using the 50/15 µs pre-emphasis technique.

Integrated level translators allow easy interfacing between the CS4265 and other devices operating over a wide range of logic levels.

ORDERING INFORMATION

CS4265-CNZ, Lead Free	-10° to 70° C	32-pin QFN
CDB4265		Evaluation Board

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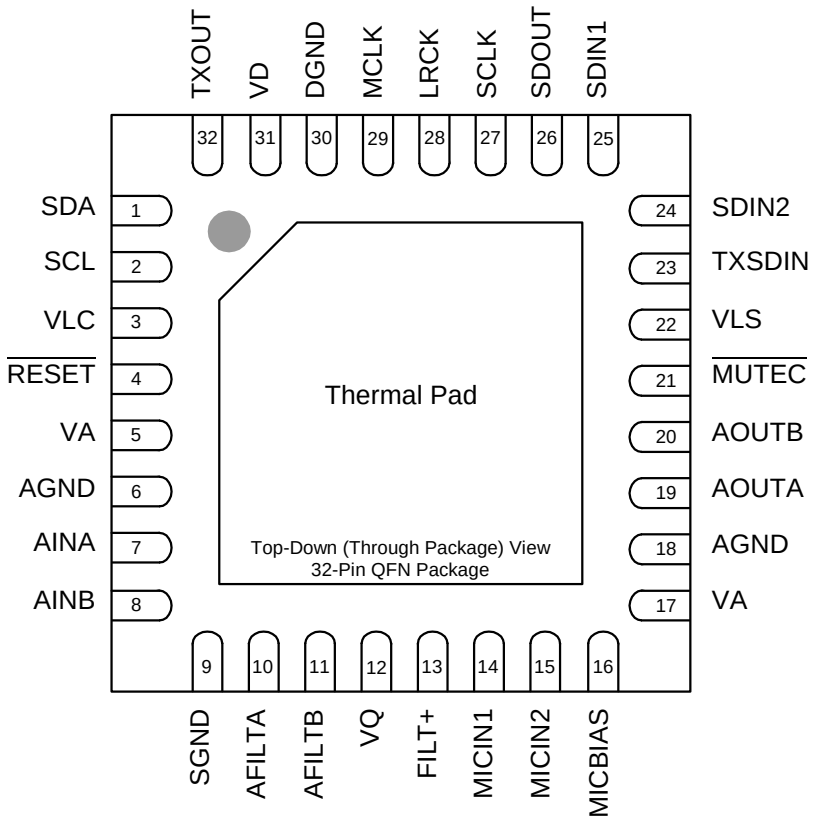
1. PIN DESCRIPTIONS



Pin Name	#	Pin Description
SDA	1	**Serial Control Data** (*Input*/*Output*) - Bidirectional data line for the I²C control port.
SCL	2	**Serial Control Port Clock** (*Input*) - Serial clock for the I²C control port.
VLC	3	**Control Port Power** (*Input*) - Determines the required signal level for the control port interface. Refer to the Recommended Operating Conditions for appropriate voltages.
$\overline{\text{RESET}}$	4	**Reset** (*Input*) - The device enters a low power mode when this pin is driven low.
VA	5	**Analog Power** *(Input)* - Positive power for the internal analog section.
AGND	6	**Analog Ground** (*Input*) - Ground reference for the internal analog section.
AINA **AINB**	7, 8	**Analog Input** (*Input*) - The full scale level is specified in the ADC Analog Characteristics specification table.
SGND	9	**Signal Ground** (*Input*) - Ground reference for the analog line inputs.
AFILTA **AFILTB**	10, 11	**Antialias Filter Connection** (*Output*) - Antialias filter connection for the ADC inputs.
VQ	12	**Quiescent Voltage** (*Output*) - Filter connection for internal quiescent voltage.
FILT+	13	**Positive Voltage Reference** (*Output*) - Positive reference voltage for the internal sampling circuits.
MICIN1 **MICIN2**	14, 15	**Microphone Input** (*Input*) - The full scale level is specified in the ADC Analog Characteristics specification table.

MICBIAS	16	**Microphone Bias** (*Output*) - Low noise bias supply for external microphone. Electrical characteristics are specified in the DC Electrical Characteristics table.
VA	17	**Analog Power** *(Input)* - Positive power for the internal analog section.
AGND	18	**Analog Ground** (*Input*) - Ground reference for the internal analog section.
AOUTA **AOUTB**	19, 20	**Analog Audio Output** (*Output*) - The full scale output level is specified in the DAC Analog Characteristics specification table.
$\overline{\text{MUTEC}}$	21	**Mute Control** (*Output)* - This pin is active during power-up initialization, reset, muting, when master clock left/right clock frequency ratio is incorrect, or power-down.
VLS	22	**Serial Audio Interface Power** (*Input*) - Determines the required signal level for the serial audio interface. Refer to the Recommended Operating Conditions for appropriate voltages.
TXSDIN	23	**Transmitter Serial Audio Data Input** (*Input)* - Input for two's complement serial audio data.
SDIN2	24	**Serial Audio Data Input 2** (*Input*) - Input for two's complement serial audio data.
SDIN1	25	**Serial Audio Data Input 1** (*Input*) - Input for two's complement serial audio data.
SDOUT	26	**Serial Audio Data Output** (*Output*) - Output for two's complement serial audio data.
SCLK	27	**Serial Clock** *(Input/Output*) - Serial clock for the serial audio interface.
LRCK	28	**Left Right Clock** *(Input/Output*) - Determines which channel, Left or Right, is currently active on the serial audio data line.
MCLK	29	**Master Clock** (*Input*) -Clock source for the delta-sigma modulators.
DGND	30	**Digital Ground** (*Input*) - Ground reference for the internal digital section.
VD	31	**Digital Power** (*Input*) - Positive power for the internal digital section.
TXOUT	32	**Transmitter Line Driver Output** (*Output)* - IEC60958-3 driver output.
Thermal Pad	-	**Thermal Pad** - Thermal relief pad for optimized heat dissipation.

2. CHARACTERISTICS AND SPECIFICATIONS

(All Min/Max characteristics and specifications are guaranteed over the Specified Operating Conditions. Typical performance characteristics and specifications are derived from measurements taken at nominal supply voltages and T_A = 25°C.)

SPECIFIED OPERATING CONDITIONS (AGND = DGND = 0 V; All voltages with respect to ground.)

Parameters		Symbol	Min	Nom	Max	Units
DC Power Supplies:	Analog	VA	3.1	5.0	5.25	V
	Digital	VD	3.1	3.3	5.25	V
	Logic - Serial Port	VLS	1.71	3.3	5.25	V
	Logic - Control Port	VLC	1.71	3.3	5.25	V
Ambient Operating Temperature (Power Applied)		T_A	-10	-	+70	°C

ABSOLUTE MAXIMUM RATINGS (AGND = DGND = 0 V All voltages with respect to ground.) (Note 1)

Parameter		Symbol	Min	Typ	Max	Units
DC Power Supplies:	Analog	VA	-0.3	-	+6.0	V
	Digital	VD	-0.3	-	+6.0	V
	Logic - Serial Port	VLS	-0.3	-	+6.0	V
	Logic - Control Port	VLC	-0.3	-	+6.0	V
Input Current	(Note 2)	I_{in}	-	-	±10	mA
Analog Input Voltage		V_{INA}	AGND-0.3	-	VA+0.3	V
Digital Input Voltage	Logic - Serial Port	V_{IND-S}	-0.3	-	VLS+0.3	V
	Logic - Control Port	V_{IND-C}	-0.3	-	VLC+0.3	V
Ambient Operating Temperature (Power Applied)		T_A	-20	-	+85	°C
Storage Temperature		T_{stg}	-65	-	+150	°C

Notes: 1. Operation beyond these limits may result in permanent damage to the device. Normal operation is not guaranteed at these extremes.

2. Any pin except supplies. Transient currents of up to ±100 mA on the analog input pins will not cause SCR latch-up.

DAC ANALOG CHARACTERISTICS (Full-Scale Output Sine Wave, 997 Hz; Test load R_L = 3 kΩ, C_L = 10 pF (see Figure 1), Fs = 48/96/192 kHz. Measurement Bandwidth 10 Hz to 20 kHz, unless otherwise specified.)

Parameter		Symbol	All Speed Modes Min	Typ	Max	Unit
Dynamic Performance for VA = 5 V						
Dynamic Range	(Note 3)					
18 to 24-Bit	unweighted		96	102	-	dB
	A-Weighted		99	105	-	dB
16-Bit	unweighted		87	93	-	dB
	A-Weighted		90	96	-	dB
Total Harmonic Distortion + Noise	(Note 3)	THD+N				
18 to 24-Bit	0 dB		-	-95	-89	dB
	-20 dB		-	-82	-76	dB
	-60 dB		-	-42	-36	dB
16-Bit	0 dB		-	-93	-87	dB
	-20 dB		-	-73	-67	dB
	-60 dB		-	-33	-27	dB
Dynamic Performance for VA = 3.3 V						
Dynamic Range	(Note 3)					
18 to 24-Bit	unweighted		93	99	-	dB
	A-Weighted		96	102	-	dB
16-Bit	unweighted		85	90	-	dB
	A-Weighted		88	93	-	dB
Total Harmonic Distortion + Noise	(Note 3)	THD+N				
18 to 24-Bit	0 dB		-	-92	-84	dB
	-20 dB		-	-79	-71	dB
	-60 dB		-	-39	-31	dB
16-Bit	0 dB		-	-90	-82	dB
	-20 dB		-	-70	-62	dB
	-60 dB		-	-30	-22	dB
Interchannel Isolation	(1 kHz)		-	100	-	dB
DC Accuracy						
Interchannel Gain Mismatch			-	0.1	0.25	dB
Gain Drift			-	100	-	ppm/°C
Analog Output						
Full Scale Output Voltage			0.60*VA	0.65*VA	0.70*VA	V_{pp}
DC Current draw from an AOUT pin	(Note 4)	I_{OUT}	-	-	10	µA
AC-Load Resistance	(Note 5)	R_L	3	-	-	kΩ
Load Capacitance	(Note 5)	C_L	-	-	100	pF
Output Impedance		Z_{OUT}	-	100	-	Ω

Note: 3. One-half LSB of triangular PDF dither added to data.

4. Guaranteed by design. The DC current draw represents the allowed current draw from the AOUT pin due to typical leakage through the electrolytic DC blocking capacitors.

5. Guaranteed by design. See Figure 2. R_L and C_L reflect the recommended minimum resistance and maximum capacitance required for the internal op-amp's stability. C_L affects the dominant pole of the internal output amp; increasing C_L beyond 100 pF can cause the internal op-amp to become unstable.

DAC COMBINED INTERPOLATION & ON-CHIP ANALOG FILTER RESPONSE

Parameter (Note 6,9)		Symbol	Min	Typ	Max	Unit
Combined Digital and On-chip Analog Filter Response			***Single Speed Mode***			
Passband (Note 6)	to -0.05 dB corner		0	-	.4780	Fs
	to -3 dB corner		0	-	.4996	Fs
Frequency Response 10 Hz to 20 kHz			-.01	-	+.08	dB
StopBand			.5465	-	-	Fs
StopBand Attenuation	(Note 7)		50	-	-	dB
Group Delay		tgd	-	10/Fs	-	s
De-emphasis Error (Note 8)	Fs = 44.1 kHz		-	-	+.05/-.25	dB
Combined Digital and On-chip Analog Filter Response			***Double Speed Mode***			
Passband (Note 6)	to -0.1 dB corner		0	-	.4650	Fs
	to -3 dB corner		0	-	.4982	Fs
Frequency Response 10 Hz to 20 kHz			-.05	-	+.2	dB
StopBand			.5770	-	-	Fs
StopBand Attenuation	(Note 7)		55	-	-	dB
Group Delay		tgd	-	5/Fs	-	s
Combined Digital and On-chip Analog Filter Response			***Quad Speed Mode***			
Passband (Note 6)	to -0.1 dB corner		0	-	0.397	Fs
	to -3 dB corner		0	-	0.476	Fs
Frequency Response 10 Hz to 20 kHz			0	-	+0.00004	dB
StopBand			0.7	-	-	Fs
StopBand Attenuation	(Note 7)		51	-	-	dB
Group Delay		tgd	-	2.5/Fs	-	s

Notes: 6. Filter response is guaranteed by design.

7. For Single Speed Mode, the Measurement Bandwidth is 0.5465 Fs to 3 Fs.
For Double Speed Mode, the Measurement Bandwidth is 0.577 Fs to 1.4 Fs.
For Quad Speed Mode, the Measurement Bandwidth is 0.7 Fs to 1 Fs.

8. De-emphasis is available only in Single Speed Mode.

9. Response is clock dependent and will scale with Fs. Note that the amplitude vs. frequency plots of this data (Figures 18 to 27) have been normalized to Fs and can be de-normalized by multiplying the X-axis scale by Fs.

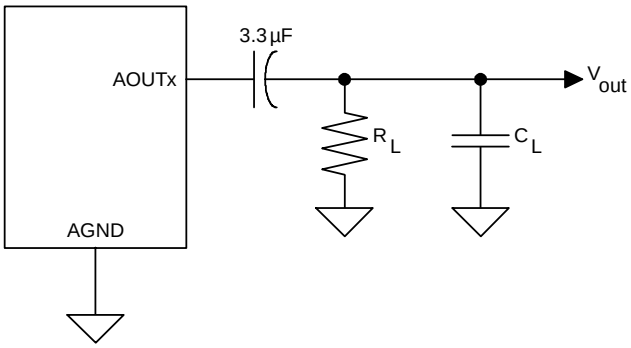


Figure 1. DAC Output Test Load

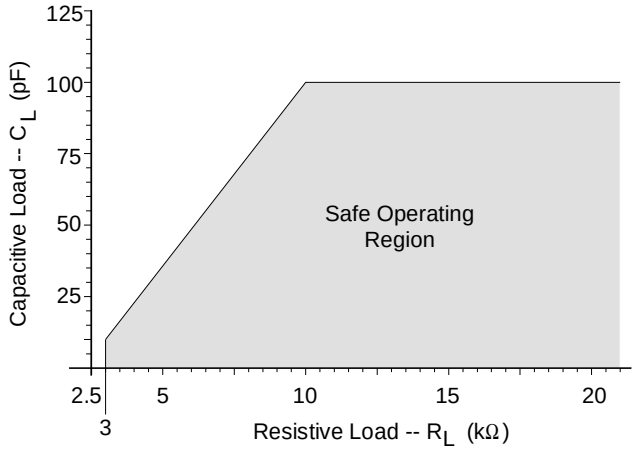


Figure 2. Maximum DAC Loading

ADC ANALOG CHARACTERISTICS

Test conditions (unless otherwise specified): Input test signal is a 1 kHz sine wave; measurement bandwidth is 10 Hz to 20 kHz. Fs = 48/96/192 kHz.

Line Level Inputs

Parameter	Symbol	Min	Typ	Max	Unit
Dynamic Performance for VA = 5 V					
Dynamic Range					
PGA Setting: -12 dB to +6 dB					
A-weighted		99	105	-	dB
unweighted		96	102	-	dB
(Note 12) 40 kHz bandwidth unweighted		-	99	-	dB
PGA Setting: +12 dB Gain					
A-weighted		93	99	-	dB
unweighted		90	96	-	dB
(Note 12) 40 kHz bandwidth unweighted		-	93	-	dB
Total Harmonic Distortion + Noise (Note 11)	THD+N				
PGA Setting: -12 dB to +6 dB					
-1 dB		-	-95	-89	dB
-20 dB		-	-82	-	dB
-60 dB		-	-42	-	dB
(Note 12) 40 kHz bandwidth -1 dB		-	-92	-	dB
PGA Setting: +12 dB Gain					
-1 dB		-	-92	-86	dB
-20 dB		-	-76	-	dB
-60 dB		-	-36	-	dB
(Note 12) 40 kHz bandwidth -1 dB		-	-89	-	dB
Dynamic Performance for VA = 3.3 V					
Dynamic Range					
PGA Setting: -12 dB to +6 dB					
A-weighted		94	102	-	dB
unweighted		91	99	-	dB
(Note 12) 40 kHz bandwidth unweighted		-	96	-	dB
PGA Setting: +12 dB Gain					
A-weighted		90	96	-	dB
unweighted		87	93	-	dB
(Note 12) 40 kHz bandwidth unweighted		-	90	-	dB

Total Harmonic Distortion + Noise (Note 11)		THD+N				
PGA Setting: -12 dB to +6 dB						
-1 dB			-	-92	-86	dB
-20 dB			-	-79	-	dB
-60 dB			-	-39	-	dB
(Note 12)	40 kHz bandwidth	-1 dB	-	-84	-	dB
PGA Setting: +12 dB Gain						
-1 dB			-	-89	-83	dB
-20 dB			-	-73	-	dB
-60 dB			-	-33	-	dB
(Note 12)	40 kHz bandwidth	-1 dB	-	-81	-	dB

Line Level Inputs

Parameter	Symbol	Min	Typ	Max	Unit
Interchannel Isolation		-	90	-	dB
Line Level Input Characteristics					
Full-scale Input Voltage		0.53*VA	0.56*VA	0.59*VA	V_{pp}
Input Impedance (Note 10)		6.12	6.8	7.48	kΩ
Maximum Interchannel Input Impedance Mismatch		-	5	-	%

Line Level and Microphone Level Inputs

Parameter	Symbol	Min	Typ	Max	Unit
DC Accuracy					
Interchannel Gain Mismatch		-	0.1	-	dB
Gain Error			-	±5	%
Gain Drift		-	±100	-	ppm/°C
Programmable Gain Characteristics					
Gain Step Size		-	0.5	-	dB
Absolute Gain Step Error		-	-	0.4	dB

10. Valid when the line level inputs are selected.

ADC ANALOG CHARACTERISTICS (cont)

Microphone Level Inputs

Parameter	Symbol	Min	Typ	Max	Unit
Dynamic Performance for VA = 5 V					
Dynamic Range					
PGA Setting: -12 dB to 0 dB					
A-weighted		77	83	-	dB
unweighted		74	80	-	dB
PGA Setting: +12 dB					
A-weighted		65	71	-	dB
unweighted		62	68	-	dB
Total Harmonic Distortion + Noise (Note 11)	THD+N				
PGA Setting: -12 dB to 0 dB					
-1 dB		-	-80	-74	dB
-20 dB		-	-60	-	dB
-60 dB		-	-20	-	dB
PGA Setting: +12 dB					
-1 dB		-	-68	-	dB
Dynamic Performance for VA = 3.3 V					
Dynamic Range					
PGA Setting: -12 dB to 0 dB					
A-weighted		77	83	-	dB
unweighted		74	80	-	dB
PGA Setting: +12 dB					
A-weighted		65	71	-	dB
unweighted		62	68	-	dB
Total Harmonic Distortion + Noise (Note 11)	THD+N				
PGA Setting: -12 dB to 0 dB					
-1 dB		-	-80	-74	dB
-20 dB		-	-60	-	dB
-60 dB		-	-20	-	dB
PGA Setting: +12 dB					
-1 dB		-	-68	-	dB
Interchannel Isolation		-	30	-	dB
Microphone Level Input Characteristics					
Full-scale Input Voltage		0.013*VA	0.014*VA	0.015*VA	V_{pp}
Input Impedance (Note 13)		-	50	-	kΩ

11. Referred to the typical line level full-scale input voltage
12. Valid for Double and Quad Speed Modes only.
13. Valid when the microphone level inputs are selected.

ADC DIGITAL FILTER CHARACTERISTICS

Parameter (Note 14, 16)	Symbol	Min	Typ	Max	Unit
Single Speed Mode					
Passband (-0.1 dB)		0	-	0.4896	Fs
Passband Ripple		-	-	0.035	dB
Stopband		0.5688	-	-	Fs
Stopband Attenuation		70	-	-	dB
Total Group Delay (Fs = Output Sample Rate)	t_{gd}	-	12/Fs	-	s
Double Speed Mode					
Passband (-0.1 dB)		0	-	0.4896	Fs
Passband Ripple		-	-	0.025	dB
Stopband		0.5604	-	-	Fs
Stopband Attenuation		69	-	-	dB
Total Group Delay (Fs = Output Sample Rate)	t_{gd}	-	9/Fs	-	s
Quad Speed Mode					
Passband (-0.1 dB)		0	-	0.2604	Fs
Passband Ripple		-	-	0.025	dB
Stopband		0.5000	-	-	Fs
Stopband Attenuation		60	-	-	dB
Total Group Delay (Fs = Output Sample Rate)	t_{gd}	-	5/Fs	-	s
High Pass Filter Characteristics					
Frequency Response -3.0 dB		-	1	-	Hz
-0.13 dB (Note 15)			20	-	Hz
Phase Deviation @ 20 Hz (Note 15)		-	10	-	Deg
Passband Ripple		-	-	0	dB
Filter Settling Time			10^5/Fs		s

Note: 14. Filter response is guaranteed by design.

15. Response shown is for Fs = 48 kHz.

16. Response is clock dependent and will scale with Fs. Note that the response plots (Figures 30 to 41) are normalized to Fs and can be de-normalized by multiplying the X-axis scale by Fs.

DC ELECTRICAL CHARACTERISTICS (AGND = DGND = 0 V, all voltages with respect to ground. MCLK=12.288 MHz; Fs=48 kHz, Master Mode)

Parameter		Symbol	Min	Typ	Max	Unit
Power Supply Current	VA = 5 V	I_A	-	41	50	mA
(Normal Operation)	VA = 3.3 V	I_A	-	37	45	mA
	VD, VLS, VLC = 5 V	I_D	-	39	47	mA
	VD, VLS, VLC = 3.3 V	I_D	-	23	28	mA
Power Supply Current.	VA = 5 V	I_A	-	0.50	-	mA
(Power-Down Mode) (Note 17).	VLS, VLC, VD=5 V	I_D	-	0.54	-	mA
Power Consumption						
(Normal Operation).	VA, VD, VLS, VLC = 5 V	-	-	400	485	mW
	VA, VD, VLS, VLC = 3.3 V	-	-	198	241	mW
(Power-Down Mode).	VA, VD, VLS, VLC = 5 V	-	-	4.2	-	mW
Power Supply Rejection Ratio (1 kHz)	(Note 18)	PSRR	-	60	-	dB
VQ Characteristics						
Quiescent Voltage		VQ	-	0.5 x VA	-	VDC
DC Current from VQ	(Note 19)	I_Q	-	-	1	µA
VQ Output Impedance		Z_Q	-	23	-	kΩ
FILT+ Nominal Voltage		FILT+	-	VA	-	VDC
Microphone Bias Voltage		MICBIAS	-	0.8 x VA	-	VDC
Current from MICBIAS		I_{MB}	-	-	2	mA

Notes: 17. Power Down Mode is defines as $\overline{\text{RESET}}$ = Low with all clock and data lines held static and no analog input.

18. Valid with the recommended capacitor values on FILT+ and VQ as shown in the Typical Connection Diagram.

19. Guaranteed by design. The DC current draw represents the allowed current draw due to typical leakage through the electrolytic de-coupling capacitors.

DIGITAL INTERFACE CHARACTERISTICS

Parameters (Note 20)		Symbol	Min	Typ	Max	Units
High-Level Input Voltage	Serial Port	V_{IH}	0.7xVLS	-	-	V
	Control Port	V_{IH}	0.7xVLC	-	-	V
Low-Level Input Voltage	Serial Port	V_{IL}	-	-	0.2xVLS	V
	Control Port	V_{IL}	-	-	0.2xVLC	V
High-Level Output Voltage at I_o=2 mA	Serial Port	V_{OH}	VLS-1.0	-	-	V
	Control Port	V_{OH}	VLC-1.0	-	-	V
	MUTEC	V_{OH}	VA-1.0	-	-	V
	TXOUT	V_{OH}	VD-1.0	-	-	V
Low-Level Output Voltage at I_o=2 mA	Serial Port	V_{OL}	-	-	0.4	V
	Control Port	V_{OL}	-	-	0.4	V
	MUTEC	V_{OL}	-	-	0.4	V
	TXOUT	V_{OL}	-	-	0.4	V
Input Leakage Current		I_{in}	-	-	±10	µA
Input Capacitance	(Note 21)		-	-	1	pF
Maximum MUTEC Drive Current			-	3	-	mA

Notes: 20. Serial Port signals include: MCLK, SCLK, LRCK, SDIN1, SDIN2, TXSDIN, SDOUT. Control Port signals include: SCL, SDA, $\overline{\text{RESET}}$.

21. Guaranteed by design.

SWITCHING CHARACTERISTICS - SERIAL AUDIO PORT (Logic '0' = DGND = 0 V; Logic '1' = VL, C_L = 20 pF) (Note 22)

Parameter	Symbol	Min	Typ	Max	Unit
Sample Rate Single Speed Mode	Fs	4	-	50	kHz
Double Speed Mode	Fs	50	-	100	kHz
Quad Speed Mode	Fs	100	-	200	kHz
MCLK Specifications					
MCLK Frequency	f_{mclk}	1.024	-	51.200	MHz
MCLK Input Pulse Width High/Low	t_{clkhl}	8	-	-	ns
MCLK Output Duty Cycle		45	50	55	%
Master Mode					
LRCK Duty Cycle		-	50	-	%
SCLK Duty Cycle		-	50	-	%
SCLK falling to LRCK edge	t_{slr}	-10	-	10	ns
SCLK falling to SDOUT valid	t_{sdo}	0	-	32	ns
SDIN valid to SCLK rising setup time	t_{sdis}	16	-	-	ns
SCLK rising to SDIN hold time	t_{sdih}	20	-	-	ns
Slave Mode					
LRCK Duty Cycle		40	50	60	%
SCLK Period					
Single Speed Mode	t_{sclkw}	$\frac{10^9}{(128)Fs}$	-	-	ns
Double Speed Mode	t_{sclkw}	$\frac{10^9}{(64)Fs}$	-	-	ns
Quad Speed Mode	t_{sclkw}	$\frac{10^9}{(64)Fs}$	-	-	ns
SCLK Pulse Width High	t_{sclkh}	30	-	-	ns
SCLK Pulse Width Low	t_{sclkl}	48	-	-	ns
SCLK falling to LRCK edge	t_{slr}	-10	-	10	ns
SCLK falling to SDOUT valid	t_{sdo}	0	-	32	ns
SDIN valid to SCLK rising setup time	t_{sdis}	16	-	-	ns
SCLK rising to SDIN hold time	t_{sdih}	20	-	-	ns

Notes: 22. See figures 3 and 4 on page 18.

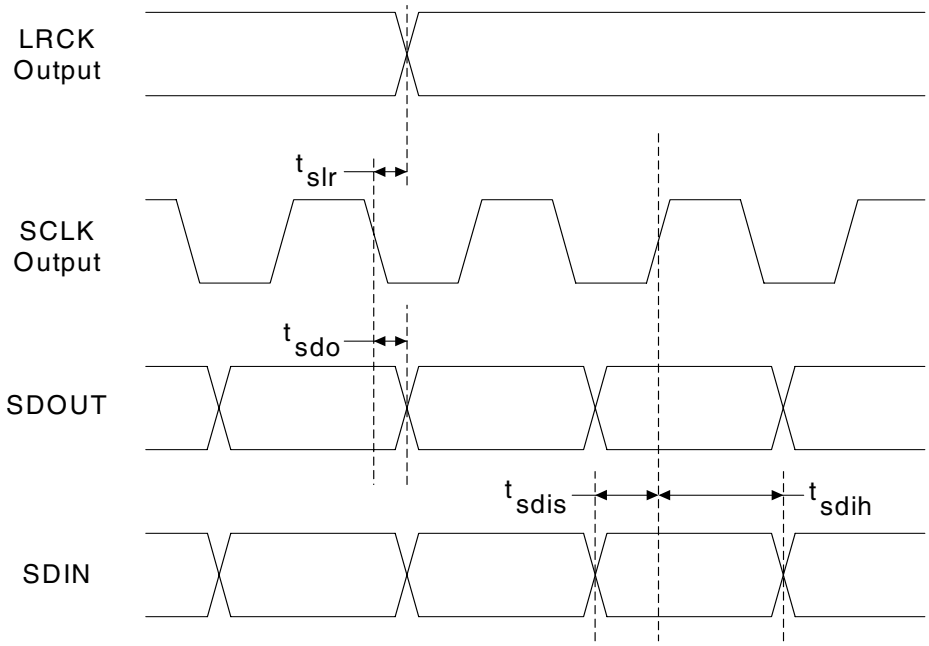


Figure 3. Master Mode Serial Audio Port Timing

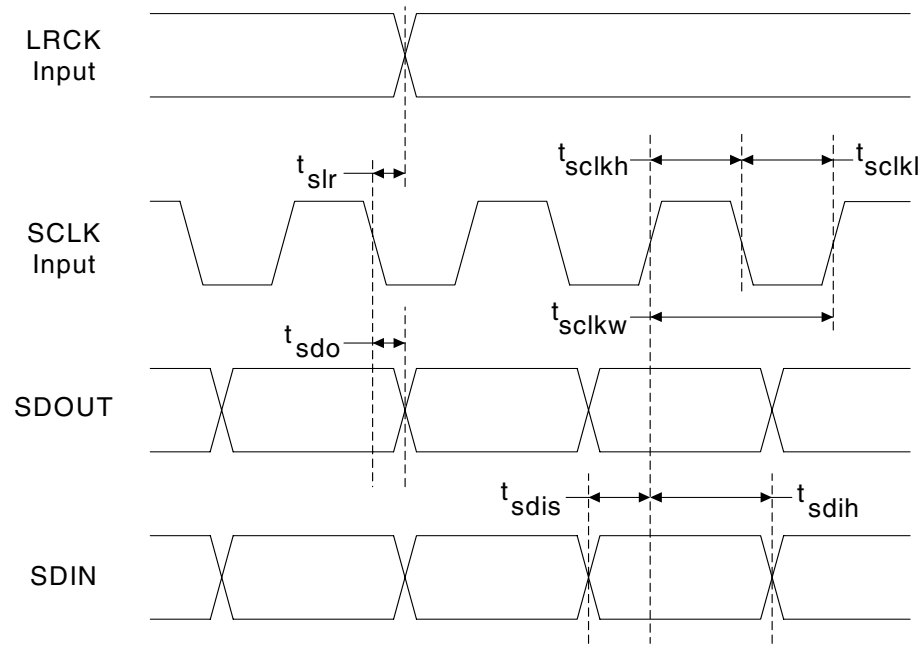


Figure 4. Slave Mode Serial Audio Port Timing

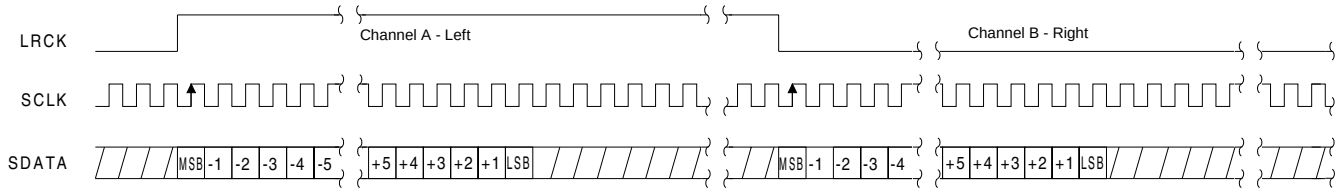


Figure 5. Format 0, Left Justified up to 24-Bit Data

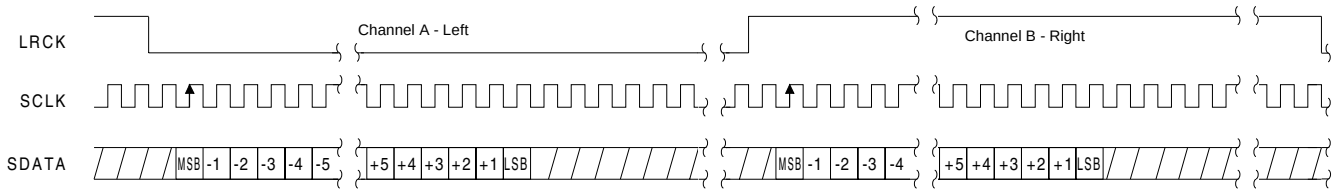


Figure 6. Format 1, I²S up to 24-Bit Data

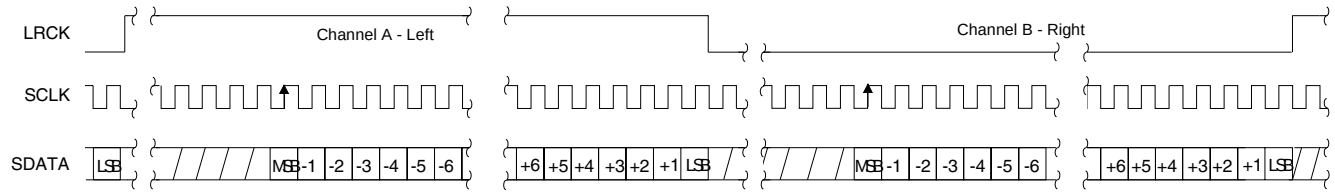


Figure 7. Format 2, Right Justified 16-Bit Data.
Format 3, Right Justified 24-Bit Data.

SWITCHING CHARACTERISTICS - I²C CONTROL PORT

(Inputs: Logic 0 = DGND, Logic 1 = VLC, C_L = 30 pF)

Parameter		Symbol	Min	Max	Unit
SCL Clock Frequency		f_{scl}	-	100	kHz
$\overline{\text{RESET}}$ Rising Edge to Start		t_{irs}	500	-	ns
Bus Free Time Between Transmissions		t_{buf}	4.7	-	µs
Start Condition Hold Time (prior to first clock pulse)		t_{hdst}	4.0	-	µs
Clock Low time		t_{low}	4.7	-	µs
Clock High Time		t_{high}	4.0	-	µs
Setup Time for Repeated Start Condition		t_{sust}	4.7	-	µs
SDA Hold Time from SCL Falling	(Note 23)	t_{hdd}	0	-	µs
SDA Setup time to SCL Rising		t_{sud}	250	-	ns
Rise Time of SCL and SDA	(Note 24)	t_{rc}	-	1	µs
Fall Time SCL and SDA	(Note 24)	t_{fc}	-	300	ns
Setup Time for Stop Condition		t_{susp}	4.7	-	µs
Acknowledge Delay from SCL Falling		t_{ack}	300	1000	ns

Notes: 23. Data must be held for sufficient time to bridge the transition time, t_{fc}, of SCL.

24. Guaranteed by design.

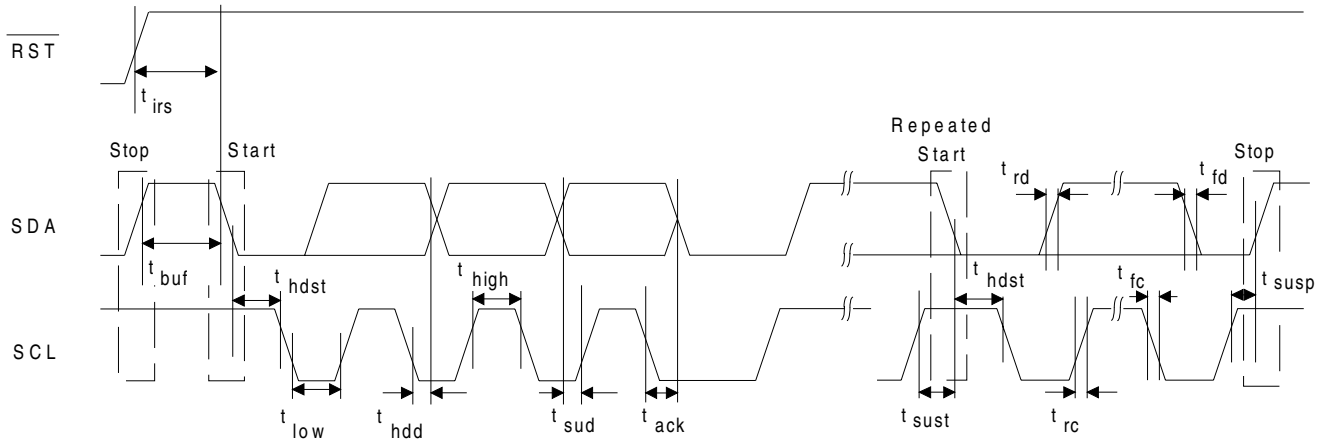


Figure 8. Control Port Timing - I²C Format

3. TYPICAL CONNECTION DIAGRAM

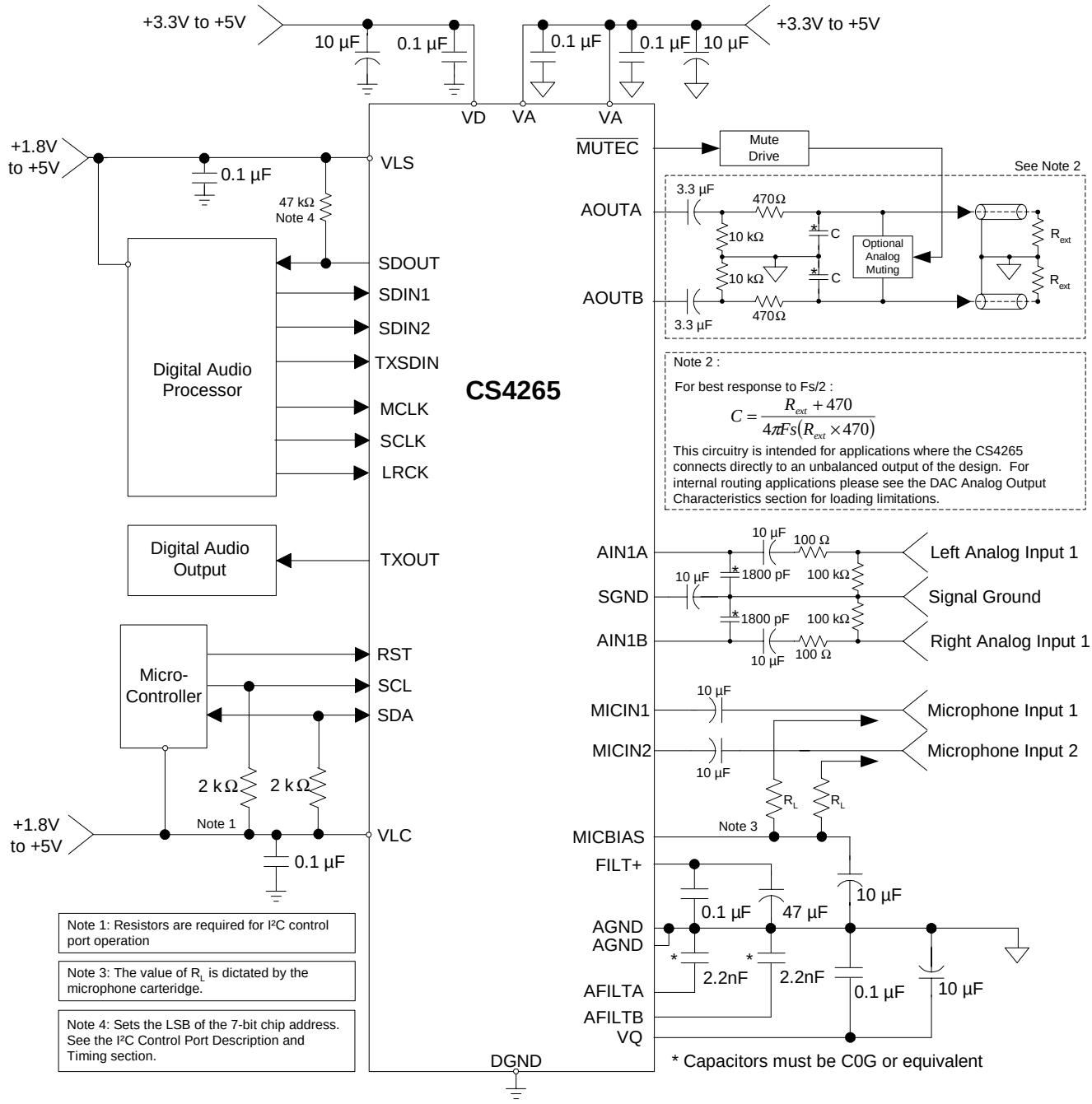


Figure 9. Typical Connection Diagram

4. APPLICATIONS

4.1 Recommended Power-Up Sequence

1) Hold $\overline{\text{RESET}}$ low until the power supply, MCLK, and LRCK are stable. In this state, the Control Port is reset to its default settings.
2) Bring $\overline{\text{RESET}}$ high. The device will remain in a low power state with the PDN bit set by default. The control port will be accessible.
3) The desired register settings can be loaded while the PDN bit remains set.
4) Clear the PDN bit to initiate the power-up sequence.

4.2 System Clocking

The CS4265 will operate at sampling frequencies from 4 kHz to 200 kHz. This range is divided into three speed modes as shown in Table 1 below.

Mode	Sampling Frequency
Single Speed	4-50 kHz
Double Speed	50-100 kHz
Quad Speed	100-200 kHz

Table 1. Speed Modes

4.2.1 Master Clock

MCLK/LRCK must maintain an integer ratio as shown in Table 2. The LRCK frequency is equal to Fs, the frequency at which audio samples for each channel are clocked into or out of the device. The FM bits (see page 35) and the MCLK Freq bits (see page 36) configure the device to generate the proper clocks in Master Mode and receive the proper clocks in Slave Mode. Table 2 illustrates several standard audio sample rates and the required MCLK and LRCK frequencies.

LRCK (kHz)	MCLK (MHz)								
	64x	96x	128x	192x	256x	384x	512x	768x	1024x
32	-	-	-	-	8.1920	12.2880	16.3840	24.5760	32.7680
44.1	-	-	-	-	11.2896	16.9344	22.5792	33.8680	45.1584
48	-	-	-	-	12.2880	18.4320	24.5760	36.8640	49.1520
64	-	-	8.1920	12.2880	16.3840	24.5760	32.7680	-	-
88.2	-	-	11.2896	16.9344	22.5792	33.8680	45.1584	-	-
96	-	-	12.2880	18.4320	24.5760	36.8640	49.1520	-	-
128	8.1920	12.2880	16.3840	24.5760	32.7680	-	-	-	-
176.4	11.2896	16.9344	22.5792	33.8680	45.1584	-	-	-	-
192	12.2880	18.4320	24.5760	36.8640	49.1520	-	-	-	-
Mode	**QSM**					**DSM**		**SSM**	

Table 2. Common Clock Frequencies

4.2.2 Master Mode

As a clock master, LRCK and SCLK will operate as outputs. LRCK and SCLK are internally derived from MCLK with LRCK equal to Fs and SCLK equal to 64 x Fs as shown in Figure 10.

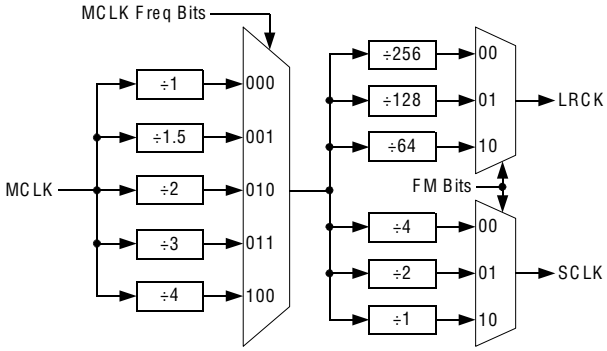


Figure 10. Master Mode Clocking

4.2.3 Slave Mode

In Slave mode, SCLK and LRCK operate as inputs. The Left/Right clock signal must be equal to the sample rate, Fs, and must be synchronously derived from the supplied master clock, MCLK.

The serial bit clock, SCLK, must be synchronously derived from the master clock, MCLK, and be equal to 128x, 64x, 48x or 32x Fs depending on the desired speed mode. Refer to Table 3 for required clock ratios.

	Single Speed	Double Speed	Quad Speed
SCLK/LRCK Ratio	32x, 48x, 64x, 128x	32x, 48x, 64x	32x, 48x, 64x

Table 3. Slave Mode Serial Bit Clock Ratios

4.3 High Pass Filter and DC Offset Calibration

When using operational amplifiers in the input circuitry driving the CS4265, a small DC offset may be driven into the A/D converter. The CS4265 includes a high pass filter after the decimator to remove any DC offset which could result in recording a DC level, possibly yielding clicks when switching between devices in a multichannel system.

The high pass filter continuously subtracts a measure of the DC offset from the output of the decimation filter. If the HPFFreeze bit (see page 35) is set during normal operation, the current value of the DC offset for the each channel is frozen and this DC offset will continue to be subtracted from the conversion result. This feature makes it possible to perform a system DC offset calibration by:

1) Running the CS4265 with the high pass filter enabled until the filter settles. See the ADC Digital Filter Characteristics section for filter settling time.
2) Disabling the high pass filter and freezing the stored DC offset.

A system calibration performed in this way will eliminate offsets anywhere in the signal path between the calibration point and the CS4265.

4.4 Analog Input Multiplexer, PGA, and Mic Gain

The CS4265 contains a stereo 2-to-1 analog input multiplexer followed by a programmable gain amplifier (PGA). The input multiplexer is able to select either a line-level input source, or a mic-level input source and route it to the PGA. The mic-level input passes through a +32 dB gain stage prior to the input multiplexer, allowing it to be used for microphone level signals without the need for any external gain. The PGA stage provides 12 dB of gain or attenuation in 0.5 dB steps. Figure 11 shows the architecture of the input multiplexer, PGA, and mic gain stages.

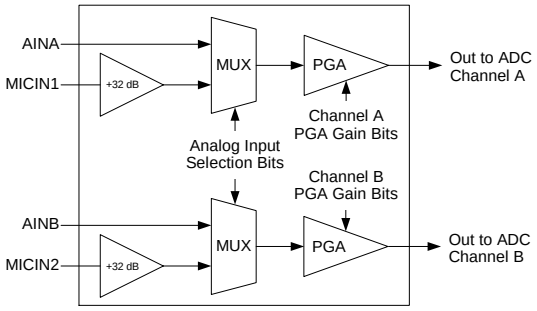


Figure 11. Analog Input Architecture

The “Analog Input Selection (Bit 0)” section on page 38 outlines the bit settings necessary to control the input multiplexer and mic gain. “Channel A PGA Control - Address 07h” on page 36 and “Channel B PGA Control - Address 08h” on page 37 outlines the register settings necessary to control the PGA. By default, the line level input is selected by the input multiplexer, and the PGA is set to 0 dB.

4.5 Input Connections

The analog modulator samples the input at 6.144 MHz (MCLK=12.288 MHz). The digital filter will reject signals within the stopband of the filter. However, there is no rejection for input signals which are ($n \times 6.144$ MHz) the digital passband frequency, where n=0,1,2,... Refer to the Typical Connection Diagram for the recommended analog input circuit that will attenuate noise energy at 6.144 MHz. The use of capacitors which have a large voltage coefficient (such as general purpose ceramics) must be avoided since these can degrade signal linearity. Any unused analog input pairs should be left unconnected.

4.5.1 Pseudo-Differential Input

The CS4265 implements a pseudo-differential input stage. The SGND input is intended to be used as a pseudo-differential reference signal. This feature allows for common mode noise rejection with single-ended signals. Figure 12 shows a basic diagram outlining the internal implementation of the pseudo-differential input stage. The Typical Connection Diagram shows the recommended pseudo-differential input topology. If pseudo-differential input

functionality is not required, simply connect the SGND pin to AGND through the parallel combination of a 10 µF and a 0.1 µF capacitor.

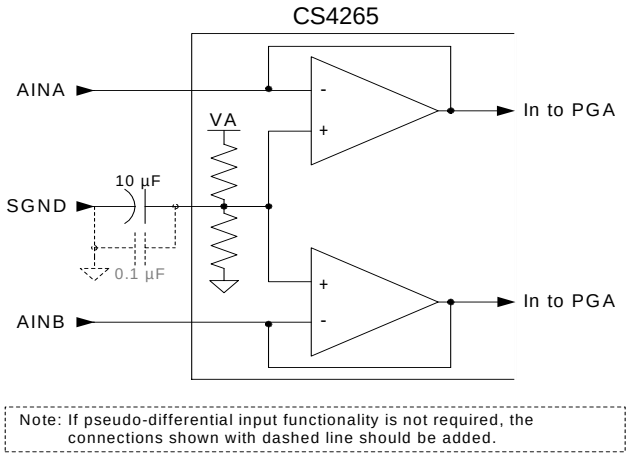


Figure 12. Pseudo-Differential Input Stage

4.6 Output Connections

The CS4265 DAC's implement a switched-capacitor filter followed by a continuous time low pass filter. Its response, combined with that of the digital interpolator, is shown in the "DAC Filter Plots" section beginning on page 45. The recommended external analog circuitry is shown in the Typical Connection Diagram.

The CS4265 DAC is a linear phase design and does not include phase or amplitude compensation for an external filter. Therefore, the DAC system phase and amplitude response will be dependent on the external analog circuitry.

4.7 Output Transient Control

The CS4265 uses Popguard™ technology to minimize the effects of output transients during power-up and power-down. This technique eliminates the audio transients commonly produced by single-ended single-supply converters when it is implemented with external DC-blocking capacitors connected in series with the audio outputs. To make best use of this feature, it is necessary to understand its operation.

4.7.1 Power-up

When the device is initially powered-up, the DAC outputs AOUTA and AOUTB are clamped to VQ which is initially low. After the PDN bit is released (set to '0'), the outputs begin to ramp with VQ towards the nominal quiescent voltage. This ramp takes approximately 200 ms to complete. The gradual voltage ramping allows time for the external DC-blocking capacitors to charge to VQ, effectively blocking the quiescent DC voltage. Audio output will begin after approximately 2000 sample periods.

4.7.2 Power-down

To prevent audio transients at power-down the DC-blocking capacitors must fully discharge before turning off the power. In order to do this, either the PDN should be set or the device should be reset about 250 ms before removing power. During this time, the voltage on VQ and the DAC outputs will gradually discharge to GND. If power is removed before this 250 ms time period has passed a transient will occur when the VA supply drops below that of VQ. There is no minimum time for a power cycle, power may be re-applied at any time.

4.7.3 Serial Interface Clock Changes

When changing the clock ratio or sample rate it is recommended that zero data (or near zero data) be present on the selected SDIN pin for at least 10 LRCK samples before the change is made. During the clocking change the DAC outputs will always be in a zero data state. If non-zero serial audio input is present at the time of switching, a slight click or pop may be heard as the DAC output automatically goes to it's zero data state.

4.8 DAC Serial Data Input Multiplexer

The CS4265 contains a 2-to-1 serial data input multiplexer. This allows two separate data sources to be input into the DAC without the use of any external multiplexing components. The “DAC SDIN Source (Bit 7)” section on page 36 describes the control port settings necessary to control the multiplexer.

4.9 De-Emphasis Filter

The CS4265 includes on-chip digital de-emphasis optimized for a sample rate of 44.1 kHz. The filter response is shown in Figure 13. The frequency response of the de-emphasis curve will scale proportionally with changes in sample rate, Fs. Please see section 6.3.3 for de-emphasis control.

The de-emphasis feature is included to accommodate audio recordings that utilize 50/15 µs pre-emphasis equalization as a means of noise reduction.

De-emphasis is only available in Single Speed Mode.

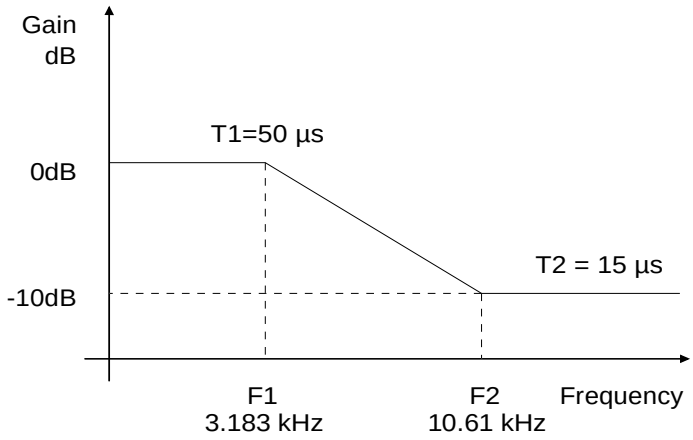


Figure 13. De-Emphasis Curve

4.10 Internal Digital Loopback

The CS4265 supports an internal digital loopback mode in which the output of the ADC is routed to the input of the DAC. This mode may be activated by setting the LOOP bit in the Signal Selection register (06h - See page 36).

When this bit is set, the status of the DAC_DIF[1:0] bits in register 03h will be disregarded by the CS4265. Any changes made to the DAC_DIF[1:0] bits while the LOOP bit is set will have no impact on operation until the LOOP bit is cleared, at which time the Digital Interface Format of the DAC will operate according to the format selected by the DAC_DIF[1:0] bits. While the LOOP bit is set, data will be present on the SDOUT pin in the format selected by the ADC_DIF bit in register 04h.

4.11 Mute Control

The $\overline{\text{MUTEC}}$ pin becomes active during power-up initialization, reset, muting, if the MCLK to LRCK ratio is incorrect, and during power-down. The $\overline{\text{MUTEC}}$ pin is intended to be used as control for an external mute circuit in order to add off-chip mute capability.

Use of the Mute Control function is not mandatory but recommended for designs requiring the absolute minimum in extraneous clicks and pops. Also, use of the Mute Control function can enable the system designer to achieve idle

channel noise/signal-to-noise ratios which are only limited by the external mute circuit. The $\overline{\text{MUTEC}}$ pin is an active-low CMOS driver. See Figure 14 below for a suggested active-low mute circuit.

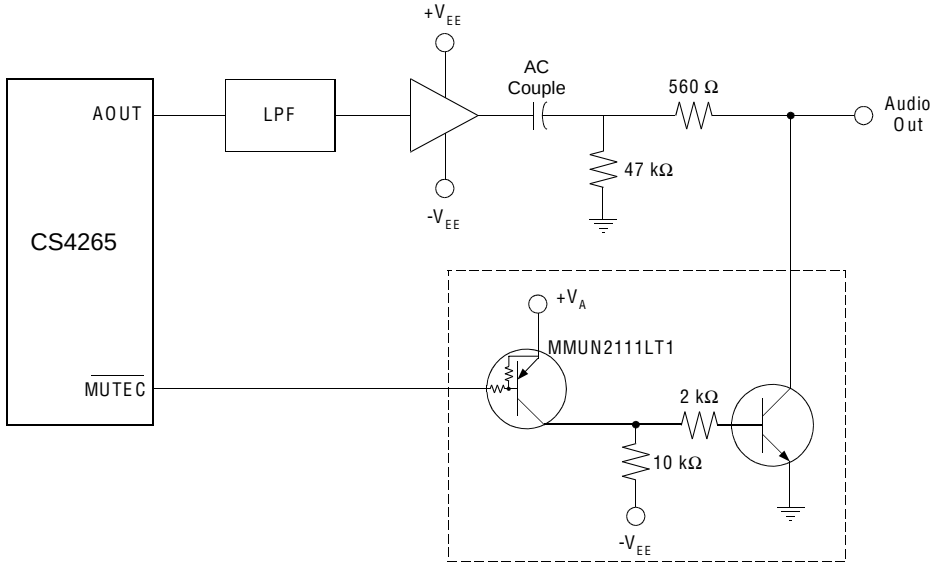


Figure 14. Suggested Active-Low Mute Circuit

4.12 AES3 Transmitter

The CS4265 includes an IEC60958-3 digital audio transmitter. A comprehensive buffering scheme provides write access to the channel status data. This buffering scheme is described in “Channel Status Buffer Management” on page 50.

The IEC60958-3 transmitter encodes and transmits audio and digital data according to the IEC60958-3 (S/PDIF) interface standard. Audio and control data are multiplexed together and bi-phase mark encoded. The resulting bit stream is driven to an output connector either directly or through a transformer. The transmitter is clocked from the clock input pin MCLK.

The channel status (C) bits in the transmitted data stream are taken from storage areas within the CS4265. The user can manually access the internal storage of the CS4265 to configure the transmitted channel status data. The section “Channel Status Buffer Management” on page 50 describes the method of manually accessing the storage areas. The CS4265 transmits all ‘0’s in the user (U) data fields.

4.12.1 TxOut Driver

The line driver is a low skew, low impedance, single-ended output capable of driving cables directly. The driver is set to ground during reset ($\overline{\text{RESET}}$ = LOW), when no transmit clock is provided, and optionally under the control of a register bit. The CS4265 also allows immediate muting of the IEC60958-3 transmitter audio data through a control register bit.

External components are used to terminate and isolate the external cable from the CS4265. These components are detailed in “External IEC60958-3 Transmitter Components” on page 49.

4.12.2 Mono Mode Operation

An IEC60958-3 stream may be used in more than one way to transmit 192 kHz sample rate data. One method is to double the frame rate of the current format. This results is a stereo signal with a sample rate of 192 kHz. An alternate method is implemented using the two sub-frames in a 96 kHz frame rate IEC60958-3 signal to carry consecutive samples of a mono signal, resulting in a 192 kHz sample rate stream. This allows older equipment, whose IEC60958-3 transmitters and receivers are not rated for 192 kHz frame rate operation, to handle 192 kHz sample

rate information. In this “mono mode”, two cables are needed for stereo data transfer. The CS4265 offers mono mode operation. The CS4265 is set placed into and out of mono mode with the MMT control bit.

In mono mode, the input port will run at the audio sample rate (Fs), while the IEC60958-3 transmitter frame rate will be at Fs/2. Consecutive left or right channel serial audio data samples may be selected for transmission on the A and B sub-frames, and the channel status block transmitted is also selectable.

Using mono mode is only necessary if the incoming audio sample rate is already at 192 kHz and contains both left and right audio data words. The “mono mode” IEC60958-3 output stream may also be achieved by keeping the CS4265 in normal stereo mode, and placing consecutive audio samples in the left and right positions in an incoming 96 kHz word rate data stream.

4.13 I²C Control Port Description and Timing

The control port is used to access the registers, allowing the CS4265 to be configured for the desired operational modes and formats. The operation of the control port may be completely asynchronous with respect to the audio sample rates. However, to avoid potential interference problems, the control port pins should remain static if no operation is required.

SDA is a bidirectional data line. Data is clocked into and out of the part by the clock, SCL. A 47 kΩ pull-up or pull-down on the SDOUT pin will set AD0, the least significant bit of the chip address. A pull-up to VLS will set AD0 to ‘1’ and a pull-down to DGND will set AD0 to ‘0’. The state of SDOUT is sensed and AD0 is set upon the release of RESET.

The signal timings for a read and write cycle are shown in Figure 15 and Figure 16. A Start condition is defined as a falling transition of SDA while the clock is high. A Stop condition is a rising transition while the clock is high. All other transitions of SDA occur while the clock is low. The first byte sent to the CS4265 after a Start condition consists of a 7 bit chip address field and a R/$\overline{W}$ bit (high for a read, low for a write). The upper 6 bits of the 7-bit address field are fixed at 100111. To communicate with a CS4265, the chip address field, which is the first byte sent to the CS4265, should match 100111 followed by the setting of AD0. The eighth bit of the address is the R/$\overline{W}$ bit. If the operation is a write, the next byte is the Memory Address Pointer (MAP) which selects the register to be read or written. If the operation is a read, the contents of the register pointed to by the MAP will be output. Setting the auto increment bit in MAP allows successive reads or writes of consecutive registers. Each byte is separated by an acknowledge bit. The ACK bit is output from the CS4265 after each input byte is read, and is input to the CS4265 from the microcontroller after each transmitted byte.

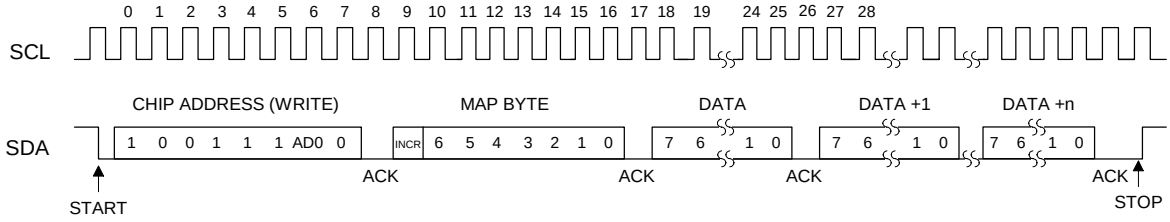


Figure 15. Control Port Timing, I²C Write

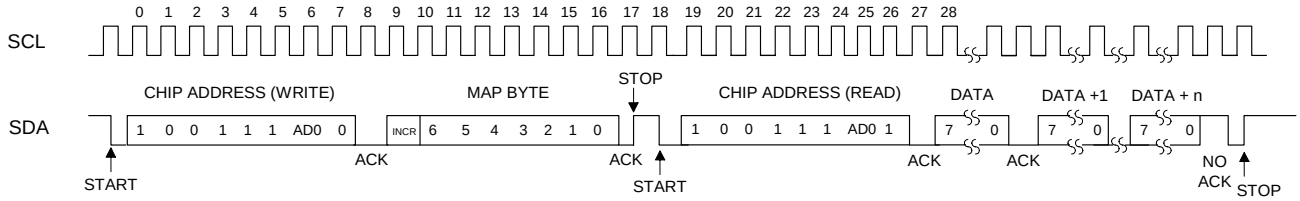


Figure 16. Control Port Timing, I²C Read

Since the read operation can not set the MAP, an aborted write operation is used as a preamble. As shown in Figure 16, the write operation is aborted after the acknowledge for the MAP byte by sending a stop condition. The following pseudocode illustrates an aborted write operation followed by a read operation.

Send start condition.

Send 100111x0 (chip address & write operation).

Receive acknowledge bit.

Send MAP byte, auto increment off.

Receive acknowledge bit.

Send stop condition, aborting write.

Send start condition.

Send 100111x1(chip address & read operation).

Receive acknowledge bit.

Receive byte, contents of selected register.

Send acknowledge bit.

Send stop condition.

Setting the auto increment bit in the MAP allows successive reads or writes of consecutive registers. Each byte is separated by an acknowledge bit.

4.14 Status Reporting

The CS4265 has comprehensive status reporting capabilities. Many conditions can be reported in the status register, as listed in the status register descriptions. See “Status - Address 0Dh” on page 39. Each source may be masked off through mask register bits. In addition, each source may be set to rising edge, falling edge, or level sensitive. Combined with the option of level sensitive or edge sensitive modes within the microcontroller, many different configurations are possible, depending on the needs of the equipment designer.

4.15 Reset

When $\overline{\text{RESET}}$ is low, the CS4265 enters a low power mode and all internal states are reset, including the control port and registers, and the outputs are muted. When $\overline{\text{RESET}}$ is high, the control port becomes operational and the desired settings should be loaded into the control registers. Writing a 0 to the PDN bit in the Power Control register will then cause the part to leave the low power state and begin operation.

The delta-sigma modulators settle in a matter of microseconds after the analog section is powered, either through the application of power or by setting the $\overline{\text{RESET}}$ pin high. However, the voltage reference will take much longer to reach a final value due to the presence of external capacitance on the FILT+ pin. During this voltage reference ramp delay, both SDOUT and DAC outputs will be automatically muted.

It is recommended that $\overline{\text{RESET}}$ be activated if the analog or digital supplies drop below the recommended operating condition to prevent power glitch related issues.

4.16 Synchronization of Multiple Devices

In systems where multiple ADCs are required, care must be taken to achieve simultaneous sampling. To ensure synchronous sampling, the master clocks and left/right clocks must be the same for all of the CS4265's in the system. If only one master clock source is needed, one solution is to place one CS4265 in Master Mode, and slave all of the other CS4265's to the one master. If multiple master clock sources are needed, a possible solution would be to supply all clocks from the same external source and time the CS4265 reset with the inactive edge of master clock. This will ensure that all converters begin sampling on the same clock edge.

4.17 Grounding and Power Supply Decoupling

As with any high resolution converter, the CS4265 requires careful attention to power supply and grounding arrangements if its potential performance is to be realized. Figure 9 shows the recommended power arrangements, with VA connected to a clean supply. VD, which powers the digital filter, may be run from the system logic supply (VLS or VLC) or may be powered from the analog supply (VA) via a resistor. In this case, no additional devices should be powered from VD. Power supply decoupling capacitors should be as near to the CS4265 as possible, with the low value ceramic capacitor being the nearest. All signals, especially clocks, should be kept away from the FILT+ and VQ pins in order to avoid unwanted coupling into the modulators. The FILT+ and VQ decoupling capacitors, particularly the 0.1 µF, must be positioned to minimize the electrical path from FILT+ and AGND. The CS4265 evaluation board demonstrates the optimum layout and power supply arrangements. To minimize digital noise, connect the CS4265 digital outputs only to CMOS inputs.

4.18 Package Considerations

The CS4265 is available in the compact QFN package. The under side of the QFN package reveals a large metal pad that serves as a thermal relief to provide for maximum heat dissipation. This pad must mate with an equally dimensioned copper pad on the PCB and must be electrically connected to ground. A series of vias should be used to connect this copper pad to one or more larger ground planes on other PCB layers. In split ground systems, it is recommended that this thermal pad be connected to AGND for best performance. The CS4265 evaluation board demonstrates the optimum thermal pad and via configuration.

5. REGISTER QUICK REFERENCE

This table shows the register names and their associated default values.

Addr	Function	7	6	5	4	3	2	1	0
01h	Chip ID	PART3	PART2	PART1	PART0	REV3	REV2	REV1	REV0
		1	1	0	1	0	0	0	1
02h	Power Control	Freeze	Reserved	Reserved	Reserved	PDN_MIC	PDN_ADC	PDN_DAC	PDN
		0	0	0	0	0	0	0	1
03h	DAC Control 1	Reserved	Reserved	DAC_DIF1	DAC_DIF0	Reserved	MuteDAC	DeEmph	Reserved
		0	0	0	0	1	0	0	0
04h	ADC Control	FM1	FM0	Reserved	ADC_DIF	Reserved	MuteADC	HPFFreeze	M/$\overline{S}$
		0	0	0	0	0	0	0	0
05h	MCLK Frequency	Reserved	MCLK Freq2	MCLK Freq1	MCLK Freq0	Reserved	Reserved	Reserved	Reserved
		0	0	0	0	0	0	0	0
06h	Signal Selection	SDINSel	Reserved	Reserved	Reserved	Reserved	Reserved	LOOP	Reserved
		0	1	0	0	0	0	0	0
07h	PGA Ch B Gain Control	Reserved	Reserved	Gain5	Gain4	Gain3	Gain2	Gain1	Gain0
		0	0	0	0	0	0	0	0
08h	PGA Ch A Gain Control	Reserved	Reserved	Gain5	Gain4	Gain3	Gain2	Gain1	Gain0
		0	0	0	0	0	0	0	0
09h	Analog Input Control	Reserved	Reserved	Reserved	PGASoft	PGAZero	Reserved	Reserved	Select
		0	0	0	1	1	0	0	1
0Ah	DAC Ch A Volume Control	Vol7	Vol6	Vol5	Vol4	Vol3	Vol2	Vol1	Vol0
		0	0	0	0	0	0	0	0
0Bh	DAC Ch B Volume Control	Vol7	Vol6	Vol5	Vol4	Vol3	Vol2	Vol1	Vol0
		0	0	0	0	0	0	0	0
0Ch	DAC Control 2	DACSoft	DACZero	InvertDAC	Reserved	Reserved	Reserved	Reserved	Reserved
		1	1	0	0	0	0	0	0
0Dh	Status	Reserved	Reserved	Reserved	EFTC	ClkErr	Reserved	ADCOvfl	ADCUndrfl
		0	0	0	0	0	0	0	0
0Eh	Status Mask	Reserved	Reserved	Reserved	EFTCM	ClkErrM	Reserved	ADCOvflM	ADCUndrflM
		0	0	0	0	0	0	0	0
0Fh	Status Mode MSB	Reserved	Reserved	Reserved	EFTC1	ClkErr1	Reserved	ADCOvfl1	ADCUndrfl1
		0	0	0	0	0	0	0	0
10h	Status Mode LSB	Reserved	Reserved	Reserved	EFTC0	ClkErr0	Reserved	ADCOvfl0	ADCUndrfl0
		0	0	0	0	0	0	0	0

Addr	Function	7	6	5	4	3	2	1	0
11h	Transmitter Control 1	Reserved	EFTCI	CAM	Reserved	Reserved	Reserved	Reserved	Reserved
		0	0	0	0	0	0	0	0
12h	Transmitter Control 2	Tx_DIF1	Tx_DIF0	TxOff	TxMute	V	MMT	MMTCS	MMTLR
		0	0	0	0	0	0	0	0
13h - 2Ah	C-Data Buffer	-	-	-	-	-	-	-	-

6. REGISTER DESCRIPTION

6.1 Chip ID - Register 01h

B7	B6	B5	B4	B3	B2	B1	B0
PART3	PART2	PART1	PART0	REV3	REV2	REV1	REV0

Function:

This register is Read-Only. Bits 7 through 4 are the part number ID which is 1101b (0Dh) and the remaining bits (3 through 0) are for the chip revision.

6.2 Power Control - Address 02h

7	6	5	4	3	2	1	0
Freeze	Reserved	Reserved	Reserved	PDN_MIC	PDN_ADC	PDN_DAC	PDN

6.2.1 Freeze (Bit 7)

Function:

This function allows modifications to be made to certain control port bits without the changes taking effect until the Freeze bit is disabled. To make multiple changes to these bits take effect simultaneously, set the Freeze bit, make all changes, then clear the Freeze bit. The bits affected by the Freeze function are listed in Table 4 below.

Table 4. Freeze-able Bits

Name	Register	Bit(s)
MuteDAC	03h	2
MuteADC	04h	2
Gain[5:0]	07h	5:0
Gain[5:0]	08h	5:0
Vol[7:0]	0Ah	7:0
Vol[7:0]	0Bh	7:0
TxMute	0Eh	4

6.2.2 Power Down MIC (Bit 3)

Function:

The microphone preamplifier block will enter a low-power state whenever this bit is set.

6.2.3 Power Down ADC (Bit 2)

Function:

The ADC pair will remain in a reset state whenever this bit is set.

6.2.4 Power Down DAC (Bit 1)

Function:

The DAC pair will remain in a reset state whenever this bit is set.

6.2.5 Power Down Device (Bit 0)

Function:

The device will enter a low-power state whenever this bit is set. The power-down bit is set by default and must be cleared before normal operation can occur. The contents of the control registers are retained when the device is in power-down.

6.3 DAC Control - Address 03h

7	6	5	4	3	2	1	0
Reserved	Reserved	DAC_DIF1	DAC_DIF0	Reserved	MuteDAC	DeEmph	Reserved

6.3.1 DAC Digital Interface Format (Bits 5:4)

Function:

The required relationship between LRCK, SCLK and SDIN for the DAC is defined by the DAC Digital Interface Format and the options are detailed in Table 5 and Figures 5-7.

Table 5. DAC Digital Interface Formats

DAC_DIF1	DAC_DIF0	Description	Format	Figure
0	0	Left Justified, up to 24-bit data (default)	0	5
0	1	I^2S, up to 24-bit data	1	6
1	0	Right Justified, 16-bit Data	2	7
1	1	Right Justified, 24-bit Data	3	7

6.3.2 Mute DAC (Bit 2)

Function:

The DAC outputs will mute and the MUTEC pin will become active when this bit is set. Though this bit is active high, it should be noted that the MUTEC pin is active low. The common mode voltage on the outputs will be retained when this bit is set. The muting function is effected, similar to attenuation changes, by the DACSoft and DACZero bits in the DAC Control 2 register.

6.3.3 De-Emphasis Control (Bit 1)

Function:

The standard 50/15 µs digital de-emphasis filter response, Figure 17, may be implemented for a sample rate of 44.1 kHz when the DeEmph bit is configured as shown in Table 6 below. NOTE: De-emphasis is available only in Single-Speed Mode.

Table 6. De-Emphasis Control

DeEmph	Description
0	Disabled (default)
1	44.1 kHz de-emphasis

6.4 ADC Control - Address 04h

7	6	5	4	3	2	1	0
FM1	FM0	Reserved	ADC_DIF	Reserved	MuteADC	HPFFreeze	M/$\overline{S}$

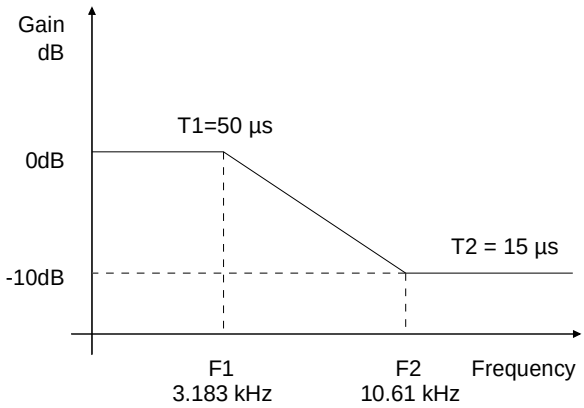


Figure 17. De-Emphasis Curve

6.4.1 Functional Mode (Bits 7:6)

Function:

Selects the required range of sample rates.

Table 7. Functional Mode Selection

FM1	FM0	Mode
0	0	Single-Speed Mode: 4 to 50 kHz sample rates
0	1	Double-Speed Mode: 50 to 100 kHz sample rates
1	0	Quad-Speed Mode: 100 to 200 kHz sample rates
1	1	Reserved

6.4.2 ADC Digital Interface Format (Bit 4)

Function:

The required relationship between LRCK, SCLK and SDOUT is defined by the ADC Digital Interface Format bit. The options are detailed in Table 8 and may be seen in Figure 5 and 6.

Table 8. ADC Digital Interface Formats

ADC_DIF	Description	Format	Figure
0	Left Justified, up to 24-bit data (default)	0	5
1	I^2S, up to 24-bit data	1	6

6.4.3 Mute ADC (Bit 2)

Function:

When this bit is set, the serial audio output of the both ADC channels will be muted.

6.4.4 ADC High Pass Filter Freeze (Bit 1)

Function:

When this bit is set, the internal high-pass filter will be disabled.The current DC offset value will be frozen and continue to be subtracted from the conversion result. See “High Pass Filter and DC Offset Calibration” on page 23.

6.4.5 Master / Slave Mode (Bit 0)

Function:

This bit selects either master or slave operation for the serial audio port. Setting this bit will select master mode, while clearing this bit will select slave mode.

6.5 MCLK Frequency - Address 05h

7	6	5	4	3	2	1	0
Reserved	MCLK Freq2	MCLK Freq1	MCLK Freq0	Reserved	Reserved	Reserved	Reserved

6.5.1 Master Clock Dividers (Bits 6:4)

Function:

Sets the frequency of the supplied MCLK signal. See Table 9 below for the appropriate settings.

Table 9. MCLK Frequency

MCLK Divider	MCLK Freq2	MCLK Freq1	MCLK Freq0
÷ 1	0	0	0
÷ 1.5	0	0	1
÷ 2	0	1	0
÷ 3	0	1	1
÷ 4	1	0	0
Reserved	1	0	1
Reserved	1	1	x

6.6 Signal Selection - Address 06h

7	6	5	4	3	2	1	0
SDINSel	Reserved	Reserved	Reserved	Reserved	Reserved	LOOP	Reserved

6.6.1 DAC SDIN Source (Bit 7)

Function:

This bit is used to select the serial audio data source for the DAC as shown in Table 10 below.

Table 10. DAC SDIN Source Selection

SDINSel Setting	DAC Data Source
0	SDIN1
1	SDIN2

6.6.2 Digital Loopback (Bit 1)

Function:

When this bit is set, an internal digital loopback from the ADC to the DAC will be enabled. Please refer to “Internal Digital Loopback” on page 26.

6.7 Channel A PGA Control - Address 07h

7	6	5	4	3	2	1	0
Reserved	Reserved	Gain5	Gain4	Gain3	Gain2	Gain1	Gain0

6.7.1 Channel A PGA Gain (Bits 5:0)

Function:

See “Channel B PGA Gain (Bits 5:0)” on page 37.

6.8 Channel B PGA Control - Address 08h

7	6	5	4	3	2	1	0
Reserved	Reserved	Gain5	Gain4	Gain3	Gain2	Gain1	Gain0

6.8.1 Channel B PGA Gain (Bits 5:0)

Function:

Sets the gain or attenuation for the ADC input PGA stage. The gain may be adjusted from -12 dB to +12 dB in 0.5 dB steps. The gain bits are in two’s complement with the Gain0 bit set for a 0.5 dB step. Register settings outside of the ±12 dB range are reserved and must not be used. See Table 11 for example settings.

Table 11. Example Gain and Attenuation Settings

Gain[5:0]	Setting
101000	-12 dB
000000	0 dB
011000	+12 dB

6.9 ADC Input Control - Address 09h

7	6	5	4	3	2	1	0
Reserved	Reserved	Reserved	PGASoft	PGAZero	Reserved	Reserved	Select

6.9.1 PGA Soft Ramp or Zero Cross Enable (Bits 4:3)

Function:

Soft Ramp Enable

Soft Ramp allows level changes, both muting and attenuation, to be implemented by incrementally ramping, in 1/8 dB steps, from the current level to the new level at a rate of 1 dB per 8 left/right clock periods. See Table 12 on page 38.

Zero Cross Enable

Zero Cross Enable dictates that signal level changes, either by attenuation changes or muting, will occur on a signal zero crossing to minimize audible artifacts. The requested level change will occur after a time-out period between 512 and 1024 sample periods (10.7 ms to 21.3 ms at 48 kHz sample rate) if the signal does not encounter a zero crossing. The zero cross function is independently monitored and implemented for each channel. See Table 12 on page 38.

Soft Ramp and Zero Cross Enable

Soft Ramp and Zero Cross Enable dictate that signal level changes, either by attenuation changes or muting, will occur in 1/8 dB steps and be implemented on a signal zero crossing. The 1/8 dB level change will occur after a time-out period between 512 and 1024 sample periods (10.7 ms to 21.3 ms at 48 kHz sample rate) if the signal does not encounter a zero crossing. The zero cross function is independently monitored and implemented for each channel. See Table 12 on page 38.

Table 12. PGA Soft Cross or Zero Cross Mode Selection

PGASoft	PGAZeroCross	Mode
0	0	Changes to affect immediately
0	1	Zero Cross enabled
1	0	Soft Ramp enabled
1	1	Soft Ramp and Zero Cross enabled (default)

6.9.2 Analog Input Selection (Bit 0)

Function:

These bits are used to select the input source for the PGA and ADC. Please see Table 13 below.

Table 13. Analog Input Selection

Select	PGA/ADC Input
0	Microphone Level Input
1	Line Level Input

6.10 DAC Channel A Volume Control - Address 0Ah

See 6.11 DAC Channel B Volume Control - Address 0Bh

6.11 DAC Channel B Volume Control - Address 0Bh

7	6	5	4	3	2	1	0
Vol7	Vol6	Vol5	Vol4	Vol3	Vol2	Vol1	Vol0

6.11.1 Volume Control (Bits 7:0)

Function:

The digital volume control allows the user to attenuate the signal in 0.5 dB increments from 0 to -127 dB. The Vol0 bit activates a 0.5 dB attenuation when set, and no attenuation when cleared. The Vol[7:1] bits activate attenuation equal to their decimal equivalent (in dB). Example volume settings are decoded as shown in Table Table 14. The volume changes are implemented as dictated by the DACSoft and DACZeroCross bits in the DAC Control 2 register (see section 6.12.1).

Table 14. Digital Volume Control Example Settings

Binary Code	Volume Setting
00000000	0 dB
00000001	-0.5 dB
00101000	-20 dB
00101001	-20.5 dB
11111110	-127 dB
11111111	-127.5 dB

6.12 DAC Control 2 - Address 0Ch

7	6	5	4	3	2	1	0
DACSoft	DACZero	InvertDAC	Reserved	Reserved	Reserved	Reserved	Reserved

6.12.1 DAC Soft Ramp or Zero Cross Enable (Bits 7:6)

Function:

Soft Ramp Enable

Soft Ramp allows level changes, both muting and attenuation, to be implemented by incrementally ramping, in 1/8 dB steps, from the current level to the new level at a rate of 1 dB per 8 left/right clock periods. See Table 15 on page 39.

Zero Cross Enable

Zero Cross Enable dictates that signal level changes, either by attenuation changes or muting, will occur on a signal zero crossing to minimize audible artifacts. The requested level change will occur after a time-out period between 512 and 1024 sample periods (10.7 ms to 21.3 ms at 48 kHz sample rate) if the signal does not encounter a zero crossing. The zero cross function is independently monitored and implemented for each channel. See Table 15 on page 39.

Soft Ramp and Zero Cross Enable

Soft Ramp and Zero Cross Enable dictate that signal level changes, either by attenuation changes or muting, will occur in 1/8 dB steps and be implemented on a signal zero crossing. The 1/8 dB level change will occur after a time-out period between 512 and 1024 sample periods (10.7 ms to 21.3 ms at 48 kHz sample rate) if the signal does not encounter a zero crossing. The zero cross function is independently monitored and implemented for each channel. See Table 15 on page 39.

Table 15. DAC Soft Cross or Zero Cross Mode Selection

DACSoft	DACZeroCross	Mode
0	0	Changes to affect immediately
0	1	Zero Cross enabled
1	0	Soft Ramp enabled
1	1	Soft Ramp and Zero Cross enabled (default)

6.12.2 Invert DAC Output (Bit 5)

Function:

When this bit is set, the output of the DAC will be inverted.

6.13 Status - Address 0Dh

7	6	5	4	3	2	1	0
Reserved	Reserved	Reserved	EFTC	ClkErr	Reserved	ADCOvfl	ADCUndrfl

For all bits in this register, a ‘1’ means the associated condition has occurred at least once since the register was last read. A ‘0’ means the associated condition has NOT occurred since the last reading of the register. Status bits that are masked off in the associated mask register will always be ‘0’ in this register. This register defaults to 00h.

6.13.1 E to F C-buffer Transfer

Function:

Indicates the completion of an E to F C-buffer transfer. See “Channel Status Buffer Management” on page 50 for more information.

6.13.2 Clock Error (Bit 3)

Function:

Indicates the occurrence of a clock error condition.

6.13.3 ADC Overflow (Bit 1)

Function:

Indicates the occurrence of an ADC overflow condition.

6.13.4 ADC Underflow (Bit 0)

Function:

Indicates the occurrence of an ADC underflow condition.

6.14 Status Mask - Address 0Eh

7	6	5	4	3	2	1	0
Reserved	Reserved	Reserved	EFTCM	ClkErrM	Reserved	ADCOvflM	ADCUndrflM

Function:

The bits of this register serve as a mask for the Status sources found in the register "Status - Address 0Dh" on page 39. If a mask bit is set to 1, the error is unmasked, meaning that its occurrence will affect the status register. If a mask bit is set to 0, the error is masked, meaning that its occurrence will not affect the status register. The bit positions align with the corresponding bits in the Status register.

6.15 Status Mode MSB - Address 0Fh

6.16 Status Mode LSB - Address 10h

7	6	5	4	3	2	1	0
Reserved	Reserved	Reserved	EFTC1	ClkErr1	Reserved	ADCOvfl1	ADCUndrfl1
Reserved	Reserved	Reserved	EFTC0	ClkErr0	Reserved	ADCOvfl0	ADCUndrfl0

Function:

The two Status Mode registers form a 2-bit code for each Status register function. There are three ways to update the Status register in accordance with the status condition. In the Rising edge active mode, the status bit becomes active on the arrival of the condition. In the Falling edge active mode, the status bit becomes active on the removal of the condition. In Level active mode, the status bit is active during the condition.

00 - Rising edge active
01 - Falling edge active
10 - Level active
11 - Reserved

6.17 Transmitter Control 1 - Address 11h

7	6	5	4	3	2	1	0
Reserved	EFTCI	CAM	Reserved	Reserved	Reserved	Reserved	Reserved

6.17.1 E to F C-Data Buffer Transfer Inhibit (Bit 6)

Function:

When cleared, C-data E to F buffer transfers are allowed. When set, C-data E to F buffer transfers are inhibited. See "IEC60958-3 Channel Status (C) Bit Management" on page 50.

6.17.2 C-Data Access Mode (Bit 5)

Function:

When cleared, the C-data buffer will operate in One-byte control port access mode. When set, the C-data buffer will operate in Two-byte control port access mode. See “IEC60958-3 Channel Status (C) Bit Management” on page 50.

6.18 Transmitter Control 2 - Address 12h

7	6	5	4	3	2	1	0
Tx_DIF1	Tx_DIF0	TxOff	TxMute	V	MMT	MMTCS	MMTLR

6.18.1 Transmitter Digital Interface Format (Bits 7:6)

Function:

The required relationship between LRCK, SCLK and SDIN for the transmitter is defined by the Transmitter Digital Interface Format and the options are detailed in Table 16 and Figures 5-7.

Table 16. Transmitter Digital Interface Formats

Tx_DIF1	Tx_DIF0	Description	Format	Figure
0	0	Left Justified, up to 24-bit data (default)	0	5
0	1	I^2S, up to 24-bit data	1	6
1	0	Right Justified, 16-bit Data	2	7
1	1	Right Justified, 24-bit Data	3	7

6.18.2 Transmitter Output Driver Control (Bit 5)

Function:

When this bit is cleared, the transmitter output pin driver will be in the normal operational mode. When set, the transmitter output pin driver will drive to a constant 0 V.

6.18.3 Transmitter Mute Control (Bit 4)

Function:

When this bit is cleared, the transmitter data will be in the normal operational mode. When set, the transmitter will output all zero data.

6.18.4 Transmitted Validity Bit Control (Bit 3)

Function:

This bit sets the transmitted Validity bit level.

When this bit is cleared, valid linear PCM audio data is indicated. When this bit is set, invalid or non-linear PCM audio data is indicated.

6.18.5 Transmitter Mono/Stereo Operation Control (Bit 2)

Function:

When this bit is cleared, the transmitter will operate in stereo mode. When set, the transmitter will operate in mono mode with one input channel’s data output in both A and B subframes (see “IEC60958-3 Channel Status (C) Bit Management” on page 50) and the CS data defined by the MMTCS bit (see section 6.18.6).

6.18.6 Mono Mode CS Data Source (Bit 1)

Function:

When this bit is cleared, the transmitter will transmit the channel A CS data in the A subframe and the channel B CS data in the B subframe.

When this bit is set, the transmitter will transmit the CS data defined for the channel selected by the MMTLR bit in both the A and B subframes.

6.18.7 Mono Mode Channel Selection (Bit 0)

Function:

When this bit is cleared, channel A input data will be transmitted in both channel A and B subframes in mono mode. When this bit is set, channel B input data will be transmitted in both channel A and B subframes in mono mode.

7. PARAMETER DEFINITIONS

Dynamic Range

The ratio of the rms value of the signal to the rms sum of all other spectral components over the specified bandwidth. Dynamic Range is a signal-to-noise ratio measurement over the specified bandwidth made with a -60 dBFS signal. 60 dB is added to resulting measurement to refer the measurement to full-scale. This technique ensures that the distortion components are below the noise level and do not affect the measurement. This measurement technique has been accepted by the Audio Engineering Society, AES17-1991, and the Electronic Industries Association of Japan, EIAJ CP-307. Expressed in decibels.

Total Harmonic Distortion + Noise

The ratio of the rms value of the signal to the rms sum of all other spectral components over the specified bandwidth (typically 10 Hz to 20 kHz), including distortion components. Expressed in decibels. Measured at -1 and -20 dBFS as suggested in AES17-1991 Annex A.

Frequency Response

A measure of the amplitude response variation from 10 Hz to 20 kHz relative to the amplitude response at 1 kHz. Units in decibels.

Interchannel Isolation

A measure of crosstalk between the left and right channels. Measured for each channel at the converter's output with no signal to the input under test and a full-scale signal applied to the other channel. Units in decibels.

Interchannel Gain Mismatch

The gain difference between left and right channels. Units in decibels.

Gain Error

The deviation from the nominal full-scale analog output for a full-scale digital input.

Gain Drift

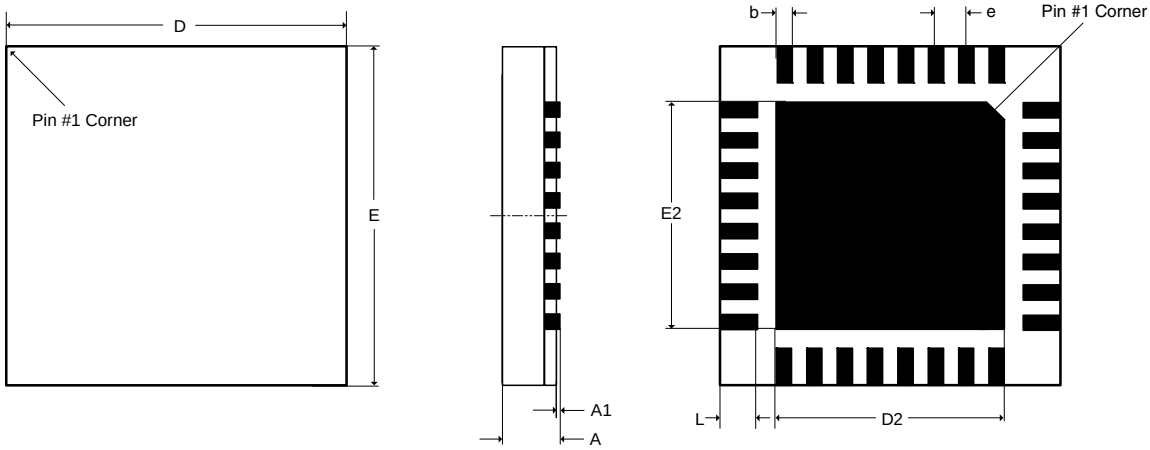
The change in gain value with temperature. Units in ppm/°C.

Offset Error

The deviation of the mid-scale transition (111...111 to 000...000) from the ideal. Units in mV.

8. PACKAGE DIMENSIONS

32L QFN (5 X 5 mm BODY) PACKAGE DRAWING



	INCHES			MILLIMETERS			NOTE
DIM	MIN	NOM	MAX	MIN	NOM	MAX	
A	--	--	0.0394	--	--	1.00	1
A1	0.0000	--	0.0020	0.00	--	0.05	1
b	0.0071	0.0091	0.0110	0.18	0.23	0.28	1,2
D		0.1969 BSC			5.00 BSC		1
D2	0.1280	0.1299	0.1319	3.25	3.30	3.35	1
E		0.1969 BSC			5.00 BSC		1
E2	0.1280	0.1299	0.1319	3.25	3.30	3.35	1
e		0.0197 BSC			0.50 BSC		1
L	0.0118	0.0157	0.0197	0.30	0.40	0.50	1

JEDEC #: MO-220

Controlling Dimension is Millimeters.

Notes: 1. Dimensioning and tolerance per ASME Y 14.5M-1995.

2. Dimensioning lead width applies to the plated terminal and is measured between 0.20 mm and 0.25 mm from the terminal tip.

9. THERMAL CHARACTERISTICS AND SPECIFICATIONS

Parameters		Symbol	Min	Typ	Max	Units
Package Thermal Resistance (Note 3)	32-QFN	θ_{JA}	-	38	-	°C/Watt
		θ_{JC}	-	52	-	°C/Watt
Allowable Junction Temperature			-	-	125	°C

Notes: 3. θ_{JA} is specified according to JEDEC specifications for multi-layer PCBs.

APPENDIX A: DAC FILTER PLOTS

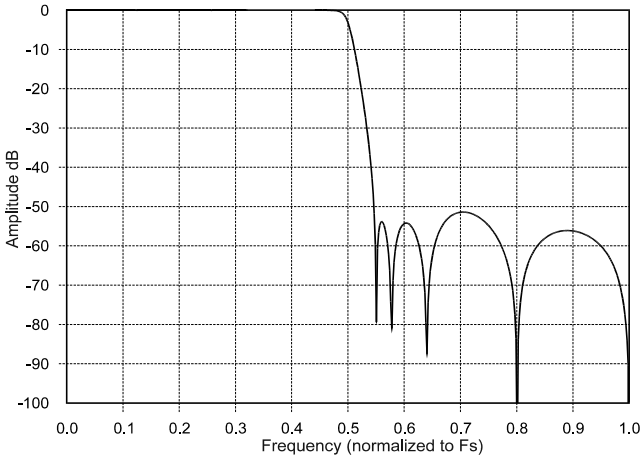


Figure 18. DAC Single Speed Stopband Rejection

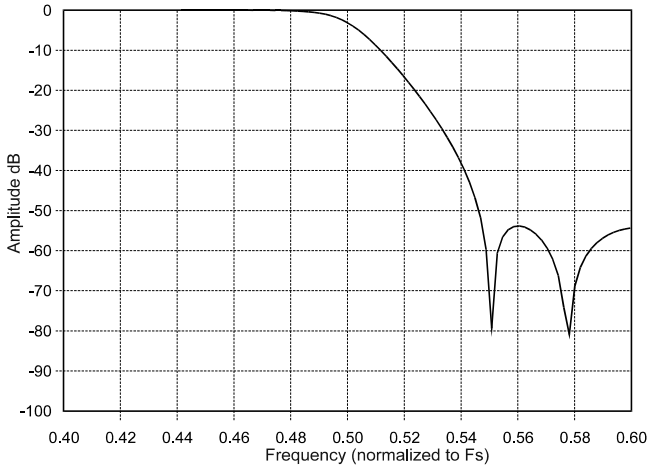


Figure 19. DAC Single Speed Transition Band

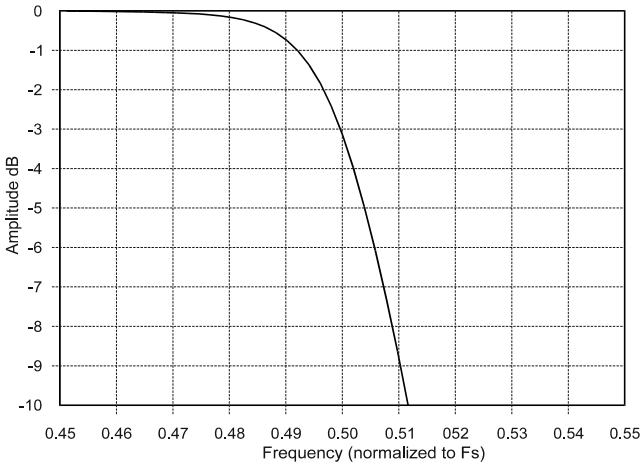


Figure 20. DAC Single Speed Transition Band

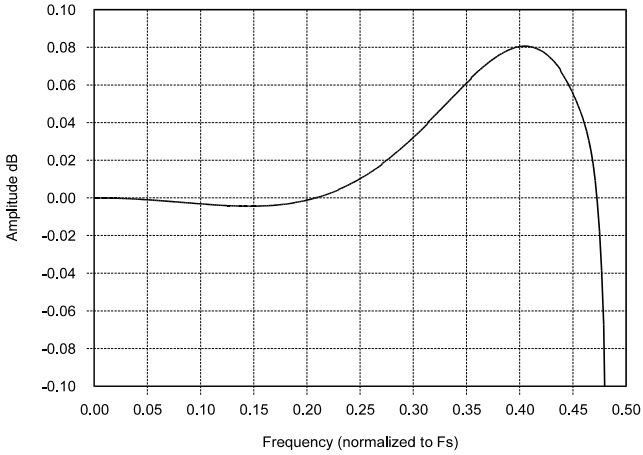


Figure 21. DAC Single Speed Passband Ripple

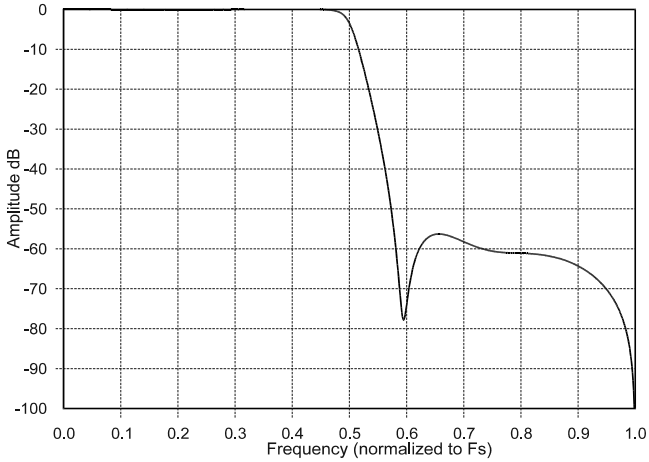


Figure 22. DAC Double Speed Stopband Rejection

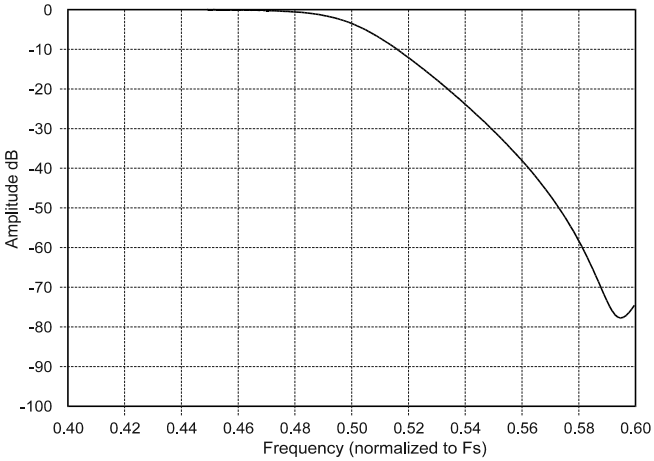


Figure 23. DAC Double Speed Transition Band

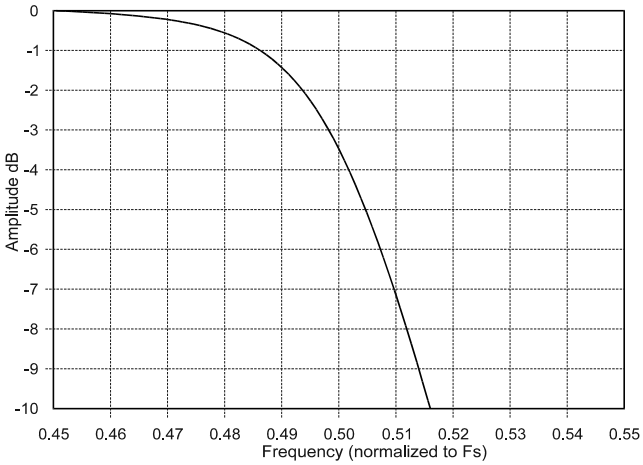


Figure 24. DAC Double Speed Transition Band

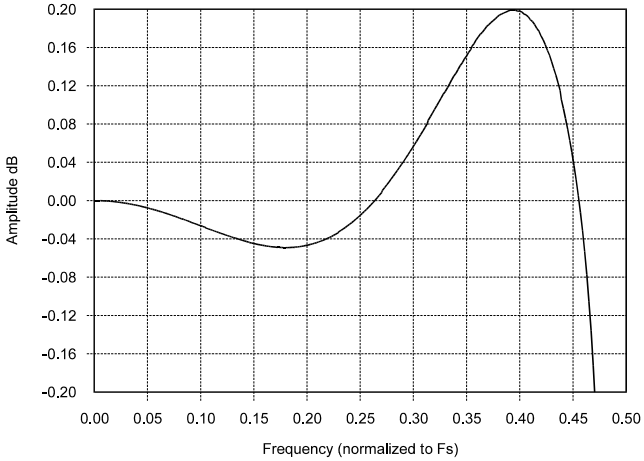


Figure 25. DAC Double Speed Passband Ripple

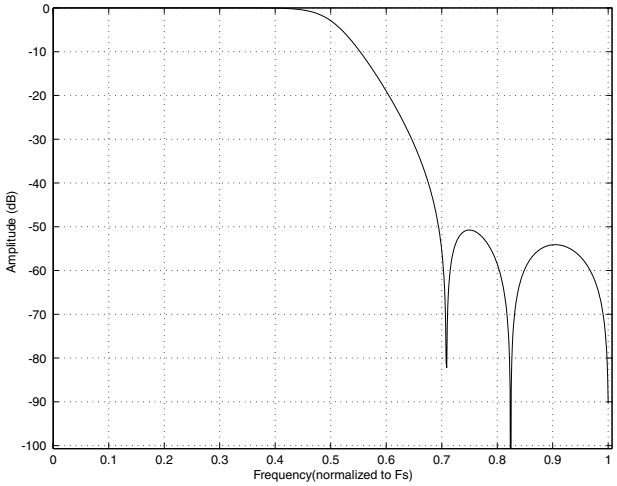


Figure 26. DAC Quad Speed Stopband Rejection

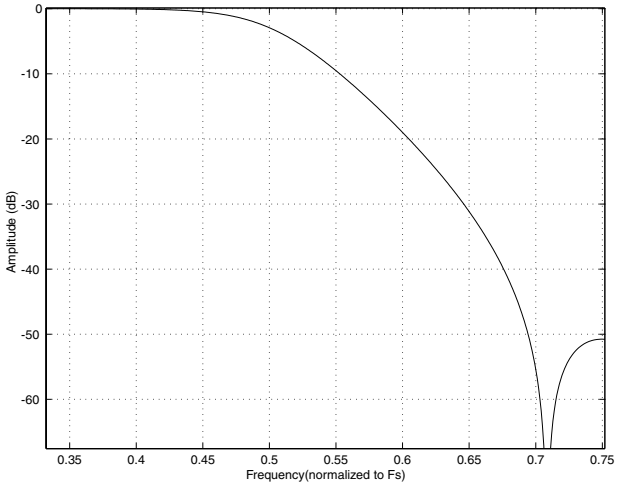


Figure 27. DAC Quad Speed Transition Band

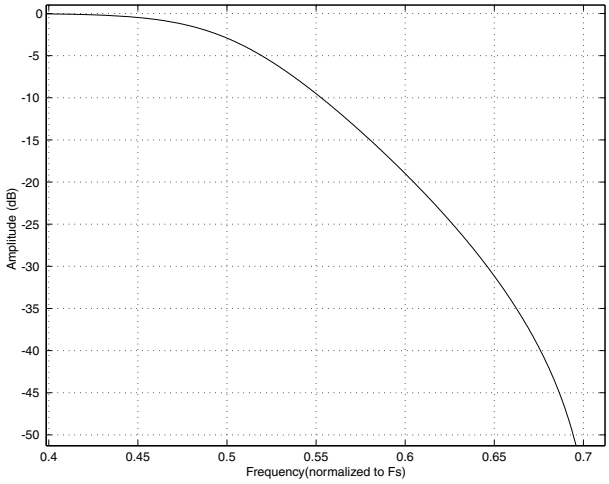


Figure 28. DAC Quad Speed Transition Band

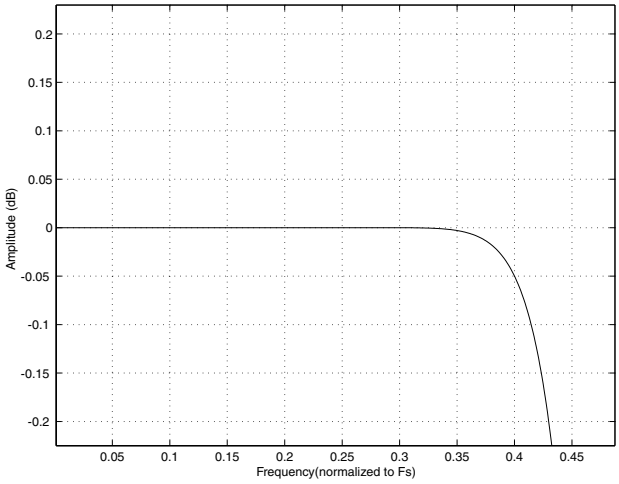


Figure 29. DAC Quad Speed Passband Ripple

APPENDIX B: ADC FILTER PLOTS

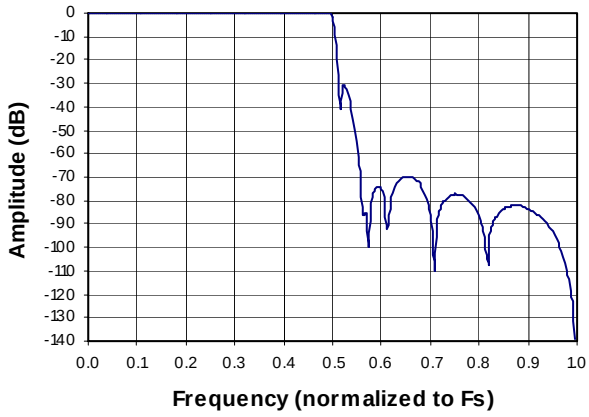


Figure 30. ADC Single Speed Stopband Rejection

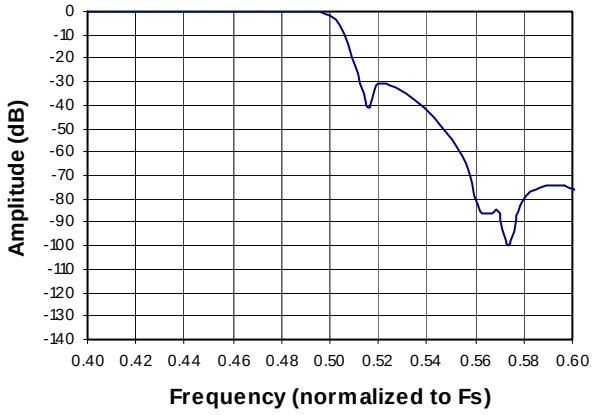


Figure 31. ADC Single Speed Stopband Rejection

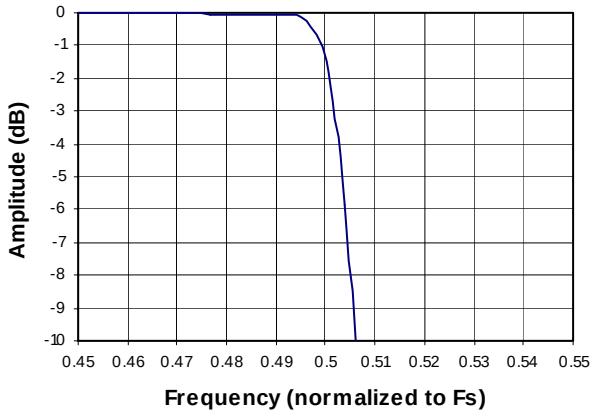


Figure 32. ADC Single Speed Transition Band (Detail)

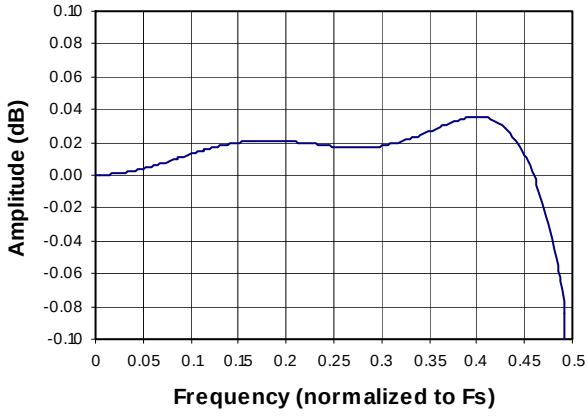


Figure 33. ADC Single Speed Passband Ripple

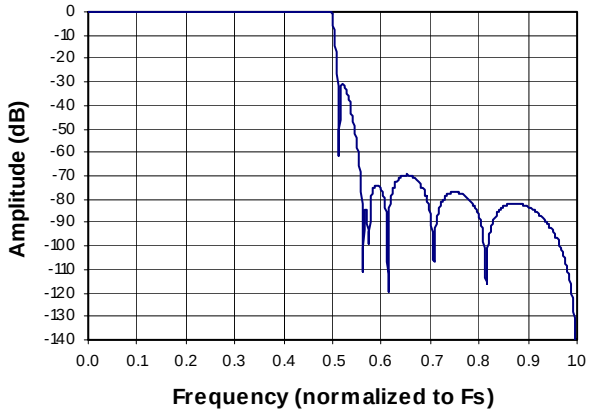


Figure 34. ADC Double Speed Stopband Rejection

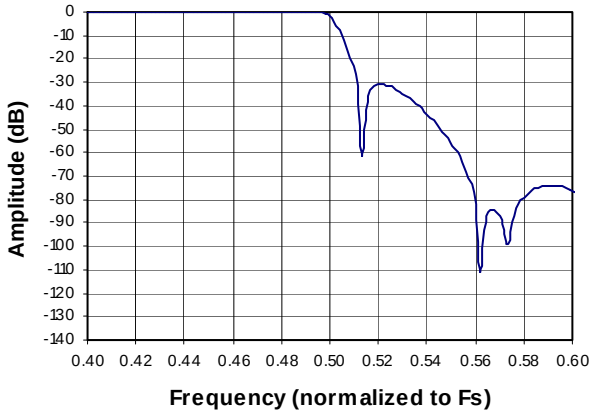


Figure 35. ADC Double Speed Stopband Rejection

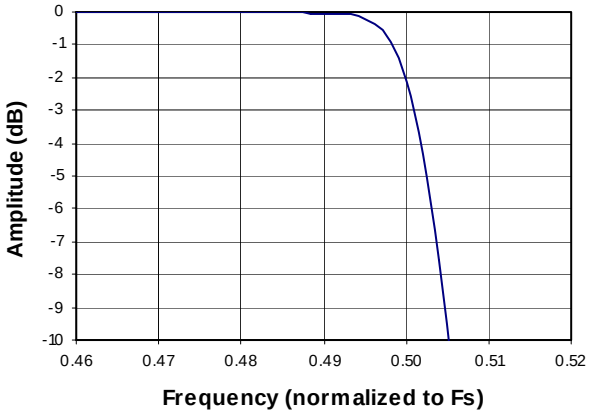


Figure 36. ADC Double Speed Transition Band (Detail)

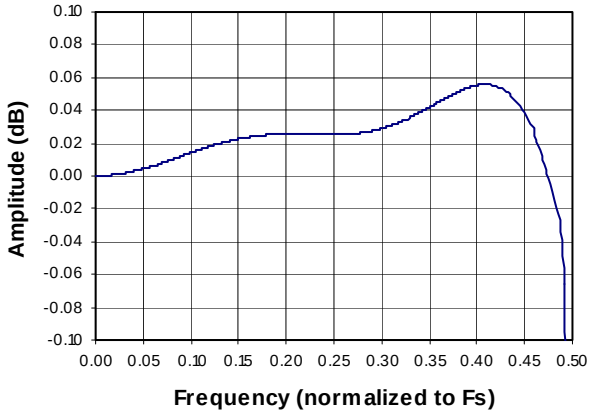


Figure 37. ADC Double Speed Passband Ripple

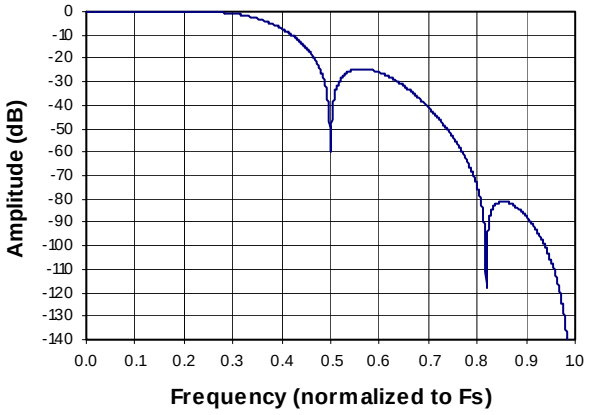


Figure 38. ADC Quad Speed Stopband Rejection

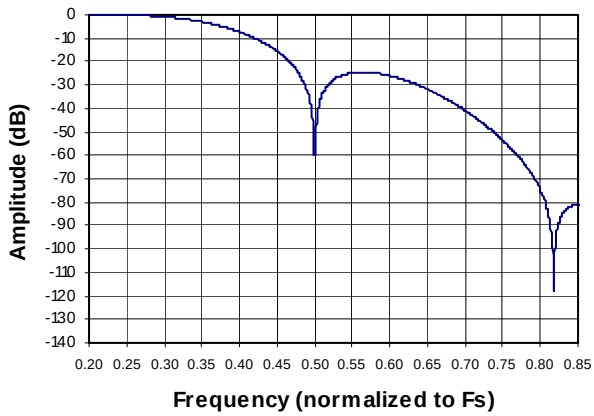


Figure 39. ADC Quad Speed Stopband Rejection

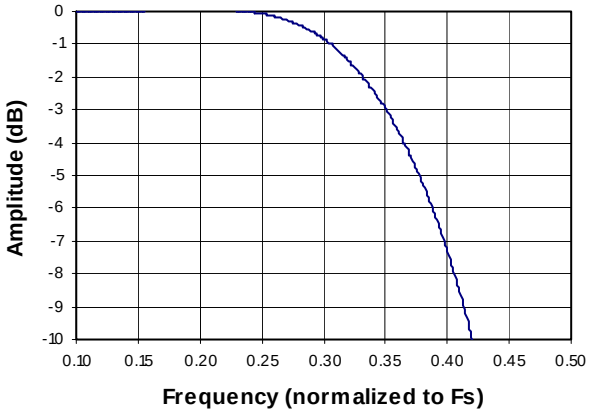


Figure 40. ADC Quad Speed Transition Band (Detail)

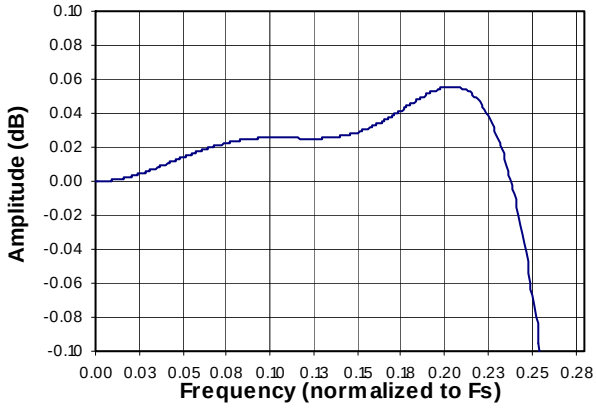


Figure 41. ADC Quad Speed Passband Ripple

APPENDIX C: EXTERNAL IEC60958-3 TRANSMITTER COMPONENTS

This section details the external components required to interface the IEC60958-3 transmitter to cables and fiber-optic components.

C.1 IEC60958-3 Transmitter External Components

The IEC60958-3 specifications call for an unbalanced drive circuit with an output impedance of 75 Ω ± 20% and a output drive level of 0.5 volts peak-to-peak ±20% when measured across a 75 Ω load using no cable. The circuit shown in Figure 42 provides the proper output impedance and drive level using standard 1% resistors. If VD is driven from +3.3 V, use resistor values of 243 Ω in place of the 374 Ω resistor and a 107 Ω resistor in place of the 90.9 Ω resistor. The standard connector for a consumer application is an RCA phono socket.

The TXOUT pin may be used to drive TTL or CMOS gates as shown in Figure 43. This circuit may be used for optical connectors for digital audio as they typically implement TTL or CMOS compatible inputs. This circuit is also useful when driving multiple digital audio outputs as RS422 line drivers typically implement TTL compatible inputs.

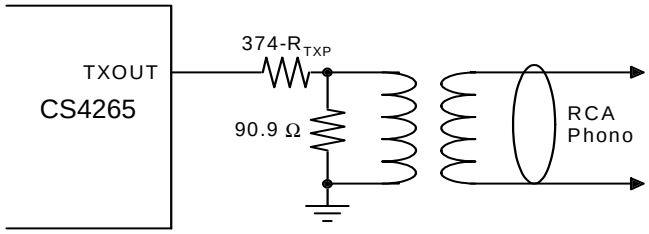


Figure 42. Consumer Output Circuit (VD = 5 V)

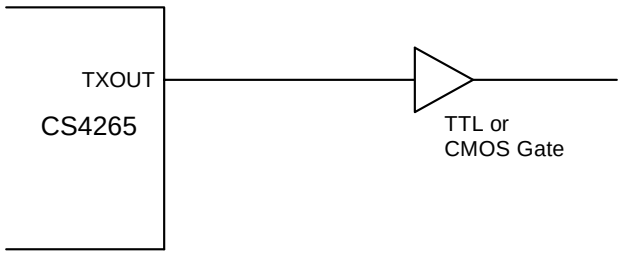


Figure 43. TTL/CMOS Output Circuit

C.2 Isolating Transformer Requirements

Please refer to the application note AN134: *AES and SPDIF Recommended Transformers* for resources on transformer selection.

APPENDIX D: CHANNEL STATUS BUFFER MANAGEMENT

The CS4265 has a comprehensive channel status (C) data buffering scheme which allows the user to manage the C data through the control port.

D.1 IEC60958-3 Channel Status (C) Bit Management

The CS4265 contains sufficient RAM to store a full block of C data for both A and B channels (192x2 = 384 bits). The user may read from or write to these RAM buffers through the control port.

The CS4265 manages the flow of channel status data at the block level, meaning that entire blocks of channel status information are buffered at the input, synchronized to the output time base, and then transmitted. The buffering scheme involves a cascade of 2 block-sized buffers, named E and F, as shown in Figure 44. The MSB of each byte represents the first bit in the serial C data stream. For example, the MSB of byte 0 (which is at control port address 13h) is the consumer/professional bit for channel status block A.

The E buffer is accessible from the control port, allowing read and writing of the C data. The F buffer is used as the source of C data for the IEC60958-3 transmitter. The F buffer accepts block transfers from the E buffer.

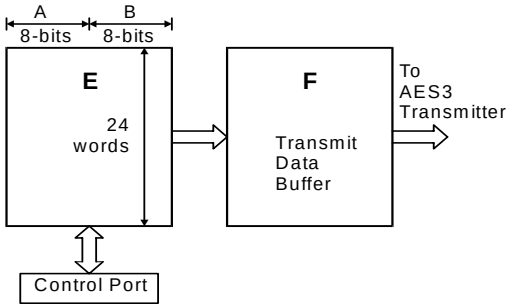


Figure 44. Channel Status Data Buffer Structure

D.1.1 Accessing the E buffer

The user can monitor the data being transferred by reading the E buffer, which is mapped into the register space of the CS4265, through the control port. The user can modify the data to be transmitted by writing to the E buffer.

The user can configure the status register such that EFTC bit is set whenever an E to F transfer completes. With this configuration in place, periodic polling of the status register allows determination of the time periods acceptable for E buffer interaction.

Also provided is an “E to F” inhibit bit. The “E to F” buffer transfer is disabled whenever the user sets this bit. This may be used whenever “long” control port interactions are occurring.

A flowchart for reading and writing to the E buffer is shown in Figure 45. For writing, the sequence starts after an E to F transfer, which is based on the output timebase.

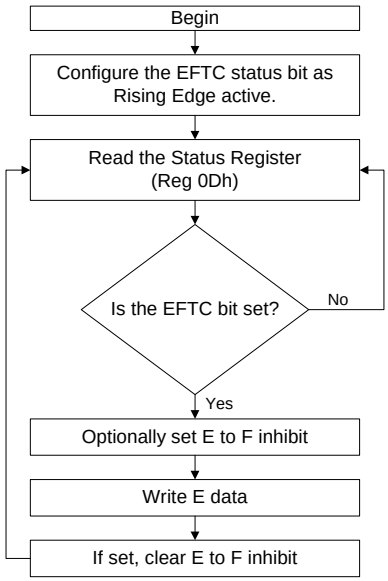


Figure 45. Flowchart for Writing the E Buffer

D.1.2 Serial Copy Management System (SCMS)

The CS4265 allows read/modify/write access to all the channel status bits. For consumer mode SCMS compliance, the host microcontroller needs to manipulate the Category Code, Copy bit and L bit appropriately.

D.1.3 Channel Status Data E Buffer Access

The E buffer is organized as 24 x 16-bit words. For each word the most significant byte is the A channel data, and the least significant byte is the B channel data (see Figure 44).

There are two methods of accessing this memory, known as one byte mode and two byte mode. The desired mode is selected through a control register bit.

D.1.3.1 One Byte mode

In many applications, the channel status blocks for the A and B channels will be identical. In this situation, if the user reads a byte from one of the channel's blocks, the corresponding byte for the other channel will be the same. Similarly, if the user wrote a byte to one channel's block, it would be necessary to write the same byte to the other block. One byte mode takes advantage of the often identical nature of A and B channel status data.

When reading data in one byte mode, a single byte is returned, which can be from channel A or B data, depending on a register control bit. If a write is being done, the CS4265 expects a single byte to be input to its control port. This byte will be written to both the A and B locations in the addressed word.

One byte mode saves the user substantial control port access time, as it effectively accesses 2 bytes worth of information in 1 byte's worth of access time. If the control port's auto increment addressing is used in combination with this mode, multi-byte accesses such as full-block reads or writes can be done especially efficiently.

D.1.3.2 Two Byte mode

There are those applications in which the A and B channel status blocks will not be the same, and the user is interested in accessing both blocks. In these situations, two byte mode should be used to access the E buffer.

In this mode, a read will cause the CS4265 to output two bytes from its control port. The first byte out will represent the A channel status data, and the 2nd byte will represent the B channel status data. Writing is similar, in that two

bytes must now be input to the CS4265's control port. The A channel status data is first, B channel status data second.

Release	Date	Changes
A1	May 2004	Initial Advance Release.
A2	September 2004	– Updated descriptions of pins 3, 4, 5, and 6 on page 5. – Removed specifications for SPI control port. – Added specification for AD0 selection in the I²C Control Port Description and Timing section on page 28. – Updated the typical connection diagram on page 21 to reflect the pin changes and AD0 selection method. – Added thermal pad to pin descriptions on page 6. – Added Package Considerations section on page 30. – Updated the Mic level input impedance specification on page 13.

Table 17. Revision History

Contacting Cirrus Logic Support

For all product questions and inquiries contact a Cirrus Logic Sales Representative.
To find the one nearest to you go to www.cirrus.com

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