Am29C861/Am29C863
Am29C961/Am29C963

High-Performance CMOS Bus Transceivers

DISTINCTIVE CHARACTERISTICS

- High-speed CMOS bidirectional bus transceivers
  - T-R delay = 7 ns typical
- Low standby power
- JEDEC FCT-compatible specs
- I_{OL} = 24 mA, Commercial and Military
- 200-mV typical hysteresis on data input ports
- Am29C900 DIP pinout option reduces lead inductance on V_{CC} and GND pins

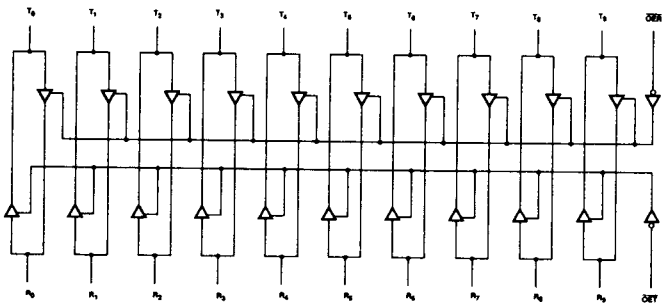
GENERAL DESCRIPTION

The Am29C861 and Am29C863 CMOS Bus Transceivers provide high-performance bus interface buffering for wide address/data paths or buses carrying parity. The Am29C861 is a 10-bit bidirectional transceiver; the Am29C863 is a 9-bit transceiver with NORed output enables for maximum control flexibility. Each device features data inputs with 200-mV typical input hysteresis to provide improved noise immunity. The Am29C861 and Am29C863 are produced with AMD's exclusive CS-11 CMOS process, and features a typical propagation delay of 7 ns, as well as an output current drive of 24 mA.

The Am29C861 and Am29C863 are available in the standard package options: DIPs, PLCCs, LCCs, SOICs, and Flatpacks. In addition, a DIP pinout option, featuring center V_{CC} and GND pins, reduces the lead inductance of the V_{CC} and GND pins. The ordering part numbers for CMOS transceivers with this pinout are the Am29C961 and Am29C963; their pinouts are shown later in this data sheet.

BLOCK DIAGRAMS

Am29C861



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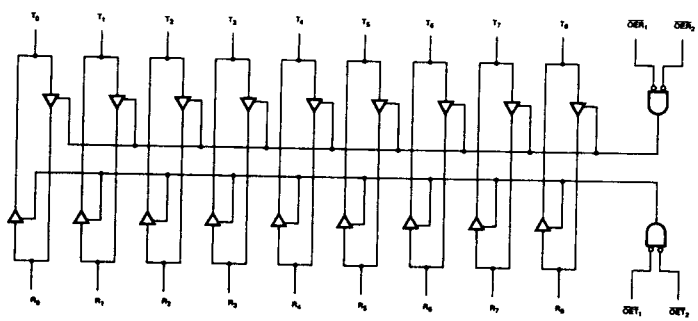
Am29C863

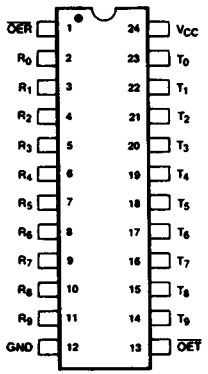


BD001070

CONNECTION DIAGRAMS
Top View

Am29C861

DIPs*



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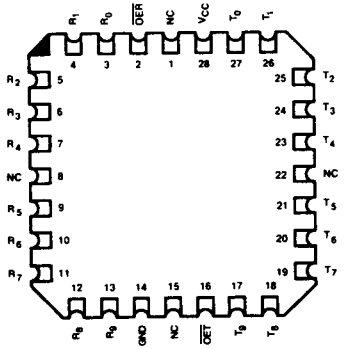

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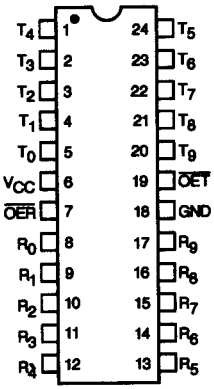
Am29C961

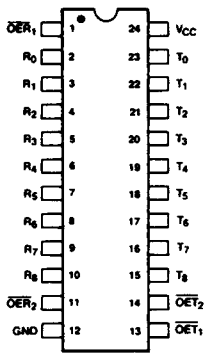
DIPs



CD010710

Am29C863

DIPs*



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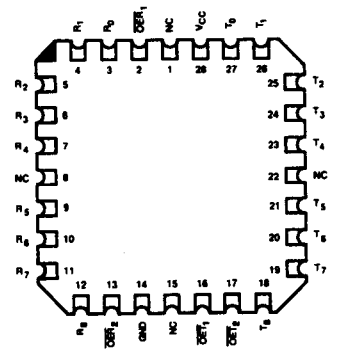
LCC**



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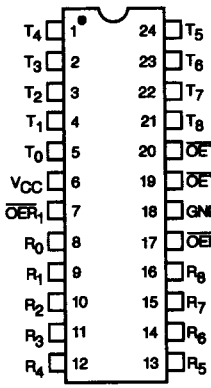
*Also available in 24-Pin Flatpack and Small Outline Package; pinout identical to DIPs.
**Also available in 28-Pin PLCC; pinout identical to LCC.

Am29C963

DIPs



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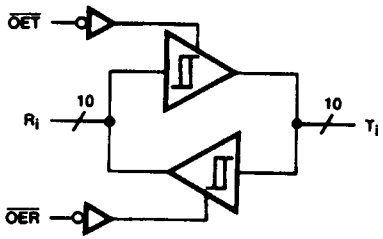
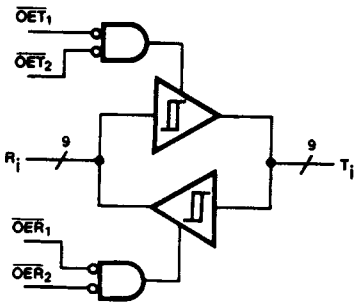
LOGIC SYMBOLS

Am29C861



LS000372

Am29C863



LS000382

FUNCTION TABLES

Am29C861

Inputs				Outputs		
$\overline{OET}$	$\overline{OER}$	R_I	T_I	R_I	T_I	Function
L	H	L	N/A	N/A	L	Transmit
L	H	H	N/A	N/A	H	Transmit
H	L	N/A	L	L	N/A	Receive
H	L	N/A	H	H	N/A	Receive
H	H	X	X	Z	Z	Hi-Z

Am29C863

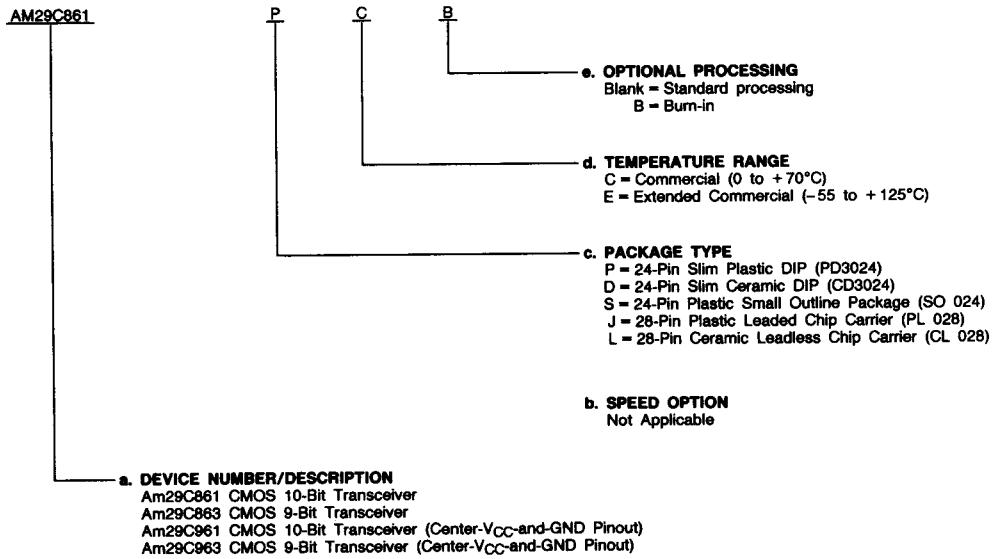
Inputs						Outputs		
$\overline{OET}_1$	$\overline{OET}_2$	$\overline{OER}_1$	$\overline{OER}_2$	R_I	T_I	R_I	T_I	Function
L	L	H	X	L	N/A	N/A	L	Transmit
L	L	X	H	L	N/A	N/A	L	Transmit
H	X	L	L	N/A	L	L	N/A	Receive
X	H	L	L	N/A	L	L	N/A	Receive
L	L	H	X	H	N/A	N/A	H	Transmit
L	L	X	H	H	N/A	N/A	H	Transmit
H	X	L	L	N/A	H	H	N/A	Receive
X	H	L	L	N/A	H	H	N/A	Receive
H	X	H	X	X	X	Z	Z	Hi-Z
X	H	X	H	X	X	Z	Z	Hi-Z

H = HIGH
L = LOW
Z = High Impedance

X = Don't Care
N/A = Not Applicable

ORDERING INFORMATION
Standard Products

AMD products are available in several packages and operating ranges. The order number (Valid Combination) is formed by a combination of: **a. Device Number**
b. Speed Option (if applicable)
c. Package Type
d. Temperature Range
e. Optional Processing



Valid Combinations	
AM29C861	PC, PCB, DC, DCB, DE, SC, JC, LC
AM29C863	
AM29C961	PC, PCB, DC, DCB, DE
AM29C963	

Valid Combinations

Valid Combinations list configurations planned to be supported in volume for this device. Consult the local AMD sales office to confirm availability of specific valid combinations, to check on newly released valid combinations, and to obtain additional data on AMD's standard military grade products.

ORDERING INFORMATION (Cont'd.)

APL Products

AMD products for Aerospace and Defense applications are available in several packages and operating ranges. APL (Approved Products List) products are fully compliant with MIL-STD-883C requirements. The order number (Valid Combination) for APL products is formed by a combination of: **a. Device Number**
b. Speed Option (if applicable)
c. Device Class
d. Package Type
e. Lead Finish

AM29C861 /B L A

e. LEAD FINISH
A = Hot Solder DIP

d. PACKAGE TYPE
L = 24-Pin Slim Ceramic DIP (CD3024)
K = 24-Pin Rectangular Medium Ceramic Flatpack (CFM024)
3 = 28-Pin Ceramic Leadless Chip Carrier (CL 028)

c. DEVICE CLASS
/B = Class B

b. SPEED OPTION
Not Applicable

a. DEVICE NUMBER/DESCRIPTION
Am29C861 CMOS 10-Bit Transceiver
Am29C863 CMOS 9-Bit Transceiver
Am29C961 CMOS 10-Bit Transceiver (Center-V_{CC}-and-GND Pinout)
Am29C963 CMOS 9-Bit Transceiver (Center-V_{CC}-and-GND Pinout)

Valid Combinations	
AM29C861	/BLA, /BKA, /B3A
AM29C863	
AM29C961	/BLA
AM29C963	

Valid Combinations

Valid Combinations list configurations planned to be supported in volume for this device. Consult the local AMD sales office to confirm availability of specific valid combinations or to check for newly released valid combinations.

Group A Tests

Group A tests consist of Subgroups 1, 2, 3, 7, 8, 9, 10, 11.

PIN DESCRIPTION

Am29C861

$\overline{OER}$ Output Enable-Receive (Input, Active LOW)
When LOW in conjunction with $\overline{OET}$ HIGH, the devices are in the Receive mode (R_i are outputs, T_i are inputs).

$\overline{OET}$ Output Enable-Transmit (Input, Active LOW)
When LOW in conjunction with $\overline{OER}$ HIGH, the devices are in the Transmit mode (R_i are inputs, T_i are output).

R_i Receive Port (Input/Output)
R_i are the 10-bit data inputs in the Transmit mode, and the outputs in the Receive mode.

T_i Transmit Port (Input/Output)
T_i are the 10-bit data outputs in the Transmit mode, and the inputs in the Receive mode.

Am29C863

$\overline{OER}_i$ Output Enables-Receive (Input, Active LOW)
When both $\overline{OER}_1$ and $\overline{OER}_2$ are LOW while $\overline{OET}_1$ or $\overline{OET}_2$ (or both) are HIGH, the device is in the Receive mode (R_i are outputs, T_i are inputs).

$\overline{OET}_i$ Output Enables-Transmit (Input, Active LOW)
When both $\overline{OET}_1$ and $\overline{OET}_2$ are LOW while $\overline{OER}_1$ or $\overline{OER}_2$ (or both) are HIGH, the device is in the Transmit mode (R_i are inputs, T_i are outputs).

R_i Receive Port (Input/Output)
R_i are the 9-bit data inputs in the Transmit mode, and the outputs in the Receive mode.

T_i Transmit Port (Input/Output)
T_i are the 9-bit data outputs in the Transmit mode, and the inputs in the Receive mode.

ABSOLUTE MAXIMUM RATINGS

Storage Temperature ..... −65 to +150°C
Supply Voltage to Ground Potential
Continuous ..... −0.5 V to +7.0 V
DC Output Voltage ..... −0.5 V to V_{CC} + 0.5 V
DC Input Voltage ..... −0.5 V to V_{CC} + 0.5 V
DC Output Diode Current: Into Output ..... +50 mA
Out of Output ..... −50 mA
DC Input Diode Current: Into Input ..... +20 mA
Out of Input ..... −20 mA
DC Output Current per Pin: I_{SINK} ..... +48 mA ($2 \times I_{OL}$)
I_{SOURCE} ..... −30 mA ($2 \times I_{OH}$)
Total DC Ground Current .($n \times I_{OL} + m \times I_{CCT}$) mA (Note 1)
Total DC V_{CC} Current .... ($n \times I_{OH} + m \times I_{CCT}$) mA (Note 1)

Stresses above those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent device failure. Functionality at or above these limits is not implied. Exposure to absolute maximum ratings for extended periods may affect device reliability.

OPERATING RANGES

Commercial (C) Devices
Temperature (T_A) ..... 0 to +70°C
Supply Voltage (V_{CC}) ..... +4.5 V to +5.5 V

Military (M) and Extended Commercial (E) Devices
Temperature (T_A) ..... −55 to +125°C
Supply Voltage (V_{CC}) ..... +4.5 V to +5.5 V

Operating ranges define those limits between which the functionality of the device is guaranteed.

DC CHARACTERISTICS over operating range unless otherwise specified (for APL Products, Group A, Subgroups 1, 2, 3 are tested unless otherwise noted)

Parameter Symbols	Parameter Description	Test Conditions			Min.	Max.	Units
V_{OH}	Output HIGH Voltage	V_{CC} = 4.5 V, V_{IN} = V_{IH} or V_{IL}	I_{OH} = −15 mA		2.4		Volts
V_{OL}	Output LOW Voltage	V_{CC} = 4.5 V, V_{IN} = V_{IH} or V_{IL}	I_{OL} = 24 mA			0.5	Volts
V_{IH}	Input HIGH Voltage	Guaranteed Input Logical HIGH Voltage for All Inputs (Note 2)			2.0		Volts
V_{IL}	Input LOW Voltage	Guaranteed Input Logical LOW Voltage for All Inputs (Note 2)				0.8	Volts
V_I	Input Clamp Voltage	V_{CC} = 4.5 V, I_{IN} = −18 mA				−1.2	Volts
I_{IL}	Input LOW Current	V_{CC} = 5.5 V Input Only	V_{IN} = 0.0 V			−10	µA
			V_{IN} = 0.4 V			−5	
I_{IH}	Input HIGH Current	V_{CC} = 5.5 V Input Only	V_{IN} = 2.7 V			5	µA
			V_{IN} = 5.5 V			10	
I_{OZH}	Output Off-State Current (High Impedance)	V_{CC} = 5.5 V I/O Port	V_{OUT} = 2.7 V			15	µA
			V_{OUT} = 5.5 V			20	
I_{OZL}		V_{CC} = 5.5 V I/O Port	V_{OUT} = 0.4 V			−15	µA
			V_{OUT} = 0.0 V			−20	
I_{SC}	Output Short-Circuit Current	V_{CC} = 5.5 V, V_O = 0 V (Note 3)			−60		mA
I_{CCQ}	Static Supply Current	V_{CC} = 5.5 V, Outputs Open	V_{IN} = V_{CC} or GND	MIL		160	µA
				COM'L		120	
I_{CCT}			V_{IN} = 3.4 V	Data Input		1.5	mA/Bit
				$\overline{OER_1}$, $\overline{OER_2}$, $\overline{OET_1}$, $\overline{OET_2}$		3.0	
I_{CCD}†	Dynamic Supply Current	V_{CC} = 5.5 V (Note 4)				400	µA/ MHz/Bit

Notes: 1. n = number of outputs, m = number of inputs.
2. Input thresholds are tested in combination with other DC parameters or by correlation.
3. Not more than one output shorted at a time. Duration should not exceed 100 milliseconds.
4. Measured at a frequency ⩽ 10 MHz with 50% duty cycle.

† Not included in Group A tests.

SWITCHING CHARACTERISTICS over operating range unless otherwise specified (for APL Products, Group A, Subgroups 9, 10, 11 are tested unless otherwise noted)

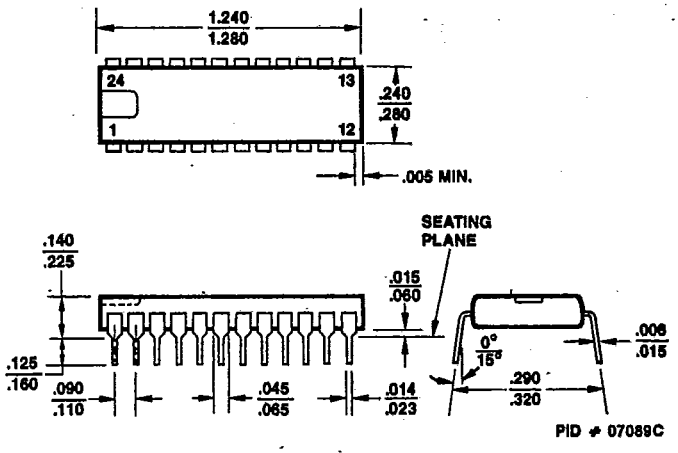
Parameter Symbol	Parameter Description	Test Conditions*	COMMERCIAL		MILITARY		Units
			Min.	Max.	Min.	Max.	
t_{PLH}	Propagation Delay from R_i to T_i or T_i to R_i Am29861A/Am29863A (Non-inverting)	C_L = 50 pF R_1 = 500 Ω R_2 = 500 Ω		10		12	ns
t_{PHL}				10		12	ns
t_{ZH}	Output Enable Time $\overline{OET}$ to T_i or $\overline{OER}$ to R_i			14		16	ns
t_{ZL}				14		16	ns
t_{HZ}	Output Disable Time $\overline{OET}$ to T_i or $\overline{OER}$ to R_i			14		16	ns
t_{LZ}				14		16	ns

*See Test Circuit and Waveforms.

PACKAGE OUTLINES*

T-90-20

PD3024



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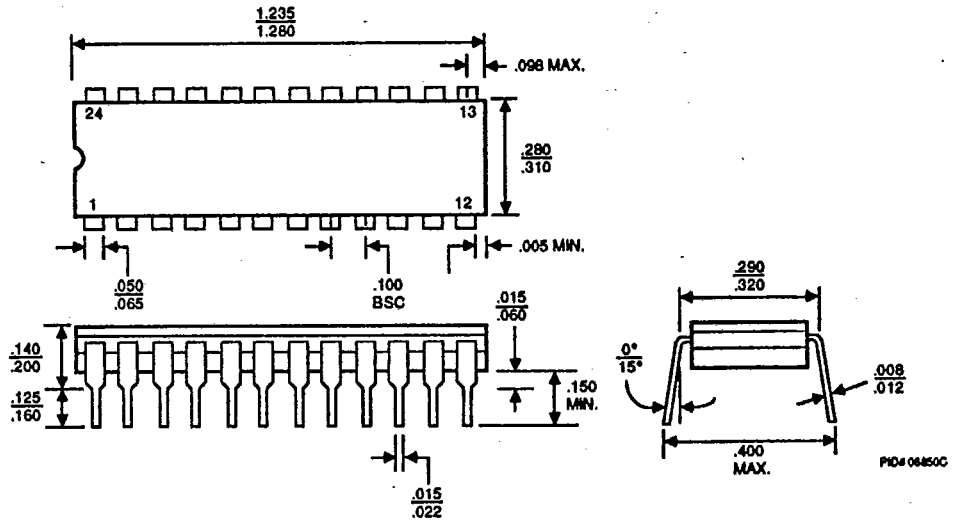
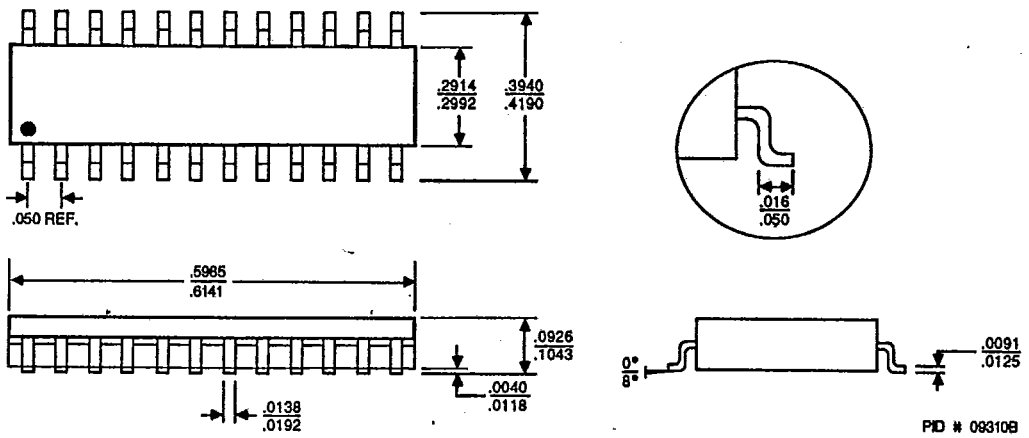


*For reference only.

PACKAGE OUTLINES (Cont'd.)

T-90-20

SO 024



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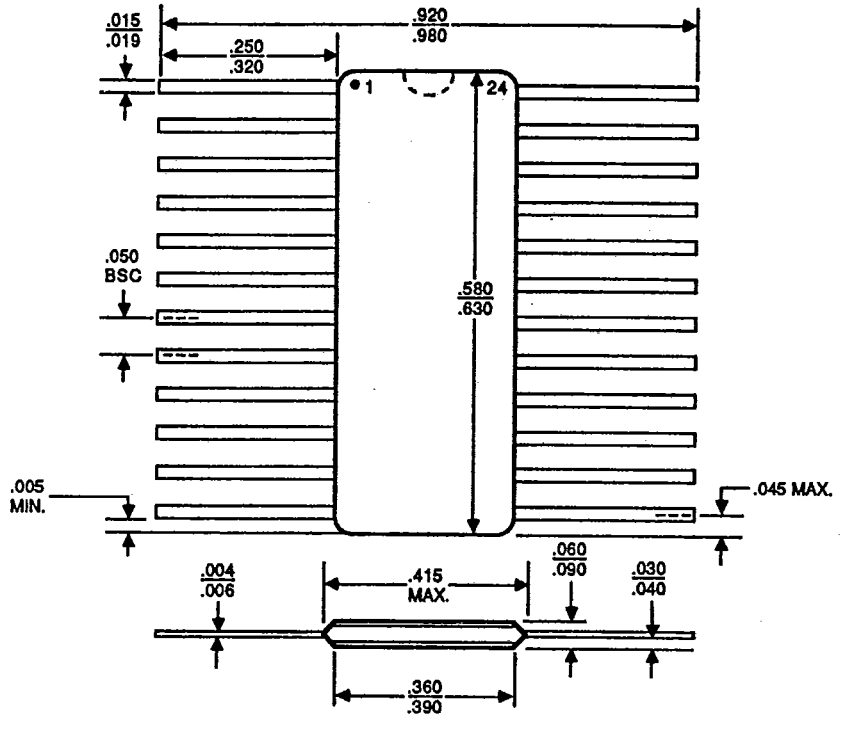

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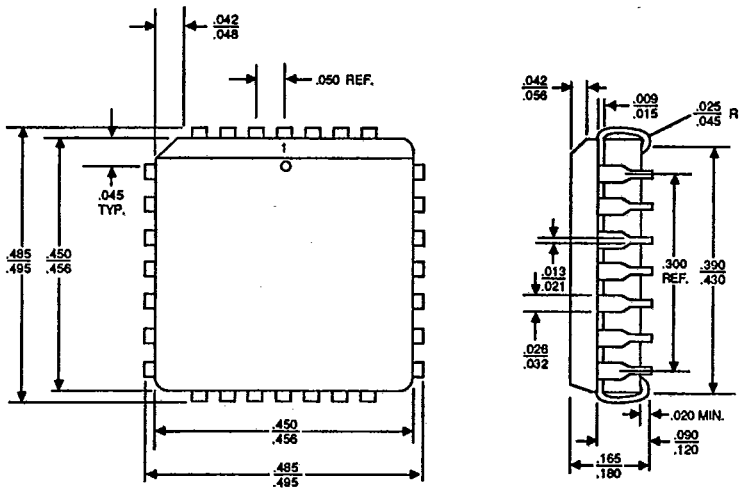
PACKAGE OUTLINES (Cont'd.)

T-90-20

PL 028



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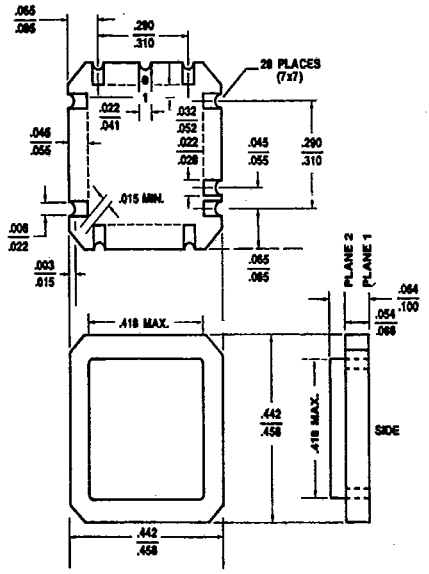

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