TDK SEMICONDUCTOR CORP.

78P2252
STM-1/OC-3 Transceiver

JUNE 2002

DESCRIPTION

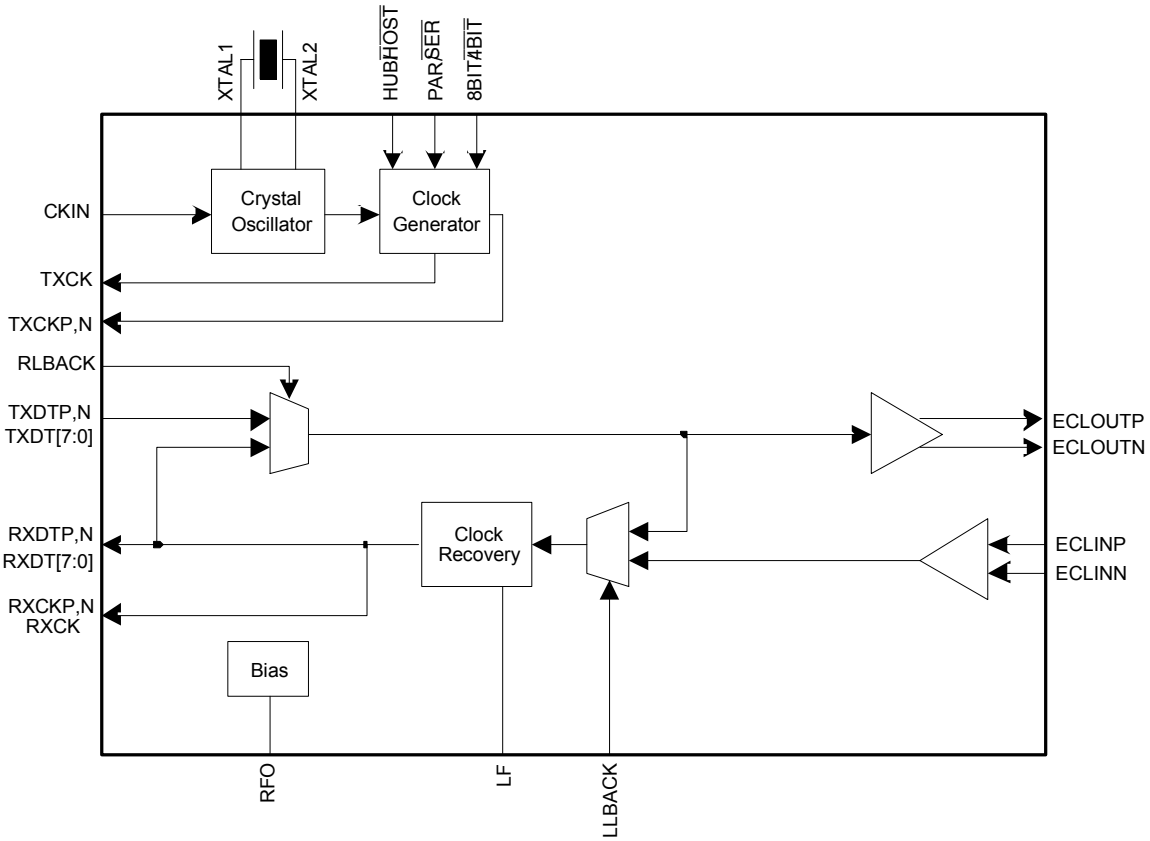
The 78P2252 is a transceiver IC designed for 155.52Mbit/s (OC-3 or STM-1) transmission. It is used at the interface to a fiber optic module. Interface to digital framer circuits is accomplished via a serial PECL or parallel CMOS interface.

The 78P2252 is built in a BiCMOS technology allowing for high performance with low power operation. The device automatically adjusts for operations with either a 3.3V or 5V power supply and is packaged in a 64-pin TQFP.

FEATURES

- **Compliant with ITU-T G.958 jitter tolerance, Telcordia TR-NWT-00253, ANSI T1.105.03-1994, and ANSI T1.105.05-1994**
- **Integrated Clock Recovery Unit (CRU)**
- **Serial PECL Interface**
- **Four and Eight bit Parallel CMOS Interfaces**
- **PECL Interfaces for connection to Fiber Optic Modules for SONET OC3 applications**
- **Integrated Clock Multiplier PLL**
- **Advanced BiCMOS Process**
- **Available in 64TQFP Package**

BLOCK DIAGRAM



FUNCTIONAL DESCRIPTION

The 78P2252 contains all the necessary transmit and receive circuitry for connection between 155.52Mbit/s signals and digital Framer/Deframer ICs.

DIGITAL INTERFACE

The digital interface of the 78P2252 can operate as a Serial PECL, 4-bit Parallel CMOS, or 8-bit Parallel CMOS interface. These modes are controlled by the PAR/$\overline{\text{SER}}$ and 8BIT/$\overline{\text{4BIT}}$ pins as shown in the following table.

Mode	PAR/$\overline{\text{SER}}$	8BIT/$\overline{\text{4BIT}}$	Data pins	Clock pins	Clock Frequency (MHz)
Serial	0	X	TXDTP,N RXDTP,N	TXCKP,N RXCKP,N	155.52
4-bit Parallel	1	0	TXDT[3:0] RXDT[3:0]	TXCK RXCK	38.88
8-bit Parallel	1	1	TXDT[7:0] RXDT[7:0]	TXCK RXCK	19.44

TRANSMITTER OPERATION

The transmitter accepts serial or parallel data and generates an NRZ coded PECL signal for transmission to a fiber optic module.

When set to serial mode via PAR/$\overline{\text{SER}}$ pin, serial data is input from the digital Framer/Deframer IC to the 78P2252 on the TXDTP and TXDTN pins at PECL levels. The data is clocked in with a line rate frequency clock generated by the 78P2252 on the TXCKP and TXCKN pins.

When set to parallel mode, parallel data is input from the digital Framer/Deframer IC to the 78P2252 on the TXDT[7:0] pins. Eight bits or four bits of data are used depending the setting of the 8BIT/$\overline{\text{4BIT}}$ pin.

- In eight bit parallel mode, data is read on pins TXDT[7:0].
- In four bit parallel mode, data is read on pins TXDT[3:0].

The parallel input data is clocked in with the generated clock output TXCK. The TXCK automatically adjusts to either one-eighth or one-fourth the standard line rate frequency, depending on the state of the 8BIT/$\overline{\text{4BIT}}$ pin.

RECEIVER OPERATION

The receiver accepts NRZ coded, serial data at 155.52Mbit/ from the fiber optic module via the ECL inputs, ECLINP and ECLINN. A clock signal is recovered using a low jitter PLL circuit.

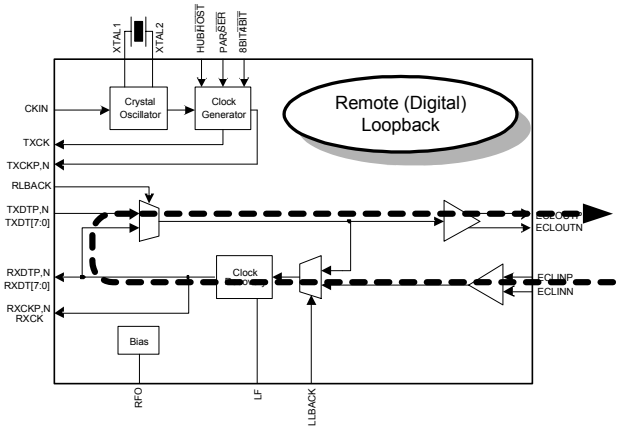
In serial mode, the received data is output on the RXDTP and RXDTN pins and the recovered clock is output on the RXCKP and RXCKN pins at the line rate frequency.

In parallel mode, the received data is converted to either eight bit or four bit parallel formats, determined by the state of the 8BIT/$\overline{\text{4BIT}}$ pin. The first bit received will arrive on the most significant output pin, RXDT[7] in eight bit mode and RXDT[3] in four bit mode. In parallel mode, the recovered clock in output on the RXCK pin at either one-eighth or one-fourth the line rate frequency, depending on the state of the 8BIT/$\overline{\text{4BIT}}$ pin.

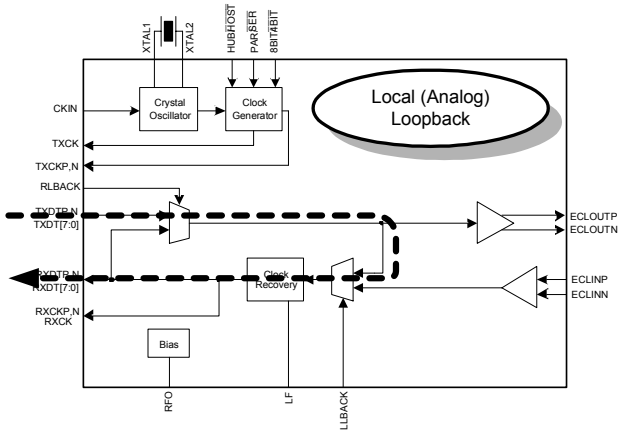
LOOPBACK OPERATION

Remote and Local Loopback modes in the 78P2252 are controlled by the RLBACK and LLBACK pins respectively.

When in Remote (Digital) Loopback mode (RLBACK logic high), the received data is internally routed onto the transmitter inputs. Note that any input data on the TXDTP,N pins or TXDT[7:0] pins is ignored in remote loopback mode.



When in Local (Analog) Loopback mode (LLBACK logic high), the transmit output signals are internally routed to the receiver inputs. Note that Local Loopback mode is disabled when HUB/$\overline{\text{HOST}}$ is low or RLBACK is high.

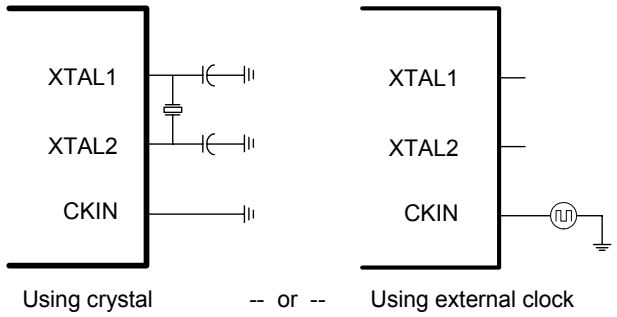


REFERENCE CLOCK

The HUB/$\overline{\text{HOST}}$ pin selects the source of the reference signal used for the internal transmit clock generator.

In Hub mode (HUB/$\overline{\text{HOST}}$ logic high), the transmit clock reference is derived from either a crystal oscillator applied to the XTAL1 and XTAL2 pins or a reference clock input applied at the CKIN pin. The reference frequency should be one-eighth the line rate frequency at 19.44MHz and should be applied in one of the following configurations.

Hub Mode Configurations



In Host mode (HUB/$\overline{\text{HOST}}$ logic low), the transmit clock reference is derived from the recovered receive clock. Note that the recovered receive clock is also used as the reference clock when Remote Loopback is enabled.

LLBACK	RLBACK	HUB/$\overline{\text{HOST}}$	Reference Clock
0	0	1	CKIN or XTAL1,2
1	0	1	CKIN or XTAL1,2
X	1	1	Recovered Rx Clock
X	X	0	Recovered Rx Clock

PIN DESCRIPTION

LEGEND

TYPE	DESCRIPTION	TYPE	DESCRIPTION
A	Analog Pin	PI	PECL Digital Input
CI	CMOS Digital Input	PO	PECL Digital Output
CO	CMOS Digital Output	S	Supply Pin

TRANSMIT PINS

NAME	PIN	TYPE	DESCRIPTION
TXDTP TXDTN	19 20	PI	Transmit Data Inputs - Serial Mode.
TXCKP TXCKN	22 23	PO	Transmit Clock Output - Serial Mode.
TXDT[7:0]	11-18	CI	Transmit Data Inputs – Parallel Mode. TXDT[7:4] are ignored in 4 bit mode.
TXCK	10	CO	Reference Clock Output – Serial mode. Transmit Clock Output – Parallel Mode.
ECLOUTP ECLOUTN	56 55	PO	Transmit Outputs.

RECEIVE PINS

NAME	PIN	TYPE	DESCRIPTION
ECLINP ECLINN	52 51	PI	Receiver inputs.
RXCKP RXCKN	25 26	PO	Recovered Receive Clock – Serial Mode.
RXCK	38	CO	Recovered Receive Clock – Parallel Mode.
RXDTP RXDTN	27 28	PO	Receive data – Serial Mode.
RXDT[7:0]	30-37	CO	Receive data – Parallel Mode. In 4 bit mode RXDT[3:0] are used and RXDT[7:4] are pulled low.

REFERENCE CLOCK PINS

NAME	PIN	TYPE	DESCRIPTION
XTAL1 XTAL2	5 6	A	Crystal Pins. These pins should be left floating if using reference clock input CKIN.
CKIN	9	CI	Reference clock input. This pin should be grounded if using the crystal oscillator inputs.

PIN DESCRIPTION (continued)

CONTROL AND STATUS PINS

NAME	PIN	TYPE	DESCRIPTION
RLBACK	41	CI	Remote (Digital) Loopback Enable. When logic high, loops receiver output data to transmitter inputs.
LLBACK	42	CI	Local (Analog) Loopback Enable. When logic high, loops transmitter output to receiver input. Note: Disabled when HUB/$\overline{\text{HOST}}$ is low or RLBACK is high.
HUB/$\overline{\text{HOST}}$	2	CI	In HUB mode (input high) the transmit reference clock is derived from the CKIN pin or the crystal oscillator. In HOST mode (input low) the transmit reference clock is derived from the recovered receive clock.
8BIT/$\overline{\text{4BIT}}$	63	CI	When in parallel mode, logic high selects 8-bit mode and logic low selects 4-bit mode. Ignored in serial mode.
PAR/$\overline{\text{SER}}$	62	CI	Selects parallel mode when high, serial mode when low.

ANALOG PINS

NAME	PIN	TYPE	DESCRIPTION
RFO	46	A	External reference resistor. See APPLICATION INFORMATION section for more info.
LF	44	A	PLL loop filter capacitor. See APPLICATION INFORMATION section for more info.

POWER SUPPLY PINS

It is recommended that all VCC pins be connected to a single power supply plane and all GND pins be connected to a single ground plane.

NAME	PIN	TYPE	DESCRIPTION
VCC	3, 8, 24, 40, 43, 53, 54, 57	S	Power Supply.
GND	1, 4, 7, 21, 29, 39, 45, 47, 48, 50, 58, 59, 60, 61, 64	S	Ground.

ELECTRICAL SPECIFICATIONS

ABSOLUTE MAXIMUM RATINGS

Operation beyond these limits may permanently damage the device.

PARAMETER	RATING
Supply Voltage	7 VDC
Storage Temperature	-65 to 150° C
Pin Voltage	-0.3 to (VCC+0.3) VDC
Pin Current	±100 mA

RECOMMENDED OPERATING CONDITIONS

Unless otherwise noted all specifications are valid over these temperatures and supply voltage ranges.

PARAMETER	RATING
DC Voltage Supply, VCC	3.3 ± 0.3 VDC; 5 ± 0.5 VDC
Ambient Operating Temperature	-40 to 85°C

DC CHARACTERISTICS:

PARAMETER	SYMBOL	CONDITIONS	MIN	NOM	MAX	UNIT
Supply Current (Parallel Mode)	Icc	Vcc = 3.3V Vcc = 5.0V		140 150	165 175	mA
Supply Current (Serial Mode)	Icc	Vcc = 3.3V Vcc = 5.0V		210 280	245 330	mA

ELECTRICAL SPECIFICATIONS (continued)

DIGITAL INPUT CHARACTERISTICS

Pins of type CI

PARAMETER	SYMBOL	CONDITIONS	MIN	NOM	MAX	UNIT
Input Voltage Low	Vil				Vcc/2 - 0.9	V
Input Voltage High	Vih		Vcc/2 + 0.9			V
Input Current	Iil, Iih		-10		10	µA
Input Capacitance	Cin			10		pF

Pins of type PI

PARAMETER	SYMBOL	CONDITIONS	MIN	NOM	MAX	UNIT
Input Voltage Low	Vil	Relative to Vcc			-1.5	V
Input Voltage High	Vih	Relative to Vcc	-1.1			V

DIGITAL OUTPUT CHARACTERISTICS

Pins of type CO

PARAMETER	SYMBOL	CONDITIONS	MIN	NOM	MAX	UNIT
Output Voltage Low	Vol			0.6	0.7	V
Output Voltage High	Voh	Below Vcc		0.6	0.7	V
Transition Time	Tt			3.5		ns

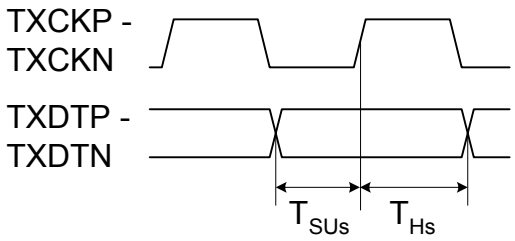
Pins of type PO

PARAMETER	SYMBOL	CONDITIONS	MIN	NOM	MAX	UNIT
Output Voltage Low	Vol	Vcc Reference biased at Vcc -1.5V with 50 ohm	-1.7	-1.4	-1.3	V
Output Voltage High	Voh	Vcc Reference biased at Vcc -1.5V with 50 ohm	-1.1	-0.9	-0.7	V
Rise Time	Tr			1	3	ns
Fall Time	Tf			1	3	ns

ELECTRICAL SPECIFICATIONS (continued)

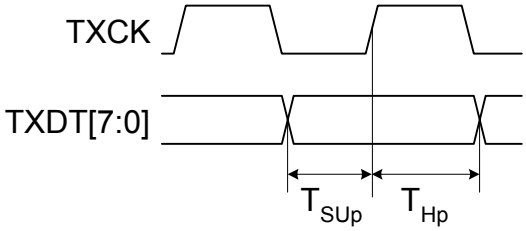
DIGITAL TIMING CHARACTERISTICS

Transmit Interface – Serial Mode



PARAMETER	SYMBOL	CONDITIONS	MIN	NOM	MAX	UNIT
Transmit Setup Time	T_{SUs}	Serial Mode	1.5			ns
Transmit Hold Time	T_{Hs}	Serial Mode	1.5			ns
TXCKP,N Duty Cycle			40		60	%

Transmit Interface – 8-bit Parallel Mode

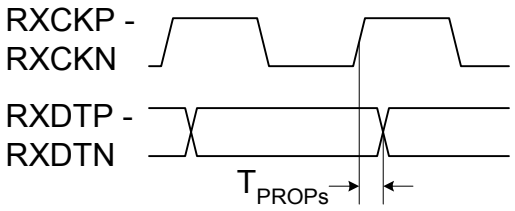


PARAMETER	SYMBOL	CONDITIONS	MIN	NOM	MAX	UNIT
Transmit Setup Time	T_{SUp}	Parallel Mode	3.5			ns
Transmit Hold Time	T_{Hp}	Parallel Mode	2.5			ns
TXCK Duty Cycle			40		60	%

ELECTRICAL SPECIFICATIONS (continued)

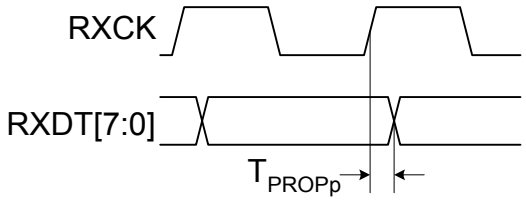
DIGITAL TIMING CHARACTERISTICS

Receive Interface – Serial Mode



PARAMETER	SYMBOL	CONDITIONS	MIN	NOM	MAX	UNIT
Receive Propagation Delay	T_{PROPs}	Serial Mode		2.4	3.0	ns
RXCKP,N Duty Cycle			40		60	%

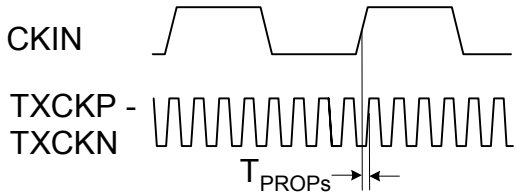
Receive Interface – 8-bit Parallel Mode



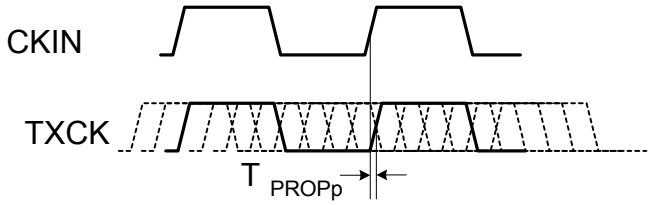
PARAMETER	SYMBOL	CONDITIONS	MIN	NOM	MAX	UNIT
Receive Propagation Delay	T_{PROPps}	Parallel Mode		4.0	6.0	ns
RXCKP,N Duty Cycle			40		60	%

ELECTRICAL SPECIFICATIONS (continued)

REFERENCE CLOCK INTERFACE



PARAMETER	SYMBOL	CONDITIONS	MIN	NOM	MAX	UNIT
CKIN to TXCKP/N Delay	T_{PROPs}	Serial Mode	3.1	4.6	5.6	ns

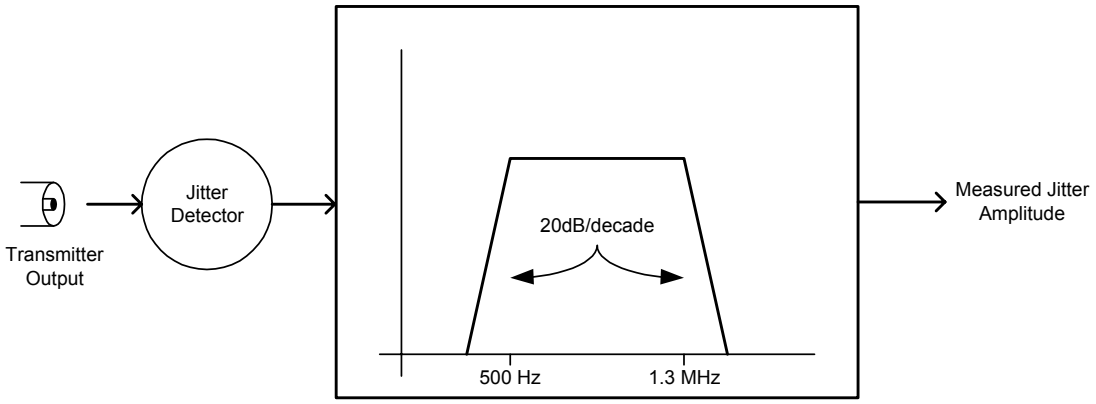


PARAMETER	SYMBOL	CONDITIONS	MIN	NOM	MAX	UNIT
CKIN to closes phase of TXCK Delay	T_{PROPp}	Parallel 8 bit Mode	1.6	3.7	5.7	ns

ELECTRICAL SPECIFICATIONS (continued)

TRANSMITTER OUTPUT JITTER

The transmit jitter specification ensures compliance with ITU-T G.958 and ANSI T1.105.03-1994 for STM-1 and OC-3 rates. The corner frequency of the transmit PLL is nominally 3.0 MHz.

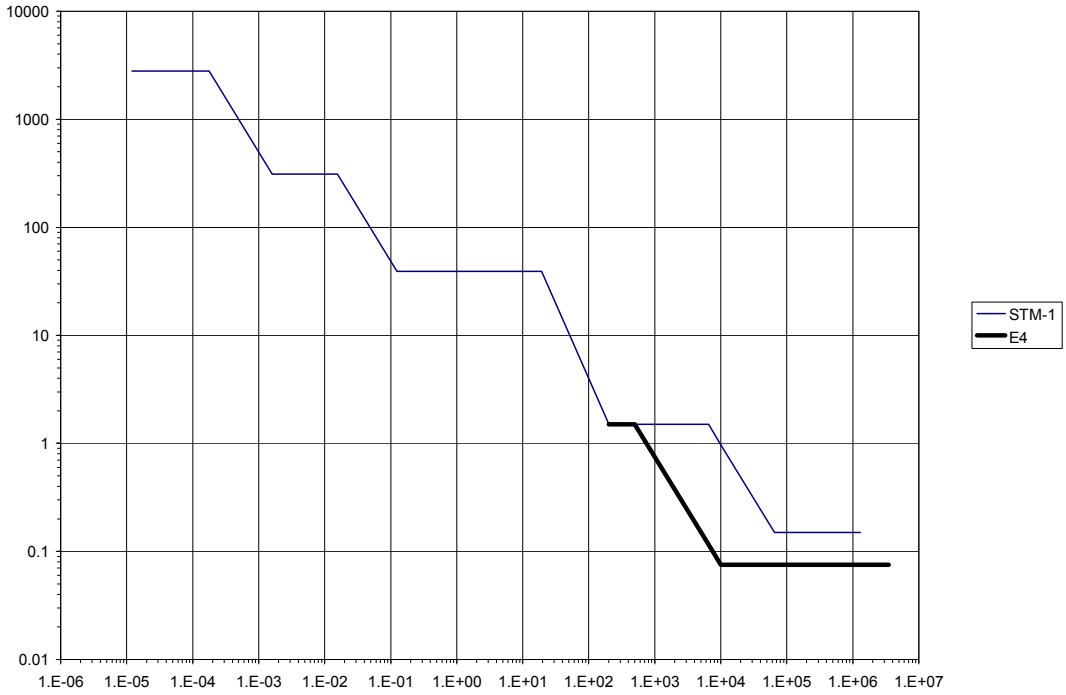


PARAMETER	CONDITION	MIN	NOM	MAX	UNIT
Transmitter Output Jitter	200 Hz to 3.5 MHz			0.075	UI_{pp}

ELECTRICAL SPECIFICATIONS (continued)

RECEIVER JITTER TOLERANCE

OC-3 jitter tolerance specifications are in ANSI T1.105.05-1994 and Telcordia TR-NWT-000253, Issue 2, Dec. 1991. STM-1 specifications are in ITU-T G.825. They are identical except that STM-1 specifies both jitter and wander. The STM-1 specification is the tightest and covers the largest frequency range.

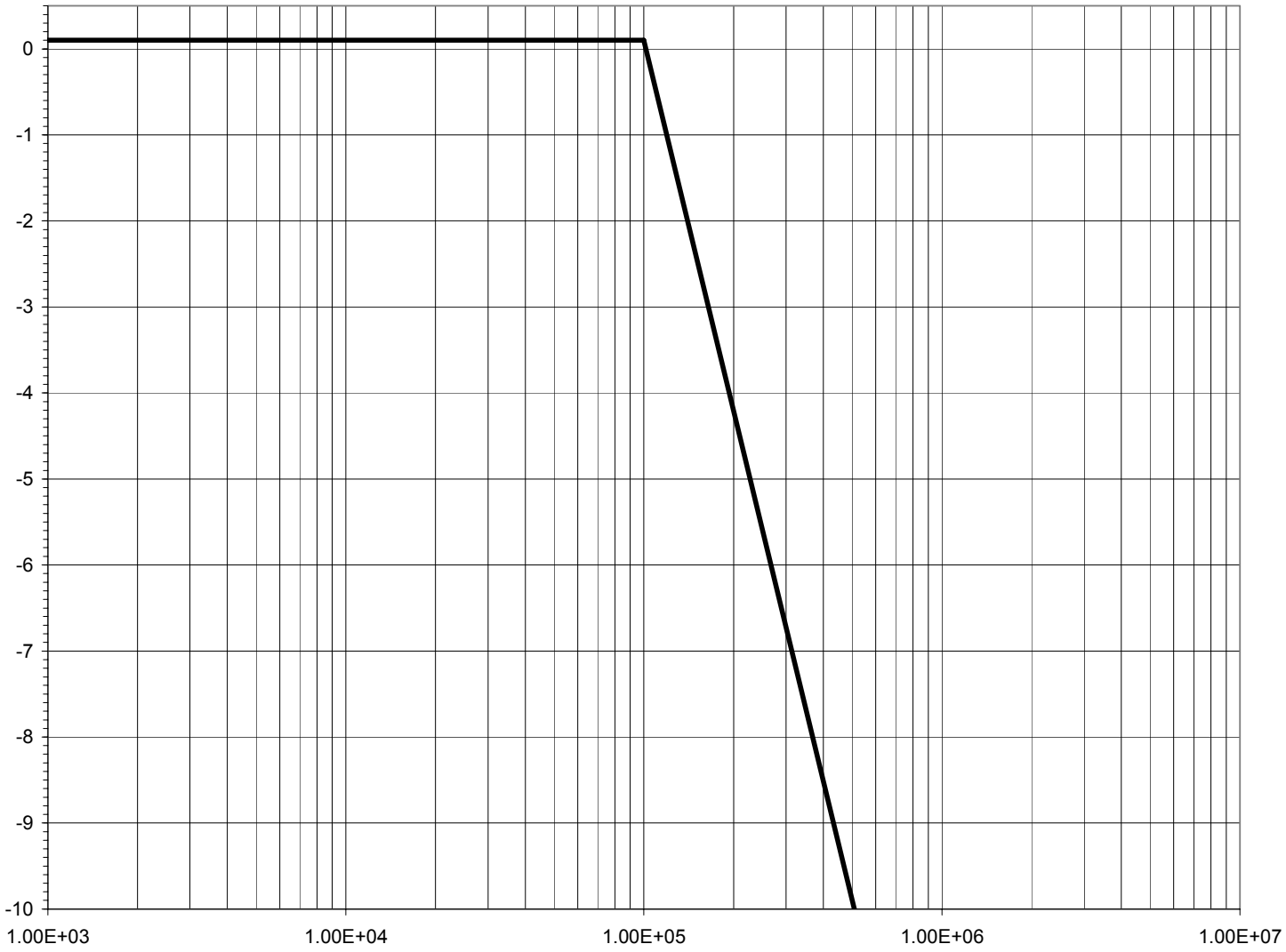


PARAMETER	CONDITION	MIN	NOM	MAX	UNIT
	12µHz to 178µHz	2800			
	1.6mHz to 15.6mHz	311			
Receiver Jitter Tolerance	125mHz to 19.3 Hz	39			UI
	500Hz to 6.5kHz	1.5			
Note 1: Not tested in production	65kHz to 3.5MHz	0.15			

ELECTRICAL SPECIFICATIONS (continued)

RECEIVER JITTER TRANSFER FUNCTION

The receiver clock recovery loop filter characteristics such that the receiver has the following transfer function. The corner frequency of the PLL is approximately 100 kHz. These specifications are not tested in production.



PARAMETER	CONDITION	MIN	NOM	MAX	UNIT
Receiver Jitter transfer function	below 100 kHz			0.1	dB
Jitter transfer function roll-off Note 1: Not tested in production			20		dB per decade

APPLICATION INFORMATION

EXTERNAL COMPONENTS:

COMPONENT	PIN(S)	VALUE	UNITS	TOLERANCE
Reference Resistor	RFO	31.6	kΩ	1%
Filter Capacitor	LF1	470	nF	5%

CRYSTAL SPECIFICATIONS:

COMPONENT	VALUE	UNITS	TOLERANCE
Center Frequency	19.44	MHz	+/- 20ppm
Load Capacitor – XTAL1 to ground; XTAL2 to ground ➢ Please check datasheet of crystal manufacturer for optimal load capacitor values.	27	pF	

SCHEMATICS

The latest typical application schematics are available in the form of Application Notes and/or Demo Board Manuals. Please contact TDK Semiconductor for more information.

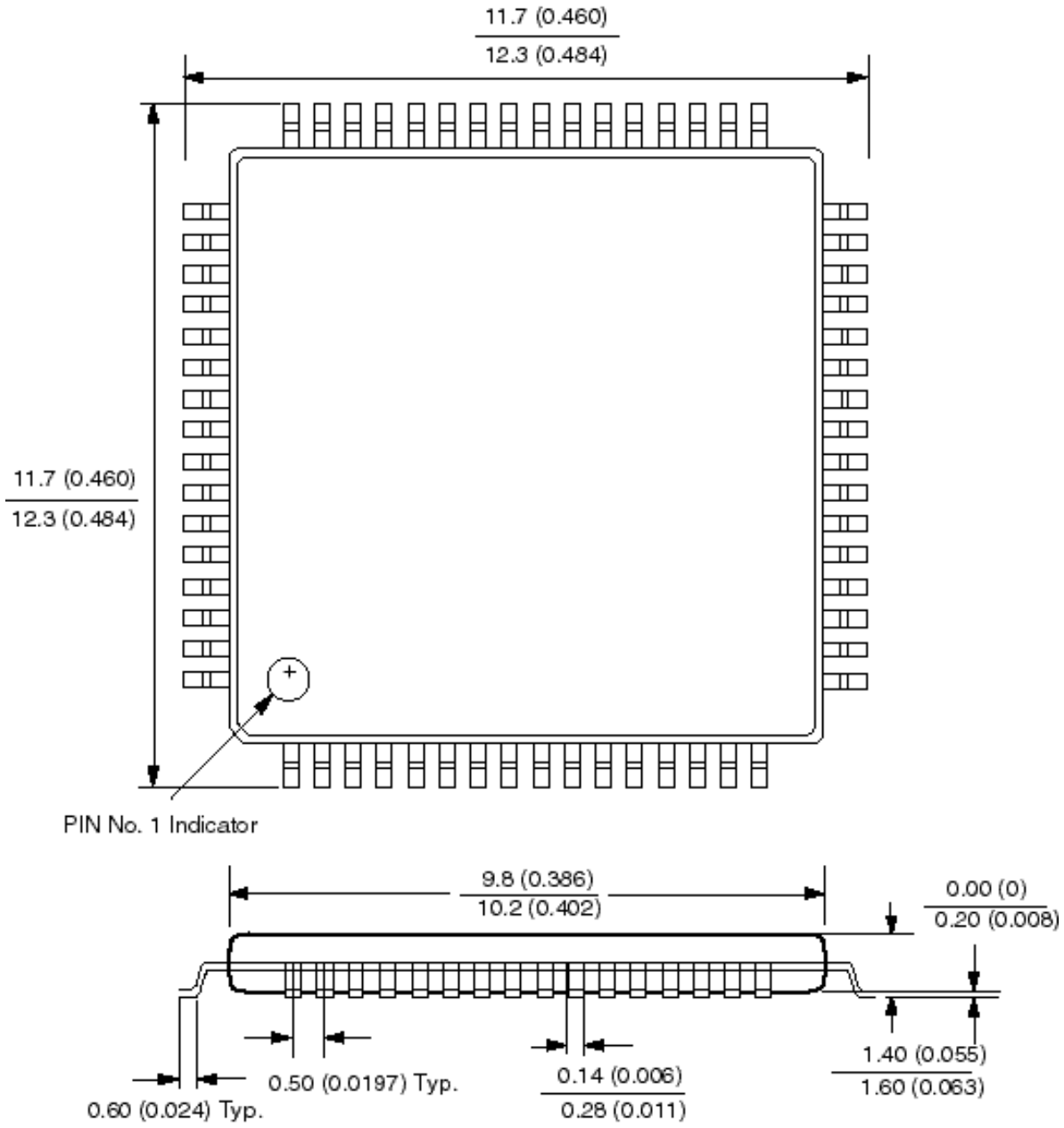
PECL INTERFACE COMPONENTS:

COMPONENT		VALUE	UNITS	TOLERANCE
Output Bias Resistor, R_{BIAS}	V_{CC} = 5v	250	Ω	5%
	V_{CC} = 3.3V	140	Ω	5%
Termination Resistor, R_{TERM}		100	Ω	5%

When the PECL signals travel one inch or less, lower power operation can be achieved by increasing R_{BIAS} and eliminating R_{TERM}.

FIGURE 1. PECL INTERFACE

MECHANICAL SPECIFICATIONS



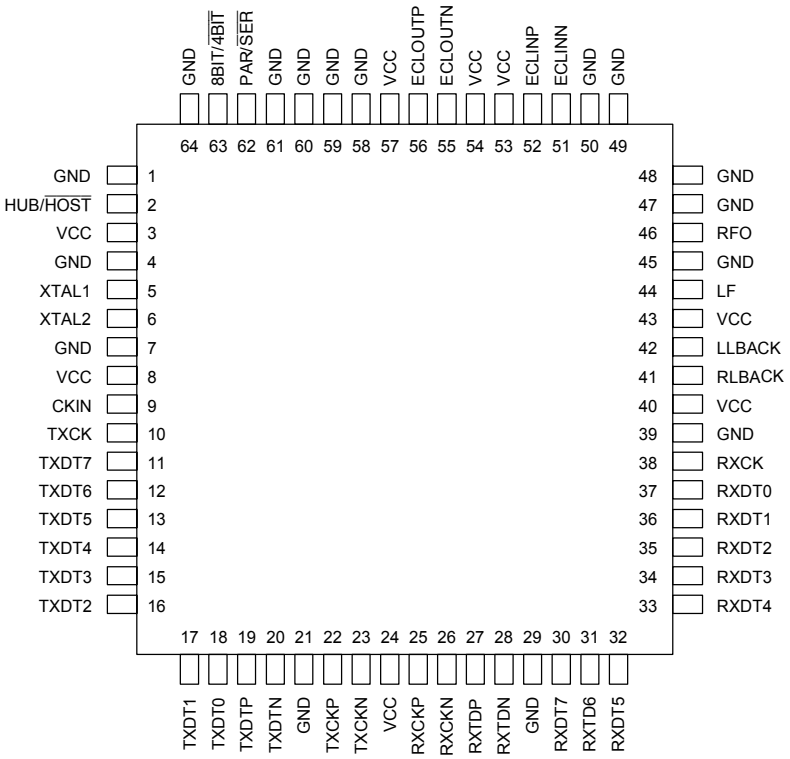
64-TQFP (JEDEC LQFP)

Mechanical Specification

PACKAGE PIN DESIGNATIONS

(Top View)

CAUTION: Use handling procedures necessary for a static sensitive component.



64-Pin TQFP (JEDEC LQFP)
78P2252-IGT

ORDERING INFORMATION

PART DESCRIPTION	ORDER NUMBER	PACKAGING MARK
78P2252 64- Pin Thin Quad Flatpack	78P2252-IGT	78P2252-IGT

TDK Semiconductor Corporation, 2642 Michelle Drive, Tustin, CA 92780-7019, (714) 508-8800, FAX: (714) 508-8877