

CMOS Programmable Electrically Erasable Logic Device

February 1993

Features

FPLA Architecture

- 12 Inputs and 10 I/Os
- Programmable-AND/OR arrays
- 42 Product Terms: 32 Logic Terms, 10 Control Terms
- 10 Sum Terms

Drop-In Replacement for PLS173

- Pin compatible
- JEDEC file compatible

Application Versatility

- Replaces random SSI/MSI logic
- Create customized comparators, multiplexers, encoders, converters, etc.

Advanced CMOS EEPROM Technology

Low Power Consumption

- 65mA + 1mA/MHz Max

High Performance

- tPD = 30ns Max, tOE = 30ns Max

EE Reprogrammability

- Superior programming
- Low-cost, "windowless" package
- Erases and programs in seconds

Development Support

- Third-party software and programmers
- AMI PEEL Development System with APEEL Logic Assembler

General Description

The AMI PEEL173 is a CMOS Programmable Electrically Erasable Logic device that provides a high-performance, low-power, reprogrammable, and architecturally enhanced alternative to conventional FPLAs. Designed in advanced CMOS EEPROM technology, the PEEL173 rivals speed parameters of comparable bipolar PLDs while providing a dramatic improvement in active power consumption. The EE reprogrammability of the PEEL173 reduces development and field retrofit costs and enhances testability to ensure 100% field programmability and function. PEEL technology allows for low-cost, "windowless" packaging in a ceramic or plastic 24-pin, 300-mil DIP.

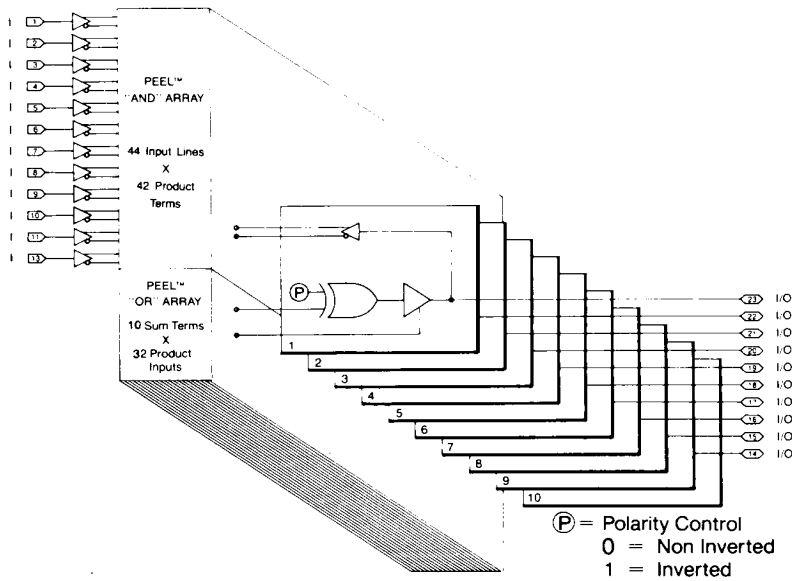
The PEEL173 provides both a programmable-AND array and a programmable OR array to offer drop-in compatibility with the bipolar PLS173. Applications for the PEEL173 cover a wide range of combinatorial functions, such as replacement of random SSI/MSI logic circuitry, priority encoders, comparators, parity generators, code converters, address decoders, and multiplexers. The PEEL173 is supported by popular development tools and programmers from third-party manufacturers, and by AMI's APEEL Logic Assembler.

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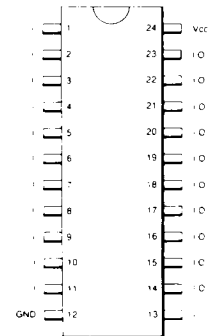
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Figure 32: PEEL173 Pin and Block Diagram

Block Diagram



Pin Configuration



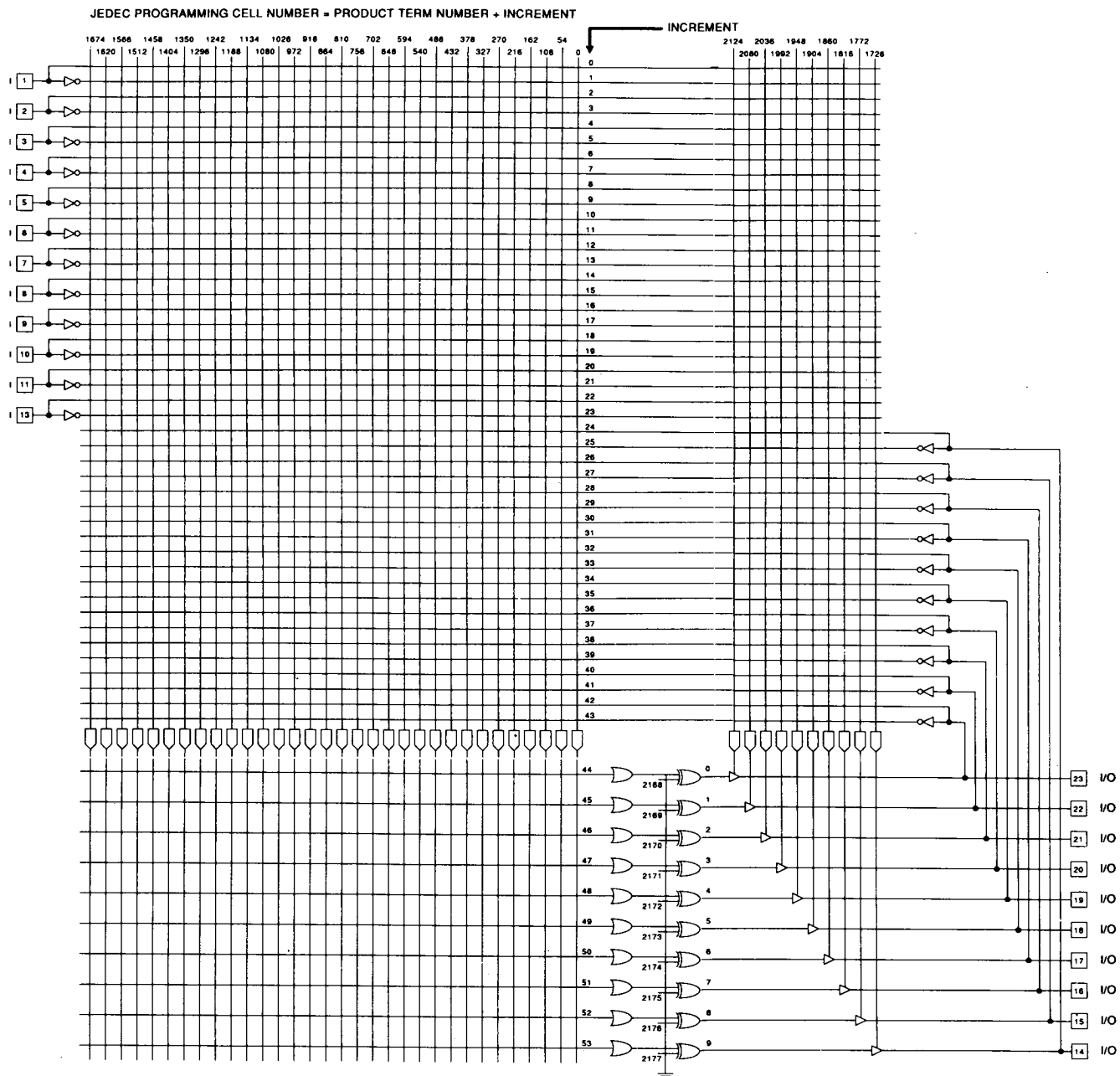
Pin Names

I = Input Only
I/O = Bi-Directional Input/Output
GND = Ground
Vcc = Power Supply (+5V)

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Figure 33: PEEL173 Logic Array Diagram



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Absolute Values

Absolute Maximum Ratings⁸

SYMBOL	PARAMETER	CONDITIONS	MIN	MAX	UNIT
V _{cc}	Supply Voltage	Relative to GND	-0.5	7.0	V
V _i	Voltage applied to Input ⁴	Relative to GND ^{1,10}	-0.5	V _{cc} +0.6	V
V _o	Voltage applied to Output	Relative to GND ¹	-0.5	V _{cc} +0.6	V
I _o	Output Current	Per pin (I _{ol} , I _{oh})		+25	mA
T _{st}	Storage Temperature		-65	+150	C
T _{lt}	Lead Temperature	(soldering 10 seconds)		+300	C

Operating Ranges

SYMBOL	PARAMETER	CONDITIONS	MIN	MAX	UNIT
V _{cc}	Supply Voltage	Commercial	4.75	5.25	V
		Industrial	4.5	5.5	V
T _a	Operating Temperature	Commercial	0	+70	C
		Industrial	-40	+85	C
T _r	Clock Rise Time ⁵	Test points at 10% and 90% levels		250	ns
T _f	Clock Fall Time ⁵	Test points at 10% and 90% levels		250	ns
T _{rvcc}	V _{cc} Rise Time ⁵	Test points at 10% and 90% levels		250	ms

DC Characteristics (Over Operating Range Specifications)

SYMBOL	PARAMETER	CONDITIONS	MIN	TYP	MAX	UNIT
I _{il}	Input Leakage	V _{in} = GND to V _{cc}			±10	μA
I _{oz}	Output Leakage	I/O = High Impedance V _o = GND to V _{cc}			±10	μA
V _{il}	Input Low Voltage		-0.3		0.8	V
V _{ih}	Input High Voltage		2.0		V _{cc} +0.3	V
V _{ol}	Output Low Voltage TTL	I _{ol} = +8.0mA ¹²			0.45	V
V _{olc}	Output Low Voltage CMOS	I _{ol} = 10μA ¹²			0.1	V
V _{oh}	Output High Voltage TTL	I _{oh} = -4.0mA ¹²	2.4			V
V _{ohc}	Output High Voltage CMOS	I _{oh} = -10μA ¹²	V _{cc} -0.1			V

Capacitance

SYMBOL	PARAMETER	CONDITIONS	MIN	TYP	MAX	UNIT
C _{in} ^{3,7}	Input Capacitance	Frequency = 1MHz		4	6	pF
C _{out} ^{3,7}	Output Capacitance	Frequency = 1MHz		8	12	pF
C _{clk} ^{3,7}	Clk Pin Capacitance	Frequency = 1MHz		8	13	pF

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Electrical Characteristics (Over Operating Range Specifications)

SYMBOL	PARAMETER	UNITS	MIN	MAX
I _{ccs}	V _{cc} Current Standby ⁹	mA		65
I _{cca}	V _{cc} Current Active ⁹	mA		I _{ccs} + 0.5 mA/MHz
t _{PD}	Input ⁴ to combinatorial output	ns		30
t _{OD}	Input ⁴ to output disable ¹¹	ns		30
t _{OE}	Input ⁴ to output enable ¹¹	ns		30

NOTES:

1. Minimum DC input is -0.5V; however, inputs may undershoot to -2.0V for periods less than 30ns.
2. Voltage applied to input or output must not exceed V_{cc}+1.0V.
3. These measurements are periodically sample tested.
4. "Input" refers to an Input signal.
5. Test points assume signal transitions of 5ns or less from the 10% and 90% points, and timing reference levels of 1.5V (unless otherwise specified).
6. See AC test point/load circuit table for t_{OE} and t_{OD} testing.
7. Typical values and capacitance are measured at V_{cc}=5.0V and T_a = 25°C.
8. Exposure to absolute maximum ratings over extended periods of time may affect device reliability. Exceeding absolute maximum ratings may cause permanent damage.
9. I/O pins are open (no load).
10. V_{in} specified is not for program/verify operation. Contact AMI for information regarding PEEL program/verify specifications.
11. t_{OD} and t_{OE} are measured at V_{oh}=-0.1V and V_{ol}=+0.1V.
12. Contact factory for increased Iol requirements.

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Figure 34: PEEL173 AC Switching Waveforms

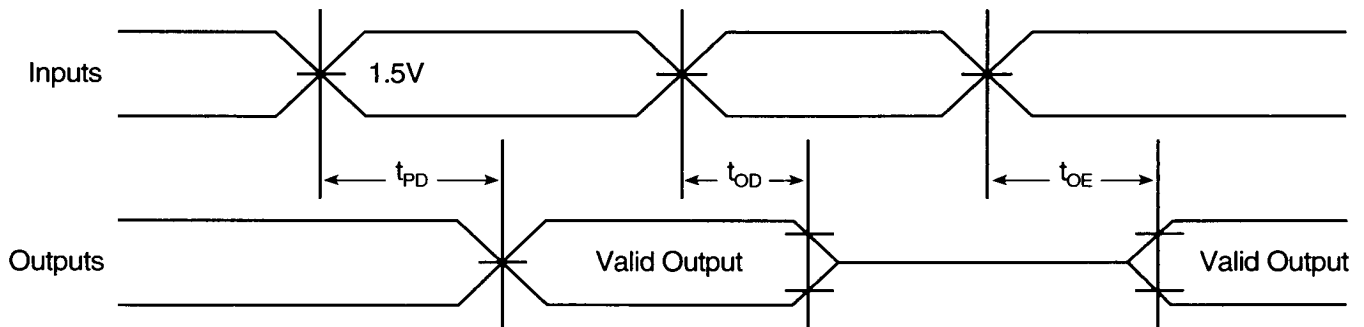


Figure 35: PEEL173 AC Test Loads

