FAST 74F583
4-Bit BCD Adder

FAST Products

Product Specification

FEATURES

- **Adds two decimal numbers**
- **Full internal look-ahead**
- **Fast ripple carry for economical expansion**
- **Sum output delay 19.5ns max**
- **Ripple carry delay 8.5ns max**
- **Input to ripple delay 13.0ns max**
- **Supply current 60mA max**

TYPE	TYPICAL PROPAGATION DELAY	TYPICAL SUPPLY CURRENT (TOTAL)
74F583	9.0ns	45mA

ORDERING INFORMATION

PACKAGES	COMMERCIAL RANGE V_{CC} = 5V±10%; T_A = 0°C to +70°C
16-Pin Plastic DIP	N74F583N
16-Pin Plastic SO	N74F583D

DESCRIPTION

The 74F583 4-bit coded (BCD) full adder performs the addition of two decimal numbers (A_0 - A_3, B_0 - B_3). The look ahead generates BCD carry terms internally, allowing the 'F583 to then do BCD addition correctly. For BCD numbers 0 through 9 at A and B inputs, the BCD sum forms at the output.

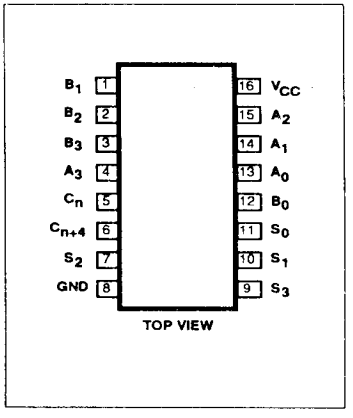
In addition of two BCD numbers totalling a number greater than 9, a valid BCD number and carry will result. For input values larger than 9, the number is converted from binary to BCD. Binary to BCD conversion occurs by grounding one set of inputs, A_n or B_n and applying a 4-bit binary number to the other set of inputs. If the input is between 0 and 9, a BCD number occurs at the output. If the binary input falls between 10 and 15, a carry term is generated. Both the carry term and the sum are the BCD equivalent of the binary input. Converting binary numbers greater than 16 may be achieved by cascading 'F583s.

INPUT AND OUTPUT LOADING AND FAN-OUT TABLE

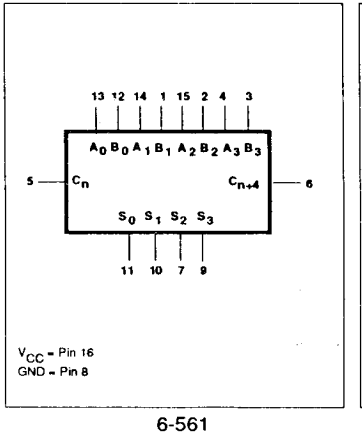
PINS	DESCRIPTION	74F(U.L.) HIGH/LOW	LOAD VALUE HIGH/LOW
A_0 - A_3	A operand inputs	1.0/2.0	20µA/1.2mA
B_0 - B_3	B operand inputs	1.0/2.0	20µA/1.2mA
C_n	Carry input	1.0/1.0	20µA/0.6mA
C_{n+4}	Carry output	50/33	1.0mA/20mA
S_0 - S_3	Sum outputs	50/33	1.0mA/20mA

NOTE:
One (1.0) FAST Unit Load is defined as: 20µA in the High state and 0.6mA in the Low state.

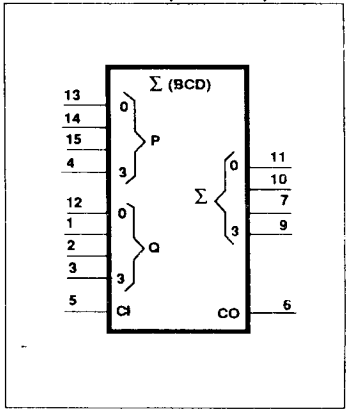
PIN CONFIGURATION



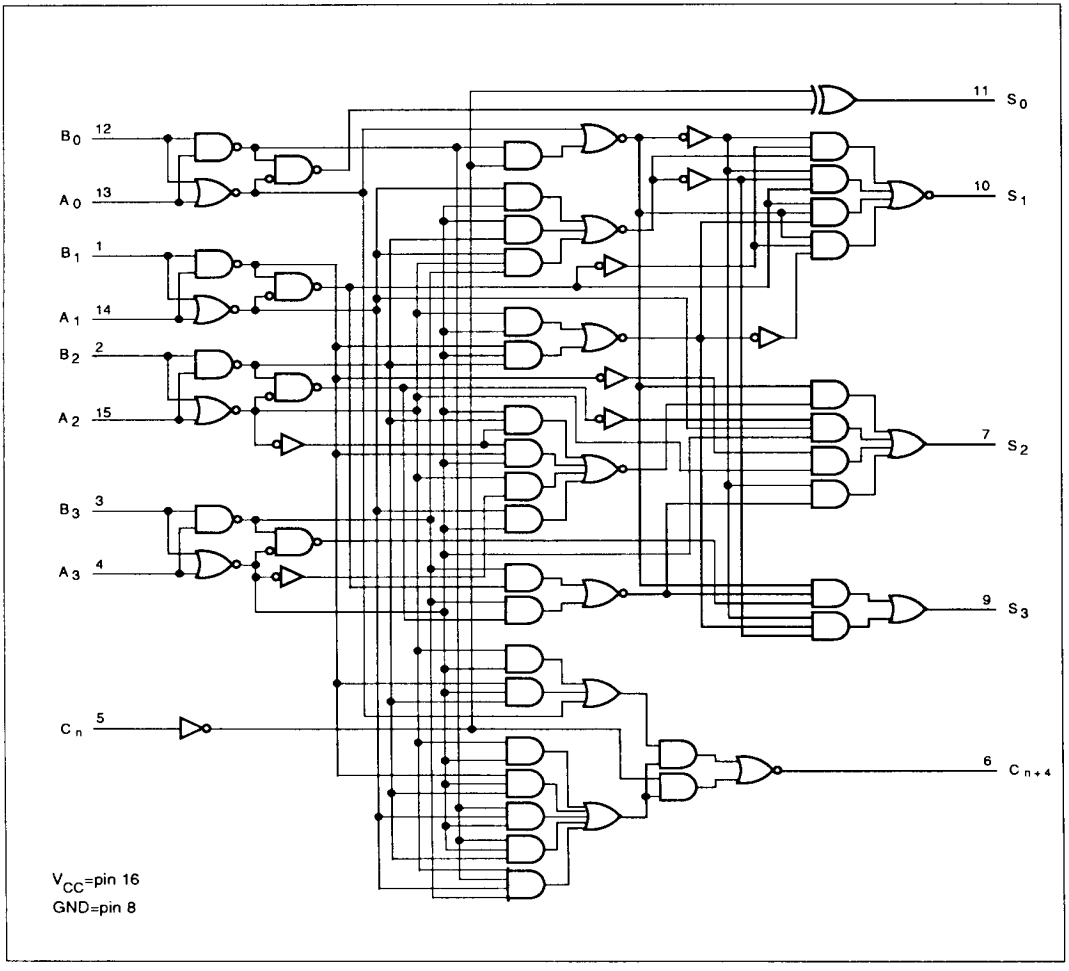
LOGIC SYMBOL



LOGIC SYMBOL(IEEE/IEC)



LOGIC DIAGRAM



ABSOLUTE MAXIMUM RATINGS

(Operation beyond the limits set forth in this table may impair the useful life of the device. Unless otherwise noted these limits are over the operating free-air temperature range.)

SYMBOL	PARAMETER	RATING	UNIT
V_{CC}	Supply voltage	-0.5 to +7.0	V
V_{IN}	Input voltage	-0.5 to +7.0	V
I_{IN}	Input current	-30 to +5	mA
V_{OUT}	Voltage applied to output in High output state	-0.5 to +V_{CC}	V
I_{OUT}	Current applied to output in Low output state	40	mA
T_A	Operating free-air temperature range	0 to +70	°C
T_{STG}	Storage temperature	-65 to +150	°C

RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER	LIMITS			UNIT
		Min	Nom	Max	
V_{CC}	Supply voltage	4.5	5.0	5.5	V
V_{IH}	High-level input voltage	2.0			V
V_{IL}	Low-level input voltage			0.8	V
I_{IK}	Input clamp current			-18	mA
I_{OH}	High-level output current			-1	mA
I_{OL}	Low-level output current			20	mA
T_A	Operating free-air temperature range	0		70	°C

DC ELECTRICAL CHARACTERISTICS

(Over recommended operating free-air temperature range unless otherwise noted.)

SYMBOL	PARAMETER		TEST CONDITIONS[1]		LIMITS			UNIT
					Min	Typ[2]	Max	
V_{OH}	High-level output voltage		V_{CC} = MIN, V_{IL} = MAX	±10%V_{CC}	2.5			V
			V_{IH} = MIN, I_{OH} = MAX	±5%V_{CC}	2.7	3.4		V
V_{OL}	Low-level output voltage		V_{CC} = MIN, V_{IL} = MAX	±10%V_{CC}		0.30	0.50	V
			V_{IH} = MIN, I_{OL} = MAX	±5%V_{CC}		0.30	0.50	V
V_{IK}	Input clamp voltage		V_{CC} = MIN, I_I = I_{IK}			-0.73	-1.2	V
I_I	Input current at maximum input voltage		V_{CC} = MAX, V_I = 7.0V				100	µA
I_{IH}	High-level input current		V_{CC} = MAX, V_I = 2.7V				20	µA
I_{IL}	Low-level input current	C_n only	V_{CC} = MAX, V_I = 0.5V				-0.6	mA
		A_n & B_n					-1.2	mA
I_{OS}	Short circuit output current[3]		V_{CC} = MAX		-60		-150	mA
I_{CC}	Supply current (total)		V_{CC} = MAX			45	60	mA

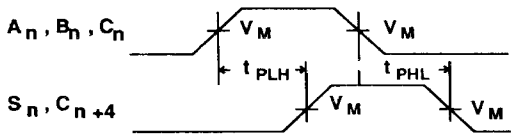
NOTES:

1. For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable type.
2. All typical values are at V_{CC} = 5V, T_A = 25°C.
3. Not more than one output should be shorted at a time. For testing I_{OS}, the use of high-speed test apparatus and/or sample-and-hold techniques are preferable in order to minimize internal heating and more accurately reflect operational values. Otherwise, prolonged shorting of a High output may raise the chip temperature well above normal and thereby cause invalid readings in other parameter tests. In any sequence of parameter tests, I_{OS} tests should be performed last.

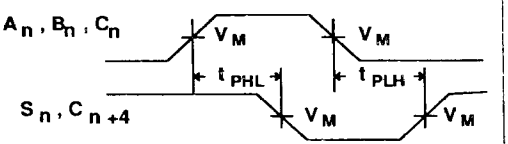
AC ELECTRICAL CHARACTERISTICS

SYMBOL	PARAMETER	TEST CONDITION	LIMITS					UNIT
			T_A = +25°C, V_{CC} = 5V, C_L = 50pF, R_L = 500Ω			T_A = 0°C to +70°C, V_{CC} = 5V ±10%, C_L = 50pF, R_L = 500Ω		
			Min	Typ	Max	Min	Max	
t_{PLH} t_{PHL}	Propagation delay A_n or B_n to S_n	Waveform 1	5.0 5.0	13.0 10.5	17.0 14.0	5.0 5.0	18.0 15.0	ns
t_{PLH} t_{PHL}	Propagation delay A_n or B_n to S_n (INV)	Waveform 2	6.0 4.0	11.0 8.0	18.0 12.0	5.0 4.0	19.5 12.5	ns
t_{PLH} t_{PHL}	Propagation delay C_n to C_{n+4}	Waveform 1,2	3.5 2.5	5.0 4.0	8.0 7.0	3.0 2.0	8.5 7.0	ns
t_{PLH} t_{PHL}	Propagation delay A_n or B_n to C_{n+4}	Waveform 1,2	5.0 5.0	8.0 7.5	11.5 10.5	4.5 4.5	13.0 11.5	ns
t_{PLH} t_{PHL}	Propagation delay C_n to S_n	Waveform 1	4.0 3.5	12.0 8.0	15.5 12.5	3.5 3.0	17.0 13.5	ns
t_{PLH} t_{PHL}	Propagation delay C_n to S_n (INV)	Waveform 2	6.0 3.5	9.5 8.0	13.0 11.5	5.0 3.0	14.5 12.0	ns

AC WAVEFORMS



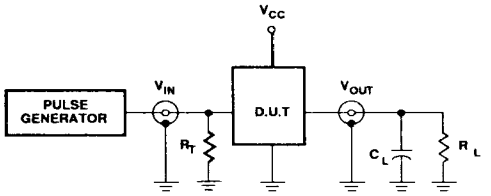
Waveform 1. Propagation Delay For Non-Inverting Outputs



Waveform 2. Propagation Delay For Inverting Outputs

NOTE: For all waveforms, V_M = 1.5V

TEST CIRCUIT AND WAVEFORMS



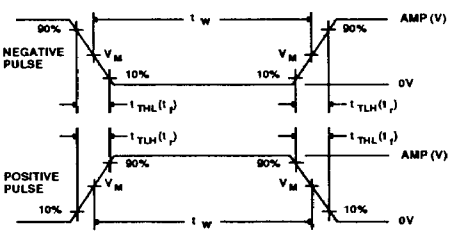
Test Circuit For Totem-Pole Outputs

DEFINITIONS

R_L = Load resistor; see AC CHARACTERISTICS for value.

C_L = Load capacitance includes jig and probe capacitance; see AC CHARACTERISTICS for value.

R_T = Termination resistance should be equal to Z_{OUT} of pulse generators.



V_M = 1.5V

Input Pulse Definition

FAMILY	INPUT PULSE REQUIREMENTS				
	Amplitude	Rep. Rate	t_W	t_{TLH}	t_{THL}
74F	3.0V	1MHz	500ns	2.5ns	2.5ns