Errata V0.2 for IT8172G V0.6

Note: The corrections have been highlighted in red in the corresponding pages attached.

Errata Version	Section	Correction	Page
0.2	4	In Table 4-2, the signal VLMDOWN/GPIO14 should be corrected to VLMDOWN/GPIO13 and the signal VLMMUTE/GPIO13 should be corrected to VLMMUTE/ GPIO14.	15
0.1	1	• In the ATA 33 IDE Bus Controller features, one note will be added: There is one special condition in PCI IDE Function Bit Decoding. Please refer to the IT8172G Application Note, ITTM-AN-01040.	1
	6	• In Table 6-7, added one note for IDE Controller: “There is one special condition in PCI IDE Function Bit Decoding. Please refer to the IT8172G Application Note, ITTM-AN-01040.”	39

Table 4-2. Pin-out Tables in Alphabetical Order [continued]

Signal	Pin	Signal	Pin	Signal	Pin	Signal	Pin
MD18	AC18	PAR	K3	PCRW#	AD15	TCK	D5
MD19	AD18	PCA0/FRA0	AC8	PE	D10	TDI	A3
MD20	AF20	PCA1/FRA1	AE8	PME#	T1	TDO	B4
MD21	AE20	PCA2/FRA2	AF7	PPD0	A6	TEST0	D6
MD22	AD19	PCA3/FRA3	AD8	PPD1	B7	TEST1	AD22
MD23	AE21	PCA4/FRA4	AE7	PPD2	C8	TEST2	AC21
MD24	AB26	PCA5/FRA5	AF6	PPD3	A7	TEST3	AE23
MD25	Y24	PCA6/FRA6	AD7	PPD4	A10	TMS	C4
MD26	AA26	PCA7/FRA7	AE6	PPD5	C11	TRDY#	L3
MD27	W24	PCA8/FRA8	AF5	PPD6	E11	TRST#	B3
MD28	V23	PCA9/FRA9	AF4	PPD7	B11	TXD	D8
MD29	V24	PCA10/FRA10	AE5	PWRBTM	D16	USBD1M	B18
MD30	V25	PCA11/FRA11	AD6	PWRON#	B16	USBD1P	D17
MD31	T22	PCA12/FRA12	AC7	RAS#	AF25	USBD2M	C18
MWE#	AF23	PCA13/FRA13	AF3	RDWR#/ VALIDIN#/EVALID#	K26	USBD2P	A19
NMI#	C26	PCA14/FRA14	AE4	RDY#/RDRDY#	P23	USBOVR#	A20
PAD0	G4	PCA15/FRA15	AD5	REQ0#	V3	USBPEN#	D18
PAD1	E1	PCA16/FRA16	AC6	REQ1#	U1	VCCRTC	B17
PAD2	F2	PCA17/FRA17	AF2	REQ2#	T3	VCC3	AB10
PAD3	G3	PCA18/FRA18	AE3	RESET#	M22	VCC3	AB17
PAD4	H4	PCA19/FRA19	AD4	RI#	A5	VCC3	E10
PAD5	F1	PCA20/FRA20	AC5	ROMSIZ1	D13	VCC3	E17
PAD6	G2	PCA21/FRA21	AF1	RTCRST#	A16	VCC3	K5
PAD7	H3	PCA22/FRA22	AE2	RTS#	C7	VCC3	K22
PAD8	G1	PCA23/FRA23	AD3	RXD	A4	VCC3	U5
PAD9	H2	PCA24/FRA24	AC4	SCRCLK0	A14	VCC3	U22
PAD10	J3	PCA25/FRA25	AE1	SCRCLK1/GNT3#	A15	VCC5	E12
PAD11	L5	PCAS#	AE16	SCRIO0	B14	VCC5	E13
PAD12	H1	PCD0/FRD0	AF11	SCRIO1/REQ3#	D14	VCCH	E14
PAD13	K4	PCD1/FRD1	AE11	SCRPFET0#	A13	**VLMDOWN/ GPIO13**	A1
PAD14	M5	PCD2/FRD2	AD11	SCRPFET1#/ REQ4#	B15	**VLMMUTE/ GPIO14**	D4
PAD15	J2	PCD3/FRD3	AF10	SCRPRES0#	C14	VLMUP/GPIO12	B2
PAD16	M3	PCD4/FRD4	AB11	SCRPRES1#/ INTD#	E15	VSS	M12
PAD17	M2	PCD5/FRD5	AD10	SCRRST0#	B13	VSS	M13
PAD18	M1	PCD6/FRD6	AC9	SCRRST1#/ GNT4#	C15	VSS	M14
PAD19	N4	PCD7/FRD7	AD9	SERIRQ	C13	VSS	M15
PAD20	P5	PCD8/FRD8	AB4	SERR#	K2	VSS	N12
PAD21	N3	PCD9/FRD9	AC2	SIZ0	AC15	VSS	N13
PAD22	N2	PCD10/FRD10	AA4	SIZ1	AE15	VSS	N14
PAD23	N1	PCD11/FRD11	AB2	SLCT	B9	VSS	N15
PAD24	P4	PCD12/FRD12	Y4	SLIN#	B10	VSS	P12
PAD25	P2	PCD13/FRD13	AA2	SPDIFO	B1	VSS	P13
PAD26	P1	PCD14/FRD14	AA1	STB#	A8	VSS	P14
PAD27	R1	PCD15/FRD15	Y2	STOP#	K1	VSS	P15
PAD28	R5	PCDS#	AF16	SWRST#	V26	VSS	R12
PAD29	R2	PCICLK	U4	SZ0/CMD6	L23	VSS	R13
PAD30	R3	PCIRST#	W1	SZ1/CMD7	J25	VSS	R14
PAD31	R4	PCLK	AD16	SZ2/CMD8	L22	VSS	R15

1. Features

- **CPU Interface**
  - Directly connects the following 32-bit RISC microprocessor interfaces
    - MIPS 5 – NEC Vr5432, QED RM5231, RM5230
    - MIPS 4 – NEC Vr4310
    - Hitachi – SH4 (7750)
  - Supports CPU bus frequency up to 100 MHz
- **SDRAM Controller**
  - 32-bit data bus interface
  - Supports two banks of SDRAM, up to 128 MB in size
  - Provides deep buffer for CPU to SDRAM burst transfer
  - Provides deep buffer for PCI to SDRAM burst transfer
  - Supports bus frequency at up to 100 MHz
- **Flash/ROM Interface**
  - Flash memory area support up to 64M bytes, with 8-bit, 16-bit and 32-bit data access capability
  - ROM area size up to 4M bytes, with 8-bit, 16-bit and 32-bit data access capability
  - Maximum 12 chip-select signals supported
  - Shared with 68K like peripheral bus
- **Peripheral Bus Controller***
  - Glueless 68K like bus interface
  - No external latch required for addressing
  - 8-bit and 16-bit data bus interface
  - Shared with the Flash/ROM Interface
  - Supports up to four DMA channels
  - Cycle posting to avoid performance hit from slow device
- **PCI Bus Controller**
  - Provides CPU to PCI buffers for burst transfer
  - PCI arbiter supports up to 5 individual bus master devices
  - 33 MHz bus frequency
  - 32-bit data bus interface
- **Interrupt Controller**
  - Supports a maskable interrupt (INT0#) to CPU
  - Supports a non-maskable interrupt (NMI#) to CPU for severe events
  - The priority order of interrupt request lines can be assigned by software
  - Module interrupts can be masked on/off independently by setting the corresponding mask registers
- **DMA Controller**
  - Supports four channels request for LPC or ECP DMA mode data transfer
  - Supports PCI bus master accessing to SDRAM
- **Chaining DMA Controller**
  - Supports four independent software DMA channels for transferring data between the SDRAM and PCI devices
  - Supports chaining and non-chaining modes
  - Supports rotating and fixed priority types
- **Timers**
  - Two 16-bit auto-reload counters with pre-scale (1,1/4,1/8,1/16) from dividing of the CPU clock
  - Supports the interrupt generation upon the timer time-out
  - Provides one Watchdog timer to monitor VALIDOUT# signal
- **Smart Card Interface**
  - Compliant with Personal Computer Smart Card (PC/SC) Working Group standard
  - Compliant with smart card (ISO 7816) protocols
  - Card present detection
  - Supports smart card insertion power on feature
  - Supports one programmable clock frequency, and 7.1 MHz and 3.5 MHz (Default) card clocks
  - Supports two channels of smart card interface
  - Supports T=0, T=1 protocol
- **ATA 33 IDE Bus Controller**
  - One channel IDE controller for two devices
  - Supports master/DMA/slave mode IDE
  - Supports any 16-bit and 32-bit ordering access to IDE data port in bus-slave access mode
  - Built in with 8-level 32-bit post-write buffer
  - Built in with 16-level 16-bit pre-fetch buffer
  - Compatible with ATA/ATAPI-4
  - Compatible to ANSI ATA proposal PIO modes 0, 1, 2, 3, 4 with flow control, DMA modes 0, 1, 2 and UDMA modes 0, 1, 2

Note 1. There are some special conditions. Please refer to the IT8172 Application Note V2.1, ITTM-AN-01033.
Note 2. There is one special condition in PCI IDE Function Bit Decoding. Please refer to the IT8172G Application Note, ITTM-AN-01040.

Table 6-7. Mapping Relation between AD Lines and Device Function

Bus Number	Device Number	Function Number	Device Function	AD Line
0	0	0	CPU/PCI Bridge	11
0	1	0	Audio Digital Controller	12
0	1	1	DMA Controller	12
0	1	2	Chain-DMA Controller	12
0	1	3	USB Host	12
0	1	4	PCI/Internal Bus Bridge	12
0	1	5	IDE Controller*	12
0	1	6	68K Controller	12
0	2	-	External Device #1	13
0	3	-	External Device #2	14
0	4	-	External Device #3	15
0	5	-	External Device #4	16
0	6	-	External Device #5	17
0	7	-	External Device #6	18
0	8	-	External Device #7	19
0	9	-	External Device #8	20
0	10	-	External Device #9	21
0	11	-	External Device #10	22
0	12	-	External Device #11	23
0	13	-	External Device #12	24
0	14	-	External Device #13	25
0	15	-	External Device #14	26
0	16	-	External Device #15	27
0	17	-	External Device #16	28
0	18	-	External Device #17	29
0	19	-	External Device #18	30
0	20	-	External Device #19	31

Type 1 Configuration Access – If the Bus Number field of CONFADDR is not 0, a Type 1 Configuration is performed on PCI bus. The CONFADDR[23:2] is mapped directly to AD[23:2]. AD[1:0] are driven to ″01″ to indicate a Type 1 Configuration cycle. All other AD lines are driven to 0.

*** There is one special condition in PCI IDE Function Bit Decoding. Please refer to the IT8172G Application Note, ITTM-AN-01040.**