

128K x 8 HIGH-SPEED CMOS STATIC RAM

NOVEMBER 1998

FEATURES

- High-speed access time: 12, 15, 20, 25 ns
- Low active power: 600 mW (typical)
- Low standby power: 500 μ W (typical) CMOS standby
- Output Enable ($\overline{OE}$) and two Chip Enable ($\overline{CE1}$ and CE2) inputs for ease in applications
- Fully static operation: no clock or refresh required
- TTL compatible inputs and outputs
- Single 5V ($\pm 10\%$) power supply
- Low power version available: IS61C1024L
- Commercial and industrial temperature ranges available

DESCRIPTION

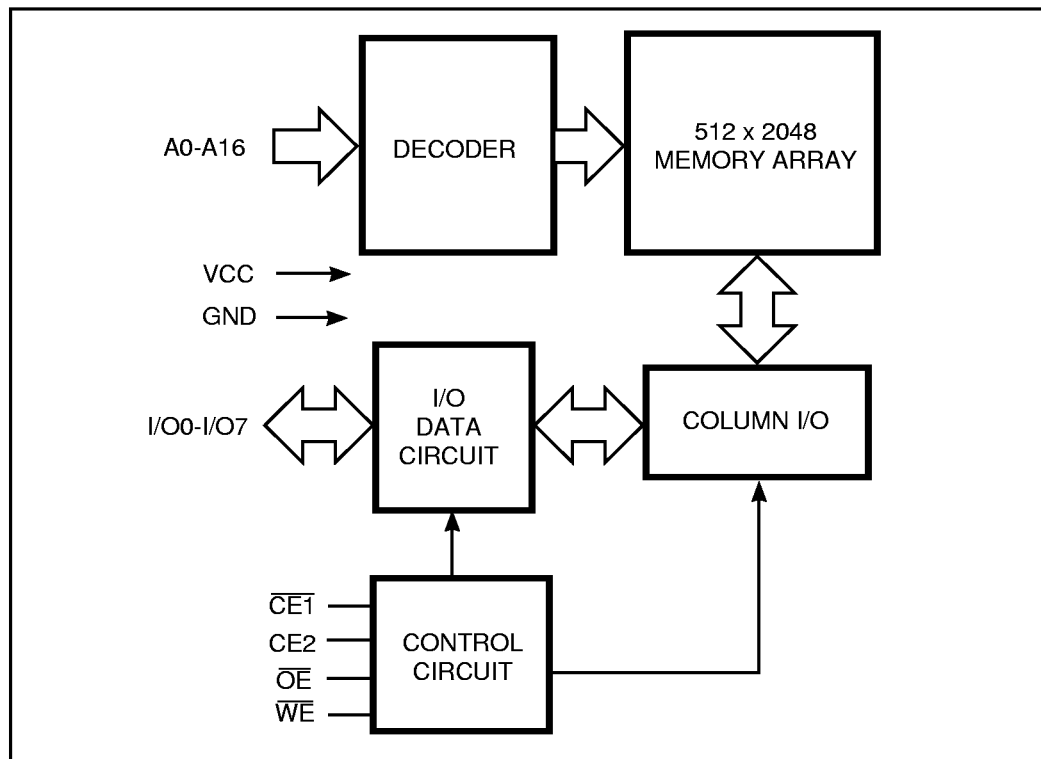
The *ISSI* IS61C1024 and IS61C1024L are very high-speed, low power, 131,072-word by 8-bit CMOS static RAMs. They are fabricated using *ISSI*'s high-performance CMOS technology. This highly reliable process coupled with innovative circuit design techniques, yields higher performance and low power consumption devices.

When $\overline{CE1}$ is HIGH or CE2 is LOW (deselected), the device assumes a standby mode at which the power dissipation can be reduced by using CMOS input levels.

Easy memory expansion is provided by using two Chip Enable inputs, $\overline{CE1}$ and CE2. The active LOW Write Enable ($\overline{WE}$) controls both writing and reading of the memory.

The IS61C1024 and IS61C1024L are available in 32-pin 300-mil plastic DIP, STSOP (8 x 13.4), 300-mil SOJ, and TSOP (Type I) packages.

FUNCTIONAL BLOCK DIAGRAM



ISSI reserves the right to make changes to its products at any time without notice in order to improve design and supply the best possible product. We assume no responsibility for any errors which may appear in this publication. © Copyright 1998, Integrated Silicon Solution, Inc.

PIN CONFIGURATION

32-Pin SOJ

NC	1	32	VCC
A16	2	31	A15
A14	3	30	CE2
A12	4	29	WE
A7	5	28	A13
A6	6	27	A8
A5	7	26	A9
A4	8	25	A11
A3	9	24	OE
A2	10	23	A10
A1	11	22	CE1
A0	12	21	I/O7
I/O0	13	20	I/O6
I/O1	14	19	I/O5
I/O2	15	18	I/O4
GND	16	17	I/O3

PIN CONFIGURATION

32-Pin TSOP (Type 1) (T) and STSOP (Type 1) (H)

A11	1	32	OE
A9	2	31	A10
A8	3	30	CE1
A13	4	29	I/O7
WE	5	28	I/O6
CE2	6	27	I/O5
A15	7	26	I/O4
VCC	8	25	I/O3
NC	9	24	GND
A16	10	23	I/O2
A14	11	22	I/O1
A12	12	21	I/O0
A7	13	20	A0
A6	14	19	A1
A5	15	18	A2
A4	16	17	A3

PIN DESCRIPTIONS

A0-A16	Address Inputs
CE1	Chip Enable 1 Input
CE2	Chip Enable 2 Input
OE	Output Enable Input
WE	Write Enable Input
I/O0-I/O7	Input/Output
Vcc	Power
GND	Ground

OPERATING RANGE

Range	Ambient Temperature	Vcc
Commercial	0°C to +70°C	5V ± 10%
Industrial	-40°C to +85°C	5V ± 10%

TRUTH TABLE

Mode	WE	CE1	CE2	OE	I/O Operation	Vcc Current
Not Selected	X	H	X	X	High-Z	Isb1, Isb2
(Power-down)	X	X	L	X	High-Z	Isb1, Isb2
Output Disabled	H	L	H	H	High-Z	Icc1, Icc2
Read	H	L	H	L	DOUT	Icc1, Icc2
Write	L	L	H	X	DIN	Icc1, Icc2

ABSOLUTE MAXIMUM RATINGS⁽¹⁾

Symbol	Parameter	Value	Unit
V _{TERM}	Terminal Voltage with Respect to GND	−0.5 to +7.0	V
T _{BIAS}	Temperature Under Bias	−55 to +125	°C
T _{STG}	Storage Temperature	−65 to +150	°C
P _T	Power Dissipation	1.5	W
I _{OUT}	DC Output Current (LOW)	20	mA

Notes:

1. Stress greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

CAPACITANCE^(1,2)

Symbol	Parameter	Conditions	Max.	Unit
C _{IN}	Input Capacitance	V _{IN} = 0V	5	pF
C _{OUT}	Output Capacitance	V _{OUT} = 0V	7	pF

Notes:

1. Tested initially and after any design or process changes that may affect these parameters.
2. Test conditions: T_A = 25°C, f = 1 MHz, V_{CC} = 5.0V.

DC ELECTRICAL CHARACTERISTICS (Over Operating Range)

Symbol	Parameter	Test Conditions		Min.	Max.	Unit
V _{OH}	Output HIGH Voltage	V _{CC} = Min., I _{OH} = −4.0 mA		2.4	—	V
V _{OL}	Output LOW Voltage	V _{CC} = Min., I _{OL} = 8.0 mA		—	0.4	V
V _{IH}	Input HIGH Voltage			2.2	V _{CC} + 0.5	V
V _{IL}	Input LOW Voltage ⁽¹⁾			−0.3	0.8	V
I _{LI}	Input Leakage	GND ≤ V _{IN} ≤ V _{CC}	Com. Ind.	−2 −5	2 5	μA
I _{LO}	Output Leakage	GND ≤ V _{OUT} ≤ V _{CC} Outputs Disabled	Com. Ind.	−2 −5	2 5	μA

Note:

1. V_{IL} = −3.0V for pulse width less than 10 ns.

IS61C1024 POWER SUPPLY CHARACTERISTICS⁽¹⁾ (Over Operating Range)

Symbol	Parameter	Test Conditions		-12 ns		-15 ns		-20 ns		-25 ns		Unit
				Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
I _{CC1}	V _{CC} Operating Supply Current	V _{CC} = Max., $\overline{CE} = V_{IL}$ I _{OUT} = 0 mA, f = 0	Com.	—	140	—	140	—	140	—	140	mA
			Ind.	—	140	—	140	—	140	—	140	
I _{CC2}	V _{CC} Dynamic Operating Supply Current	V _{CC} = Max., $\overline{CE} = V_{IL}$ I _{OUT} = 0 mA, f = f _{MAX}	Com.	—	220	—	200	—	170	—	150	mA
			Ind.	—	220	—	200	—	170	—	150	
I _{SB1}	TTL Standby Current (TTL Inputs)	V _{CC} = Max., V _{IN} = V _{IH} or V _{IL} $\overline{CE1} \geq V_{IH}$, f = 0 or $\overline{CE2} \leq V_{IL}$, f = 0	Com.	—	40	—	40	—	40	—	40	mA
			Ind.	—	60	—	60	—	60	—	60	
I _{SB2}	CMOS Standby Current (CMOS Inputs)	V _{CC} = Max., $\overline{CE1} \leq V_{CC} - 0.2V$, $\overline{CE2} \leq 0.2V$ V _{IN} > V _{CC} - 0.2V, or V _{IN} ≤ 0.2V, f = 0	Com.	—	30	—	30	—	30	—	30	mA
			Ind.	—	40	—	40	—	40	—	40	

Note:

1. At f = f_{MAX}, address and data inputs are cycling at the maximum frequency, f = 0 means no input lines change.

IS61C1024L POWER SUPPLY CHARACTERISTICS⁽¹⁾ (Over Operating Range)

Symbol	Parameter	Test Conditions		-15 ns		-20 ns		-25 ns		Unit
				Min.	Max.	Min.	Max.	Min.	Max.	
I _{CC1}	V _{CC} Operating Supply Current	V _{CC} = Max., $\overline{CE} = V_{IL}$ I _{OUT} = 0 mA, f = 0	Com.	—	85	—	85	—	85	mA
			Ind.	—	110	—	110	—	110	
I _{CC2}	V _{CC} Dynamic Operating Supply Current	V _{CC} = Max., $\overline{CE} = V_{IL}$ I _{OUT} = 0 mA, f = f _{MAX}	Com.	—	160	—	150	—	150	mA
			Ind.	—	160	—	150	—	150	
I _{SB1}	TTL Standby Current (TTL Inputs)	V _{CC} = Max., V _{IN} = V _{IH} or V _{IL} $\overline{CE1} \geq V_{IH}$, f = 0 or $\overline{CE2} \leq V_{IL}$, f = 0	Com.	—	40	—	40	—	40	mA
			Ind.	—	60	—	60	—	60	
I _{SB2}	CMOS Standby Current (CMOS Inputs)	V _{CC} = Max., $\overline{CE1} \leq V_{CC} - 0.2V$, $\overline{CE2} \leq 0.2V$ V _{IN} > V _{CC} - 0.2V, or V _{IN} ≤ 0.2V, f = 0	Com.	—	500	—	500	—	500	μA
			Ind.	—	750	—	750	—	750	

Note:

1. At f = f_{MAX}, address and data inputs are cycling at the maximum frequency, f = 0 means no input lines change.

READ CYCLE SWITCHING CHARACTERISTICS⁽¹⁾ (Over Operating Range)

Symbol	Parameter	-12 ⁽²⁾		-15 ns		-20 ns		-25 ns		Unit
		Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
t _{RC}	Read Cycle Time	12	—	15	—	20	—	25	—	ns
t _{AA}	Address Access Time	—	12	—	15	—	20	—	25	ns
t _{OH}	Output Hold Time	3	—	3	—	3	—	3	—	ns
t _{ACE1}	$\overline{\text{CE1}}$ Access Time	—	12	—	15	—	20	—	25	ns
t _{ACE2}	CE2 Access Time	—	12	—	15	—	20	—	25	ns
t _{DOE}	$\overline{\text{OE}}$ Access Time	—	6	—	7	—	9	—	9	ns
t _{LZOE} ⁽³⁾	$\overline{\text{OE}}$ to Low-Z Output	0	—	0	—	0	—	0	—	ns
t _{HZOE} ⁽³⁾	$\overline{\text{OE}}$ to High-Z Output	0	6	0	6	0	7	0	10	ns
t _{LZCE1} ⁽³⁾	$\overline{\text{CE1}}$ to Low-Z Output	2	—	2	—	3	—	3	—	ns
t _{LZCE2} ⁽³⁾	CE2 to Low-Z Output	2	—	2	—	3	—	3	—	ns
t _{HZCE} ⁽³⁾	$\overline{\text{CE1}}$ or CE2 to High-Z Output	0	7	0	8	0	9	0	10	ns
t _{PU} ⁽⁴⁾	$\overline{\text{CE1}}$ or CE2 to Power-Up	0	—	0	—	0	—	0	—	ns
t _{PD} ⁽⁴⁾	$\overline{\text{CE1}}$ or CE2 to Power-Down	—	12	—	12	—	18	—	20	ns

Notes:

1. Test conditions assume signal transition times of 3 ns or less, timing reference levels of 1.5V, input pulse levels of 0 to 3.0V and output loading specified in Figure 1.
2. -12 ns device for IS61C1024 only.
3. Tested with the load in Figure 2. Transition is measured ± 500 mV from steady-state voltage. Not 100% tested.
4. Not 100% tested.

AC TEST CONDITIONS

Parameter	Unit
Input Pulse Level	0V to 3.0V
Input Rise and Fall Times	3 ns
Input and Output Timing and Reference Level	1.5V
Output Load	See Figures 1 and 2

AC TEST LOADS

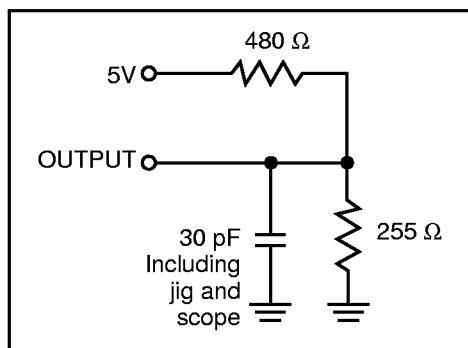


Figure 1

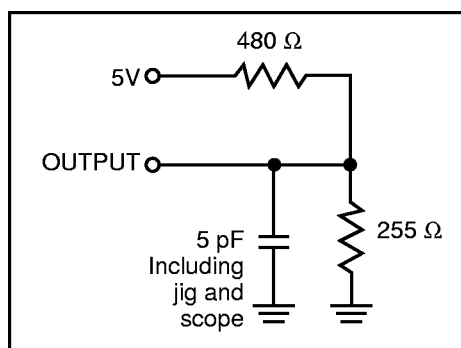
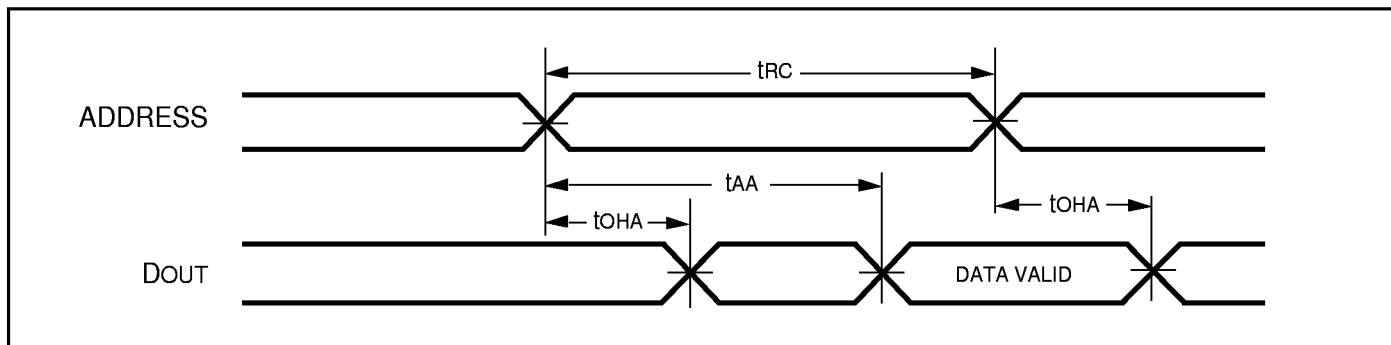


Figure 2

READ CYCLE NO. 1^(1,2)



1. $\overline{\text{WE}}$ is HIGH for a Read Cycle.
2. The device is continuously selected. $\overline{\text{OE}}, \overline{\text{CE1}} = \text{V}_{\text{IL}}, \text{CE2} = \text{V}_{\text{IH}}$.
3. Address is valid prior to or coincident with $\overline{\text{CE1}}$ LOW and CE2 HIGH transitions.

WRITE CYCLE SWITCHING CHARACTERISTICS^(1,2) (Over Operating Range, Standard and Low Power)

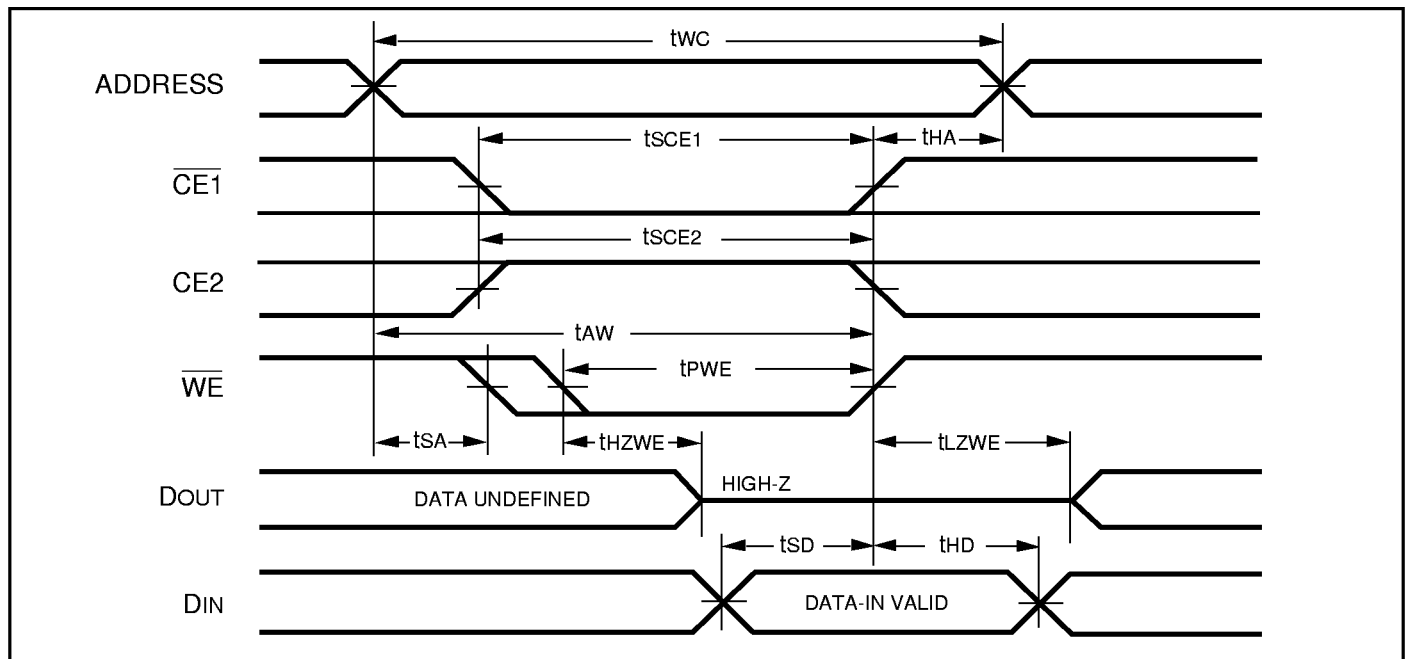
Symbol	Parameter	-12 ns ⁽³⁾		-15 ns		-20 ns		-25 ns		Unit
		Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
t _{WC}	Write Cycle Time	12	—	15	—	20	—	25	—	ns
t _{SCE1}	$\overline{CE1}$ to Write End	10	—	12	—	15	—	20	—	ns
t _{SCE2}	CE2 to Write End	10	—	12	—	15	—	20	—	ns
t _{AW}	Address Setup Time to Write End	10	—	12	—	15	—	20	—	ns
t _{HA}	Address Hold from Write End	0	—	0	—	0	—	0	—	ns
t _{SA}	Address Setup Time	0	—	0	—	0	—	0	—	ns
t _{PWE⁽⁴⁾}	$\overline{WE}$ Pulse Width	10	—	10	—	12	—	15	—	ns
t _{SD}	Data Setup to Write End	7	—	8	—	10	—	12	—	ns
t _{HD}	Data Hold from Write End	0	—	0	—	0	—	0	—	ns
t _{HZWE⁽⁵⁾}	$\overline{WE}$ LOW to High-Z Output	—	7	—	7	—	10	—	12	ns
t _{LZWE⁽⁵⁾}	$\overline{WE}$ HIGH to Low-Z Output	2	—	2	—	2	—	2	—	ns

Notes:

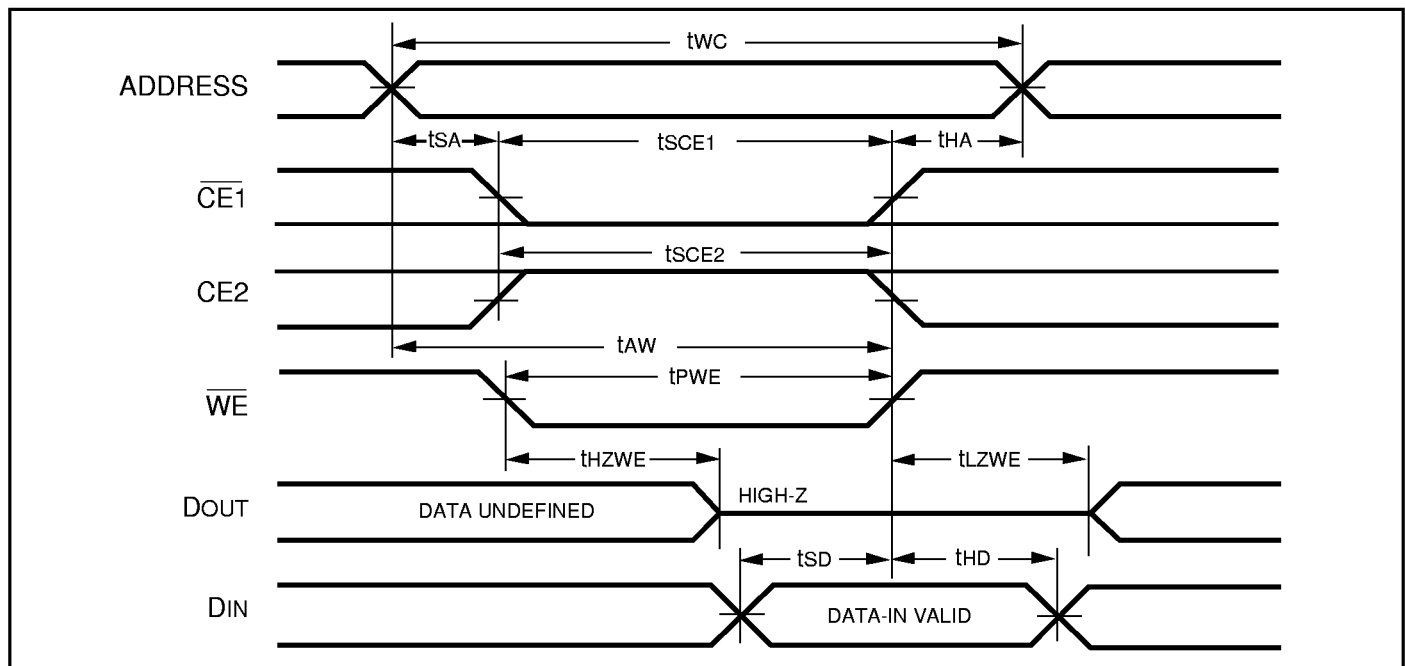
1. Test conditions assume signal transition times of 5 ns or less, timing reference levels of 1.5V, input pulse levels of 0 to 3.0V and output loading specified in Figure 1.
2. The internal write time is defined by the overlap of $\overline{CE1}$ LOW, CE2 HIGH and $\overline{WE}$ LOW. All signals must be in valid states to initiate a Write, but any one can go inactive to terminate the Write. The Data Input Setup and Hold timing are referenced to the rising or falling edge of the signal that terminates the Write.
3. -12 ns device for IS61C1024 only.
4. Tested with $\overline{OE}$ HIGH.
5. Tested with the load in Figure 2. Transition is measured ± 500 mV from steady-state voltage. Not 100% tested.

AC WAVEFORMS

WRITE CYCLE NO. 1^(1,2) ($\overline{WE}$ Controlled)



WRITE CYCLE NO. 2^(1,2) ($\overline{CE1}$, CE2 Controlled)



Notes:

1. The internal write time is defined by the overlap of $\overline{CE1}$ LOW, CE2 HIGH and $\overline{WE}$ LOW. All signals must be in valid states to initiate a Write, but any one can go inactive to terminate the Write. The Data Input Setup and Hold timing are referenced to the rising or falling edge of the signal that terminates the Write.
2. I/O will assume the High-Z state if $\overline{OE} = V_{IH}$.

IS61C1024 STANDARD VERSION
ORDERING INFORMATION
Commercial Range: 0°C to +70°C

Speed (ns)	Order Part No.	Package
12	IS61C1024-12J	300-mil Plastic SOJ
12	IS61C1024-12N	300-mil Plastic DIP
12	IS61C1024-12K	400-mil Plastic SOJ
12	IS61C1024-12H	STSOP (Type I)
12	IS61C1024-12T	TSOP (Type I)
15	IS61C1024-15J	300-mil Plastic SOJ
15	IS61C1024-15N	300-mil Plastic DIP
15	IS61C1024-15K	400-mil Plastic SOJ
15	IS61C1024-15H	STSOP (Type I)
15	IS61C1024-15T	TSOP (Type I)
20	IS61C1024-20J	300-mil Plastic SOJ
20	IS61C1024-20N	300-mil Plastic DIP
20	IS61C1024-20K	400-mil Plastic SOJ
20	IS61C1024-20H	STSOP (Type I)
20	IS61C1024-20T	TSOP (Type I)
25	IS61C1024-25J	300-mil Plastic SOJ
25	IS61C1024-25N	300-mil Plastic DIP
25	IS61C1024-25K	400-mil Plastic SOJ
25	IS61C1024-25H	STSOP (Type I)
25	IS61C1024-25T	TSOP (Type I)

IS61C1024 STANDARD VERSION
ORDERING INFORMATION
Industrial Range: -40°C to +85°C

Speed (ns)	Order Part No.	Package
12	IS61C1024-12JI	300-mil Plastic SOJ
12	IS61C1024-12NI	300-mil Plastic DIP
12	IS61C1024-12KI	400-mil Plastic SOJ
12	IS61C1024-12HI	STSOP (Type I)
12	IS61C1024-12TI	TSOP (Type I)
15	IS61C1024-15JI	300-mil Plastic SOJ
15	IS61C1024-15NI	300-mil Plastic DIP
15	IS61C1024-15KI	400-mil Plastic SOJ
15	IS61C1024-15HI	STSOP (Type I)
15	IS61C1024-15TI	TSOP (Type I)
20	IS61C1024-20JI	300-mil Plastic SOJ
20	IS61C1024-20NI	300-mil Plastic DIP
20	IS61C1024-20KI	400-mil Plastic SOJ
20	IS61C1024-20HI	STSOP (Type I)
20	IS61C1024-20TI	TSOP (Type I)
25	IS61C1024-25JI	300-mil Plastic SOJ
25	IS61C1024-25NI	300-mil Plastic DIP
25	IS61C1024-25KI	400-mil Plastic SOJ
25	IS61C1024-25HI	STSOP (Type I)
25	IS61C1024-25TI	TSOP (Type I)

IS61C1024L LOW POWER VERSION
ORDERING INFORMATION
Commercial Range: 0°C to +70°C

Speed (ns)	Order Part No.	Package
15	IS61C1024L-15J	300-mil Plastic SOJ
	IS61C1024L-15N	300-mil Plastic DIP
	IS61C1024L-15K	400-mil Plastic SOJ
	IS61C1024L-15H	STSOP (Type I)
	IS61C1024L-15T	TSOP (Type I)
20	IS61C1024L-20J	300-mil Plastic SOJ
	IS61C1024L-20N	300-mil Plastic DIP
	IS61C1024L-20K	400-mil Plastic SOJ
	IS61C1024L-20H	STSOP (Type I)
	IS61C1024L-20T	TSOP (Type I)
25	IS61C1024L-25J	300-mil Plastic SOJ
	IS61C1024L-25N	300-mil Plastic DIP
	IS61C1024L-25K	400-mil Plastic SOJ
	IS61C1024L-25H	STSOP (Type I)
	IS61C1024L-25T	TSOP (Type I)

IS61C1024L LOW POWER VERSION
ORDERING INFORMATION
Industrial Range: -40°C to +85°C

Speed (ns)	Order Part No.	Package
15	IS61C1024L-15JI	300-mil Plastic SOJ
	IS61C1024L-15NI	300-mil Plastic DIP
	IS61C1024L-15KI	400-mil Plastic SOJ
	IS61C1024L-12HRI	STSOP (Type I)
	IS61C1024L-15TI	TSOP (Type I)
20	IS61C1024L-20JI	300-mil Plastic SOJ
	IS61C1024L-20NI	300-mil Plastic DIP
	IS61C1024L-20KI	400-mil Plastic SOJ
	IS61C1024L-12HRI	STSOP (Type I)
	IS61C1024L-20TI	TSOP (Type I)
25	IS61C1024L-25JI	300-mil Plastic SOJ
	IS61C1024L-25NI	300-mil Plastic DIP
	IS61C1024L-25KI	400-mil Plastic SOJ
	IS61C1024L-12HRI	STSOP (Type I)
	IS61C1024L-25TI	TSOP (Type I)

NOTICE

Integrated Silicon Solution, Inc., reserves the right to make changes to the products contained in this publication in order to improve design, performance or reliability. Integrated Silicon Solution, Inc. assumes no responsibility for the use of any circuits described herein, conveys no license under any patent or other right, and makes no representation that the circuits are free of patent infringement. Charts and schedules contained herein reflect representative operating parameters, and may vary depending upon a user's specific application. While the information in this publication has been carefully checked, Integrated Silicon Solution, Inc. shall not be liable for any damages arising as a result of any error or omission.

Integrated Silicon Solution, Inc. does not recommend the use of any of its products in life support applications where the failure or malfunction of the product can reasonably be expected to cause failure of the life support system or to significantly affect its safety or effectiveness. Products are not authorized for use in such applications unless Integrated Silicon Solution, Inc. receives written assurances, to its satisfaction, that: (a) the risk of injury or damage has been minimized; (b) the user assumes all such risks; and (c) potential liability of Integrated Silicon Solution, Inc. is adequately protected under the circumstances.

Copyright 1998 Integrated Silicon Solution, Inc.

Reproduction in whole or in part, without the prior written consent of Integrated Silicon Solution, Inc., is prohibited.



Integrated Silicon Solution, Inc.

2231 Lawson Lane

Santa Clara, CA 95054

Fax: (408) 588-0806

Toll Free: 1-800-379-4774

E-mail: sales@issi.com

<http://www.issi.com>