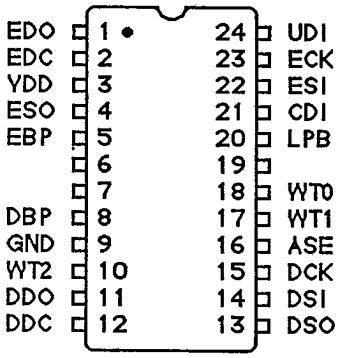
# HYPER-FEC III CMOS HARD DECISION FORWARD ERROR CORRECTION ENCODER/DECODER 241203

## FEATURES

- ◊ Information data bit rates from DC to 20 Mbits per second
- ◊ Decoder corrects up to 3 bit errors per 24-bit codeword and detects 4 errors
- ◊ Approximately 3dB of net coding gain and 6dB of transfer gain at one error per million
- ◊ Automatically synchronizes using error free data with no loss of data. Short sync acquisition time.
- ◊ Decoder delay of only 35 information bit periods
- ◊ Decoder outputs number of errors in each received codeword
- ◊ Single +5V supply
- ◊ Loopback and bypass modes
- ◊ Low power CMOS design - compatible with both TTL and CMOS logic

## PIN CONFIGURATION (Top View)




**PIN NAMES**

| | |
|---|---|
| UDI - UNCODED DATA INPUT | EDO - ENCODER DATA OUTPUT |
| ECK - ENCODER CLOCK | EDC - ENCODER DATA CLOCK |
| ESI - ENCODER SYNC INPUT | ESO - ENCODER SYNC OUTPUT |
| CDI - CODED DATA INPUT | EBP - ENCODER BYPASS |
| LPB - LOOPBACK ENABLE | DBP - DECODER BYPASS |
| WT0 - ERROR WEIGHT BIT 0 | WT2 - ERROR WEIGHT BIT 2 |
| WT1 - ERROR WEIGHT BIT 1 | DDO - DECODER DATA OUTPUT |
| ASE - AUTO-SYNC ENABLE | DDC - DECODER DATA CLOCK |
| DCK - DECODER CLOCK | YDD - POWER |
| DSI - DECODER SYNC INPUT | GND - GROUND |
| DSO - DECODER SYNC OUTPUT | |

**FIGURE 1. PIN CONFIGURATION.**

## DESCRIPTION

The 241203 HYPER-FEC III Encoder/Decoder consists of a Hard Decision encoder and decoder designed to detect and correct errors in digital transmission channels. The Encoder accepts a 12-bit serial data word, and by adding check bits, converts it to a 24-bit serial codeword. The Decoder receives the serial codeword and performs the decoding algorithm to correct up to three and detect any four random errors occuring anywhere in the received codeword. The corrected 12-bit data word is then extracted from the 24-bit codeword and is outputted serially. The Encoder and Decoder are functionally independent, enabling full duplex operation at the same or different data rates. The HYPER-FEC III is based on a one-half rate (24,12) extended Golay short block code.

The only inputs required by the Encoder (Decoder) are uncoded data (coded data) and clock. The user can provide an optional encoder sync to specify the 12-bit data word boundaries. An encoder sync output is provided to help synchronize the coded output data with other equipment.

The Decoder contains an auto-synchronization circuit which locks in after only two consecutive error-free words have been received. The auto-sync circuit is constantly monitoring itself to prevent false sync acquisition and to reacquire sync, if sync is lost. The auto-sync circuit can be overridden, if desired, by applying an external synchronization signal. A sync output is provided to synchronize the decoded output data with other equipment. The decoder measures the bit-error-rate by counting and outputting the number of errors detected in each input codeword.

The HYPER-FEC III is offered in a 24-pin, 600 mil, dual-in-line plastic package and is guaranteed to operate from 0°C to 70°C. Industrial and military grade parts are available by special request.

## CODE SPECIFICATION

| | | | |
|---|---|---|---|
| CODE TYPE: | Hard Decision (24,12) Extended Golay | CODE RATE: | 1/2 |
| NET CODING GAIN: | 3dB @ BER of $1 \times 10^{-6}$ | TRANSFER CODING GAIN: | 6dB @ BER of $1 \times 10^{-6}$ |
| EFFICIENCY: | Theoretical upper bound, i.e., an optimal quasi-perfect code | THROUGHPUT RATE: | DC to 20 MBits per second of user data |

## PIN DESCRIPTIONS (ENCODER)

**ESI** ENCODER SYNC INPUT - An optional input used to synchronize the encoder timing. The sync signal should occur during the last bit period (bit 12) of a data word to establish the timing for all subsequent data bits until the next sync pulse occurs. ESI is clocked into the encoder with the falling edge of ECK.

**ECK** ENCODER CLOCK - This input provides the timing for the encoder and shouldbe run at the coded data rate, i.e. twice the rate of the uncoded input data (UDI).

**UDI** UNCODED DATA INPUT - The serial input data to be encoded. One data word consists of 12 bits of data. The input data bit rate is one-half the rate of the encoder clock (ECK).

**ESO** ENCODER SYNC OUTPUT - This output establishes the encoder data output (EDO) codeword boundaries. The pulse width of ESO is equal to one output bit time with the falling edge occuring at the midpoint of the the 24th bit of the codeword.

**EDC** ENCODER DATA CLOCK - This output is a clock signal running at the rate of the input data, i.e. one-half the rate of the encoder clock (ECK). EDC is used to clock in the uncoded data input (UDI).

**EDO** ENCODER DATA OUTPUT - This output is the serially coded data output running at the rate of the encoder clock (ECK). It is formatted into 24-bit codewords.

**EBP** ENCODER BYPASS - This input signal allows the user to bypass the encoding process. When enabled (HIGH), the uncoded data input (UDI) is connected directly to the encoder data output (EDO). EBP must be disabled (LOW) for encoder operation.

## PIN DESCRIPTIONS (DECODER)

**CDI** CODED DATA INPUT - This input is the serial input coded data for decoding. One codeword consists of 24 bits (12 data plus 12 parity check bits). This input runs at the rate of the decoder clock (DDC).

**DCK** DECODER CLOCK - This input clock provides the timing for the decoder and runs at the coded data rate. Codeword data bits are clocked into the decoder on the rising edge of DCK.

**DSI** DECODER SYNC INPUT - This optional input sync signal establishes codeword synchronization. DSI should occur during the last bit period (bit 24) of a codeword to establish the timing for all subsequent codewords until the next sync pulse occurs.

**DDO** DECODER DATA OUTPUT - This output is the serially decoded data output running at half the rate of the decoder clock (DCK). It should be considered as an error free data word unless 4 errors are detected (WT2 = HIGH).

**DDC** DECODER DATA CLOCK - This output clock signal runs at the rate of the decoder data output, i.e. one-half the rate of the decoder clock (DCK). DDC clocks out the decoder data output (DDO) on the falling edge.

**DSO** DECODER SYNC OUTPUT - This output signal is synchronous with the last bit of each output data word. DSO can be used to synchronize the transfer of output data words to external equipment or circuitry.

**ASE** AUTO SYNC ENABLE - This input signal is used to enable (HIGH) or disable (LOW) the decoder's internal auto sync circuitry. ASE has an internal pullup so that the auto sync is enabled with no pin connection.

**LPB** LOOPBACK ENABLE - This input signal enables (HIGH) or disables (LOW) the connection of the encoder output to the decoder input to facilitate loopback testing.

**DBP** DECODER BYPASS - This input signal allows the user to bypass the decoding process. When enabled (HIGH), the decoder data input (CDI) is connected directly to the decoder data output (DDO). DBP must be disabled (LOW) for encoder operation.

**WT0-2** WEIGHT OUTPUT - The weight output signals indicate the weight (# of errors) of the error pattern detected for each codeword. Error patterns with a weight of 4 are not correctable and therefore the decoded data output (DDO) is outputted with no corrections.

| WT2 | WT1 | WT0 | # OF ERRORS |
|---|---|---|---|
| 0 | 0 | 0 | 0 |
| 0 | 0 | 1 | 1 |
| 0 | 1 | 0 | 2 |
| 0 | 1 | 1 | 3 |
| 1 | 0 | 0 | 4 |

## ABSOLUTE MAXIMUM RATINGS

| | |
|---|---|
| Ambient Operating Temperature | 0°C to +70°C |
| Storage Temperature | -65°C to +150°C |
| Supply Voltage to Ground Potential | -0.5V to 7.0V |
| Applied Output Voltage | -0.5V to 7.0V |
| Applied Input Voltage | -0.5V to 7.0V |
| Power Dissipation | 100 mW at an uncoded data rate of 1 Mbit per second |

Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only. Functional operation of this device at these or any other conditions above those indicated on the operational sections of this specification is not implied and exposure to absolute maximum rating conditions for extended periods may affect device reliabilty.

## DC CHARACTERISTICS

**$T_A$ = 0°C to 70°C, VDD = 5V ± 5% (unless otherwise specified)**

| Symbol | Parameter | Min | Typ | Max | Units | Test Conditions |
|---|---|---|---|---|---|---|
| $V_{OH}$ | Output HIGH Voltage | 2.4 | | VDD | V | $I_{OH}$ = -0.4 mA |
| $V_{OL}$ | Output LOW Voltage | | | 0.4 | V | $I_{OL}$ = 1.6 mA |
| $V_{IH}$ | Input HIGH Voltage | 2.0 | | VDD | V | Note 1 |
| $V_{IL}$ | Input LOW Voltage | -0.5 | | 0.6 | V | Notes 1 & 2 |
| $I_{LI}$ | Input Leakage Current | | 20 | 100 | µA | Note 3 |
| $I_{LO}$ | Output Leakage Current | | 20 | | µA | |
| $I_{CC}$ | Power Supply Current | | 20 | | mA | Note 4 |

Note 1: Operation of chip at speeds higher than 10 MHz requires $V_{IH}$ = 3.8V (min) & $V_{IL}$ = 0.6V (max).
Note 2: Input levels that swing more negative than -0.5 V will be clamped and may cause damage to the device.
Note 3: Pin ASE is the only input pin that has a leakage current of 100 µA.
Note 4: $f_{data}$= 1 Mbit/second.

**TABLE 1. DC CHARACTERISTICS.**

## CAPACITANCE

**$T_A$ = 25°C, f = 5 MHz**

| Symbol | Parameter | Min | Typ | Max | Units | Test Conditions |
|---|---|---|---|---|---|---|
| $C_I$ | Input Capacitance | | | 10 | pf | All pins tied to AC gnd |
| $C_O$ | Output Capacitance | | | 10 | pf | except pins under test |

**TABLE 2. CAPACITANCE.**

## PACKAGE DIAGRAM

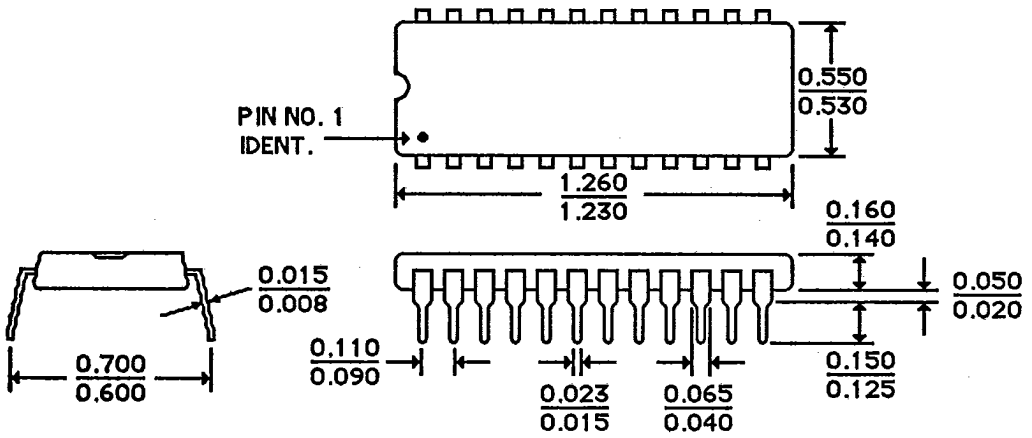



**FIGURE 2. 24-PIN PLASTIC DUAL-IN LINE PACKAGE.**

## CONTROL SIGNAL TRUTH TABLE

(ASE is assumed enabled if no signal is present)

| CONTROL SIGNAL | | ENABLE | DISABLE |
|---|---|---|---|
| LPB | LOOPBACK ENABLE | 1 | 0 |
| ASE | AUTO SYNC ENABLE | 1 | 0 |
| EBP | ENCODER BYPASS | 1 | 0 |
| DBP | DECODER BYPASS | 1 | 0 |

**TABLE 3. CONTROL SIGNALS.**

## TIMING INFORMATION: ENCODER

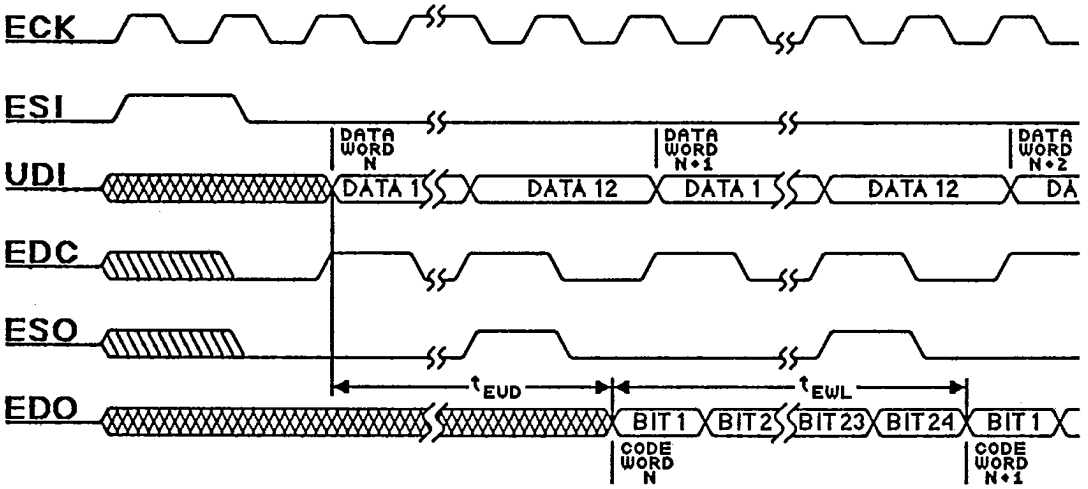



**FIGURE 3. OVERALL TIMING.**

## TIMING INFORMATION: ENCODER (Continued)

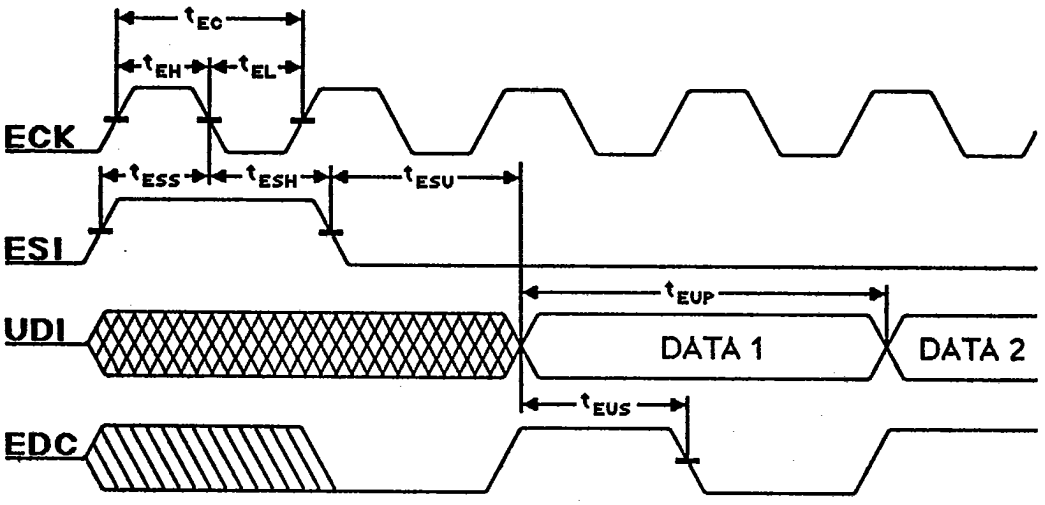



FIGURE 4. INPUT SYNC AND DATA TIMING.

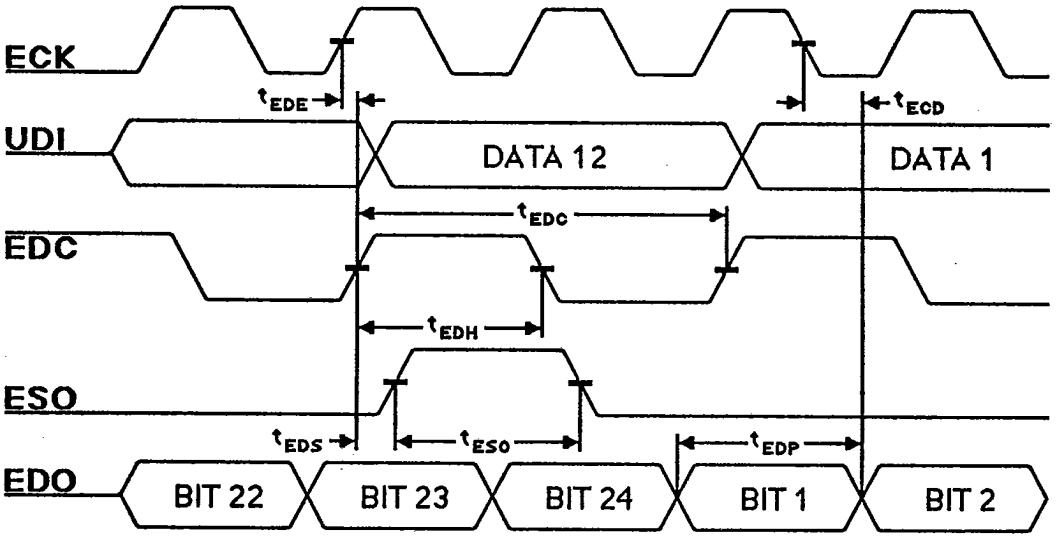



FIGURE 5. OUTPUT SYNC AND DATA TIMING.

## TIMING INFORMATION: ENCODER (Continued)

| SYMBOL | DESCRIPTION | MIN | TYP | MAX | UNITS | NOTES |
|---|---|---|---|---|---|---|
| $t_{EC}$ | ECK Cycle Time = T | 25 | | | ns | 1 |
| $t_{EH}$ | ECK HIGH Pulse Width = H | 12 | | | ns | |
| $t_{EL}$ | ECK LOW Pulse Width = L | 12 | | | ns | |
| $t_{ESS}$ | ESI Setup Time | 8 | H | T-8 | ns | |
| $t_{ESH}$ | ESI Hold Time | 4 | L | 2T-8 | ns | |
| $t_{ESU}$ | ESI to Valid UDI | | T | | ns | 2 |
| $t_{EUS}$ | UDI Setup Time | 10 | T | | ns | 3 |
| $t_{EUP}$ | UDI Bit Period | 2T | 2T | 2T | ns | |
| $t_{EDC}$ | EDC Cycle Time | 2T | 2T | 2T | ns | |
| $t_{EDH}$ | EDC HIGH Pulse Width | T | T | T | ns | |
| $t_{EDS}$ | EDC to ESO Time Delay | | | 10 | ns | |
| $t_{ESO}$ | ESO Pulse Width | T | T | T | ns | |
| $t_{EDP}$ | EDO Bit Period | T | T | T | ns | |
| $t_{ECD}$ | ECK LOW to Valid EDO | | | 15 | ns | 4 |
| $t_{EUD}$ | Valid UDI to Corresponding EDO | 24T-L | 24T-L | 24T-L | ns | 5 |
| $t_{EWL}$ | EDO Word Length | 24T | 24T | 24T | ns | |
| $t_{EDE}$ | ECK to EDC Time Delay | | 15 | 20 | ns | |

**NOTES:**
1) All times in nanoseconds.
2) $t_{ESU} = 2T + L - t_{ESH} - t_{EUS}$.
3) Typically EDC should go LOW near the center of data bit (UDI).
4) Data is clocked out of the Encoder on the falling edge of ECK.
5) Output data word (EDO) is delayed by approximately one complete data word from input data word (UDI).

**TABLE 4. ENCODER AC ELECTRICAL CHARACTERISTICS.**

## TIMING INFORMATION: DECODER

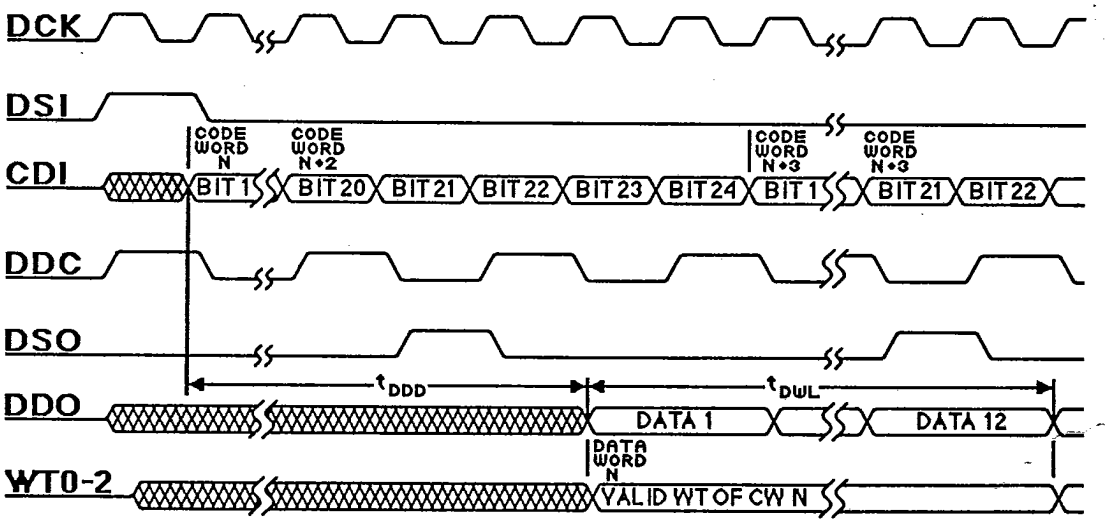



**FIGURE 6. OVERALL TIMING.**

## TIMING INFORMATION: DECODER (Continued)

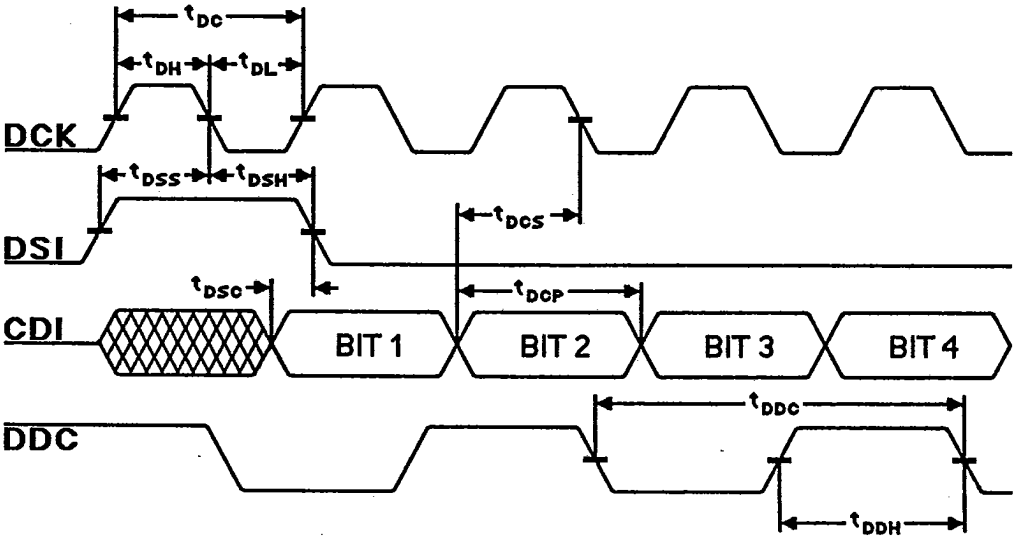



**FIGURE 7. INPUT SYNC AND DATA TIMING.**

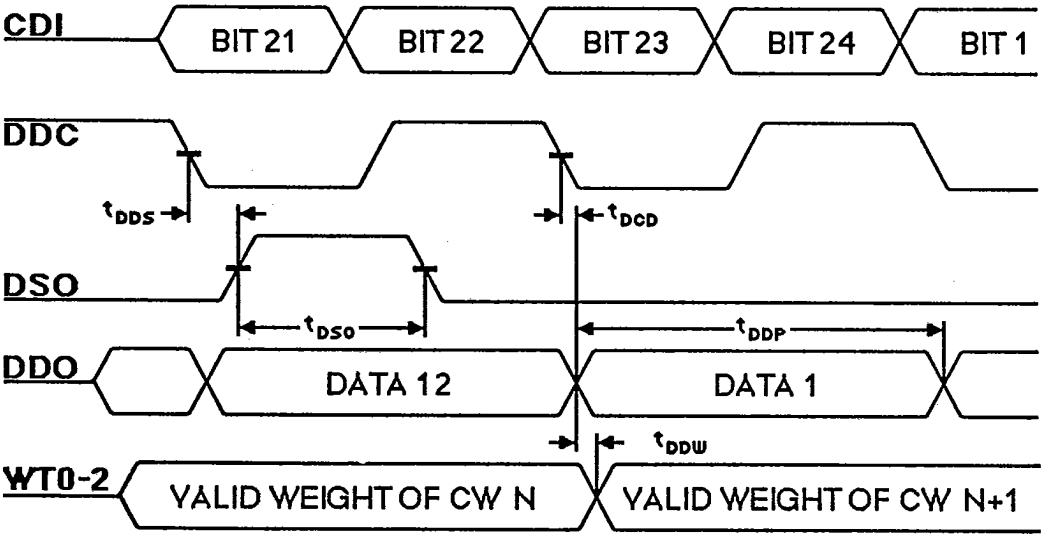



**FIGURE 8. OUTPUT SYNC AND DATA TIMING.**

## TIMING INFORMATION: DECODER (Continued)

| SYMBOL | DESCRIPTION | MIN | TYP | MAX | UNITS | NOTES |
|---|---|---|---|---|---|---|
| $t_{DC}$ | DCK Cycle Time = **T** | 25 | | | ns | 1 |
| $t_{DH}$ | DCK HIGH Pulse Width = **H** | 12 | | | ns | |
| $t_{DL}$ | DCK LOW Pulse Width = **L** | 12 | | | ns | |
| $t_{DSS}$ | DSI Setup Time | 8 | **H** | | ns | 2 |
| $t_{DSH}$ | DSI Hold Time | 6 | **L** | | ns | |
| $t_{DSC}$ | DSI to Valid CDI | | 0 | | ns | 3 |
| $t_{DCS}$ | CDI Setup Time | 12 | T/2 | T-8 | ns | 4 |
| $t_{DCP}$ | CDI Bit Period | T | T | T | ns | |
| $t_{DDC}$ | DDC Cycle Time | 2T | 2T | 2T | ns | |
| $t_{DDH}$ | DDC HIGH Pulse Width | T | T | T | ns | |
| $t_{DDS}$ | DDC to DSO Time Delay | | | 6 | ns | |
| $t_{DSO}$ | DSO Pulse Width | T | T | T | ns | |
| $t_{DDP}$ | DDO Bit Period | 2T | 2T | 2T | ns | |
| $t_{DCD}$ | DDC LOW to Valid DDO | | | 6 | ns | 5 |
| $t_{DDD}$ | Valid CDI to Corresponding DDO | 35T | 35T | 35T | ns | 6 |
| $t_{DWL}$ | DDO Word Length | 24T | 24T | 24T | ns | |
| $t_{DDW}$ | DDO to Valid WT0-2 | | | 10 | ns | |

**NOTES:**
1) All times in nanoseconds.
2) DSI is clocked in on the falling edge of DCK.
3) $t_{DSC} = t_{DSH} - T + t_{DCS}$.
4) CDI is clocked in on the rising edge of DCK. CDI must be stable at least 12 ns before falling edge of DCK.
5) DDO is clocked out on the falling edge of DDC.
6) $t_{DDD}$ is approximately equal to 3 input codewords.

TABLE 5. DECODER AC ELECTRICAL CHARACTERISTICS.

## CODING PERFORMANCE AND FEATURES

A common measure of the performance of any coding scheme is the net coding gain achieved by using the code. Net coding gain is simply the difference between the signal-to-noise ratio (SNR) required on an uncoded channel and the SNR required for the same channel coded, with each channel delivering the same bit error rate (BER). The SNR is measured as the ratio of the energy per information bit (Eb) to the noise power per cycle of bandwidth (No). The 241203 Encoder/Decoder implements the half-rate Extended Golay code which has the capability of correcting up to three random errors per codeword and detecting four errors. The Extended Golay code is classified as a quasi-perfect code. A quasi-perfect code achieves optimal coding efficiency, i.e. the redundancy required to obtain the specified error correction/detection capability is equal to the theoretical upper bound.

Figure 9 shows the BER vs. SNR for a channel with and without the 241203 Encoder/Decoder. Note that the net coding gain varies with BER so that an accurate specification of net coding gain must also include the BER at which it is specified. The 241203 Encoder/Decoder achieves a 3dB net coding gain at a BER of one error per million. Figure 10 shows the BER on an encoded channel before decoding vs. the BER after decoding.The coding gain achieved through the use of forward error correcting can be utilized in different ways to improve the overall performance of the channel. For example, with the 3dB of net coding gain obtained by using the 241203 Encoder/Decoder, the radiated power at the source can be reduced by 3dB (i.e. cut in one-half) while still maintaining the same BER and throughput obtained before FEC. If transmission power is not a problem then the 3dB of net coding gain could be used to greatly improve the BER of the channel (by several orders of magnitude) while using the same uncoded channel transmission power and maintaining the same throughput. Note that since the implemented (24,12) Extended Golay code is a half-rate code, then twice the channel bandwidth is required to maintain the same data throughput.

The HYPER-FEC III encoder/decoder outputs the binary weight (# of errors) of the error pattern detected in each codeword. The error pattern weight reflects the quality of the transmission media and can be used to dynamically switch the encoding/decoding process in or out in order to maximize bandwidth efficiency. Switching the encoder out of the transmission link can easily be accomplished with the encoder bypass (EBP) control signal. When EBP is enabled, the encoder's uncoded data input (UDI) is connected directly to the encoder data output (EDO) pin. Similarly, when the decoder bypass (DBP) control signal is enabled, the decoder data output (DDO) is connected directly to the decoder data output (DDO) pin. A loopback enable control input is also provided to facilitate loopback testing by connecting the encoder data output (EDO) to the decoder data input (CDI).

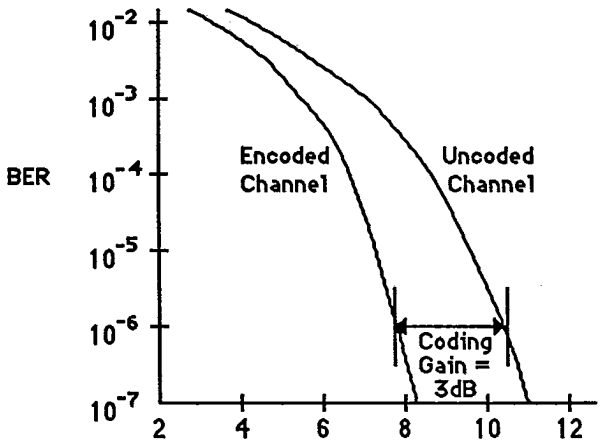



**FIGURE 9.** BER VS. SNR FOR A CHANNEL WITH AND WITHOUT (24,12) EXTENDED GOLAY CODING. ASSUMES AN AWGN* CHANNEL AND BPSK OR QPSK MODULATION.

*AWGN = ADDITIVE WHITE GAUSSIAN NOISE

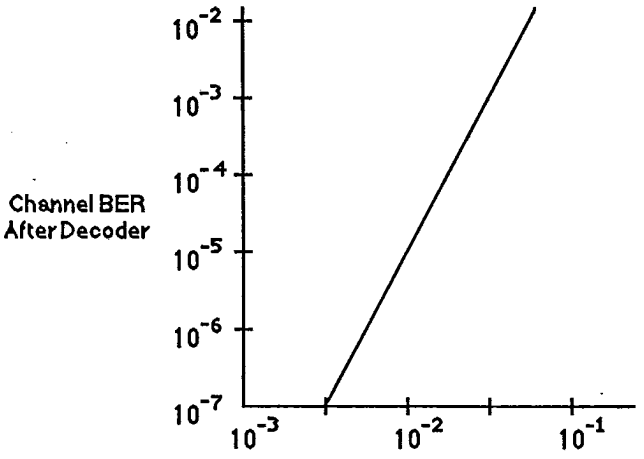



**FIGURE 10.** CHANNEL BER BEFORE DECODER VS. BER AFTER DECODER FOR (24,12) EXTENDED GOLAY CODING. ASSUMES AN AWGN* CHANNEL AND BPSK OR QPSK MODULATION.

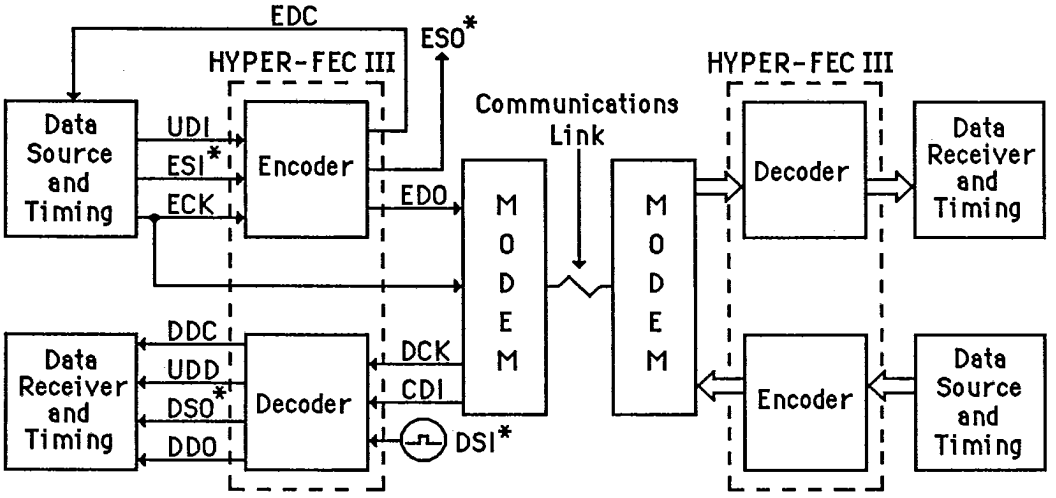
*AWGN = ADDITIVE WHITE GAUSSIAN NOISE

## APPLICATION NOTE

The Hyper-FEC III Encoder/Decoder provides the communication equipment designer with a simple and economical means to incorporate the Extended Golay (24,12) FEC code into both new and existing designs. Until now, incorporating the Extended Golay (24,12) FEC code, or any other multiple error correcting block code into a design meant adding a significant amount of complex MSI and LSI circuitry with its associated expense. This expense, in terms of of the added real estate and power required by the FEC circuitry and the increased cost of the product, (except in highly specialized applications) typically ruled out the incorporation of FEC into many designs. Incorporation of a complete FEC block coding system on a single, easy-to-use VLSI chip bypasses these expenses and now makes FEC a practical and economical reality for any type data link corrupted by bit errors.. This application note shows how the Hyper-FEC III chip can be easily incorporated in a communication link design. An example is given incorporating the Hyper-FEC III chip into a typical communication channel carrying synchronous 8-bit ASCII data. A companion application note on the chip, "Application Note 1: Theory, Performance and Application of the Hyper-FEC III VLSI Chip," discusses in detail the theory behind the code implemented by the chip and the performance improvement possible by using the chip.

The FEC encoding process is virtually transparent to any protocol or data format used by the channel. FEC coding can therefore be used with any type character or bit-oriented communication protocol (BISYNC, HDLC, SDLC, etc.) and any type of data format (synchronous, asynchronous, binary, ASCII, etc.).

The Hyper-FEC III chip is a completely self-contained encoder and decoder implementing the Extended Golay (24,12) code. As illustrated in Figure 11, the only input signals required by the encoder are the data input signal (UDI), and a clock signal (ECK) running at twice the input data rate. An optional sync input signal (ESI) can be inputted to the encoder to synchronize the codeword's 12-bit data block boundaries with the input data. Output signals from the encoder, in addition to the encoded data output signal (EDO), are the encoder data clock signal (EDC) running at the input data rate and an encoder sync output signal (ESO). The EDC signal is used to clock the data input (UDI) into the encoder and the ESO signal is used to identify codeword sync for optional use by external equipment. The encoded data (CDI), along with a clock synchronized and running at the encoded data rate (DCK), are the only input signals required by the decoder. The auto-sync feature built into the decoder automatically establishes codeword sync when two contiguous error free codewords are received by the decoder. The codewords used to establish synchronization are correctly decoded and are not lost.




* Optional signals available to the user

Figure 11. Incorporating the Hyper-FEC III Encoder/Decoder into the communication channel

An optional external codeword sync signal input (DSI) is provided on the chip to permit external synchronization of the decoder. An external sync signal overrides the operation of the built-in auto-sync circuitry. The decoder outputs decoded data (DDO) in a continuous serial bit stream format clocked at one-half the input encoded data rate. A decoded data clock (DDC) synchronized to the decoder data bit stream is also provided. The decoder sync output signal establishes the word boundaries between the outputted 12-bit data words.

The error correcting capability of the code (usually expressed in dB of coding gain) assumes that the bit errors occurring in the channel are statistically random and independent. Bit errors of this type occur in many types of communication channels due to the effects of additive white Gaussian noise (AWGN). Burst errors can also be corrected by using an interleaving scheme between the encoder and decoder. Data interleaving is a technique to randomize the burst errors by scattering the codeword bits in time so that burst errors are distributed across many codewords (A more detailed discussion of interleaving is discussed in Application Note 1). The de-interleaving process rearranges the received codeword bits before passing them on to the decoder. Interleaving can be designed to handle any size burst error pattern.

**EXAMPLE**

The following example illustrates the use of the Hyper-FEC III chip to improve the BER performance of a communication link carrying 8-bit ASCII data. The example makes use of the optional synchronization input signal of the encoder to format the data into one and one-half characters (12 data bits total) per codeword. This is desirable when working with data formatted in 8-bit bytes because reformatting the decoded serial output data from the decoder into the original 8 bits is simplified. It is also highly desireable if the user intends to establish external codeword sync using some type of control character or bit pattern (e.g. the ESC character is typically used for synchronization purposes when working with synchronous ASCII data blocks).

## APPLICATION NOTE (Continued)

### Encoder

Figures 12 and 13 illustrate the design of the encoder end of the communication link. The 8-bit ASCII characters are read out of an 8-bit parallel-to-serial register into the encoder data input (UDI). A clock (ECK) running at twice the uncoded data rate must also be provided to the encoder. ECK is divided by two inside the encoder to create a clock running at the data input rate (EDC). EDC is outputted by the encoder and used as the clock for the 8-bit parallel-to-serial register. It is also divided by eight to produce a parallel load pulse (LD) for the parallel-to-serial register. The LD pulse is divided by three to produce a codeword synchronization input signal (ESI) to the encoder. The codeword synchronization signal formats one-and-one-half characters into each codeword's 12-bit data block. Each codeword's data block thus has two phases; a phase where the data block (measured from LSB to MSB) consists of a full character followed by one-half character, and a phase where the data block consists of one-half character followed by a full character. The encoder generates 12 parity check bits based on the 12 input data bits and interleaves them with the data bits to form the 24-bit Extended Golay codeword. Each 24-bit codeword is then serially shifted out of the encoder by the ECK clock. The digital delay through the encoder, measured from the beginning of a 12-bit data block entering the encoder to when it first appears at the encoded data output, is twelve unencoded data bit-times.

### Decoder

Figure 14 shows the receiving end design incorporating the Hyper-FEC III chip decoder. The data codewords (CDI) from the modem are clocked into the decoder. A decoder input clock (DCK), synchronous with the input data, is also supplied to the decoder. This implementation shows how an optional external codeword sync recovery circuit may be incorporated. Since the original source information is not altered by the encoding process, an external sync circuit can be easily designed if a known sync pattern is inserted into the source data bit stream. ESC characters are normally used as sync characters when working with ASCII data. The external sync signal (DSI) overrides the internal sync circuitry. After a processing delay of 35 decoded data bit times (approximately three codewords), the decoded data is clocked out of the decoder by the decoded data clock (DDC). The DDO signal is clocked into a 24-bit serial-to-parallel shift register. In order to establish the 8-bit character boundaries for our ASCII data, the last sixteen bits of the register are examined for two contiguous ESC characters. When the ESC characters are detected, character sync and the correct codeword phase is established. The decoded data sync signal output (DSO) is divided by two to establish the load pulse for the 24-bit (three characters) holding register. Characters are then read from the holding register into the data receiver under control of the data receiver. Figure 14 illustrates the data receiver performing a shift-and-read operation on the holding register to input the characters into the data receiver.

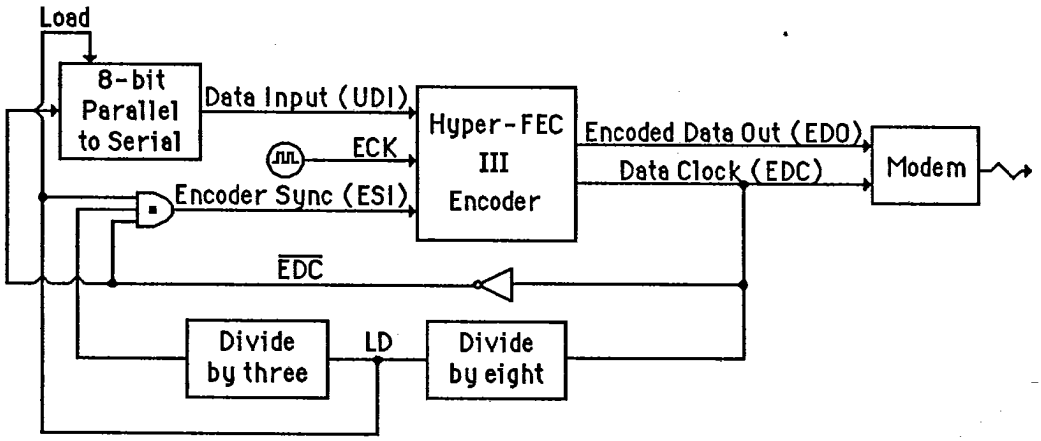



Figure 12 . Using the Hyper-FEC III Encoder to encode 8-bit character transmissions input rate (EDC).

## APPLICATION NOTE (Continued)

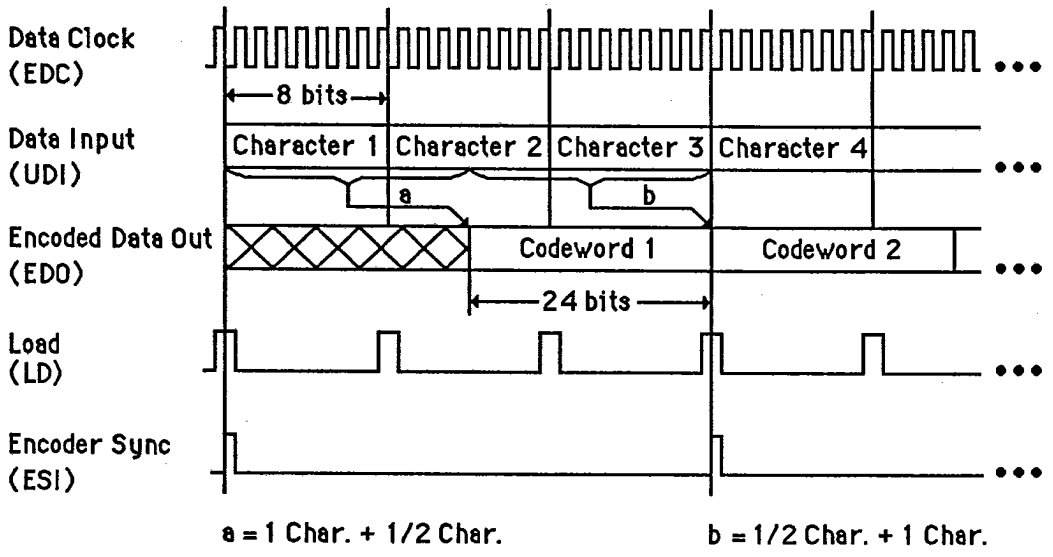



Figure 13. Timing for the Hyper-FEC III Encoder when encoding 8-bit character transmissions

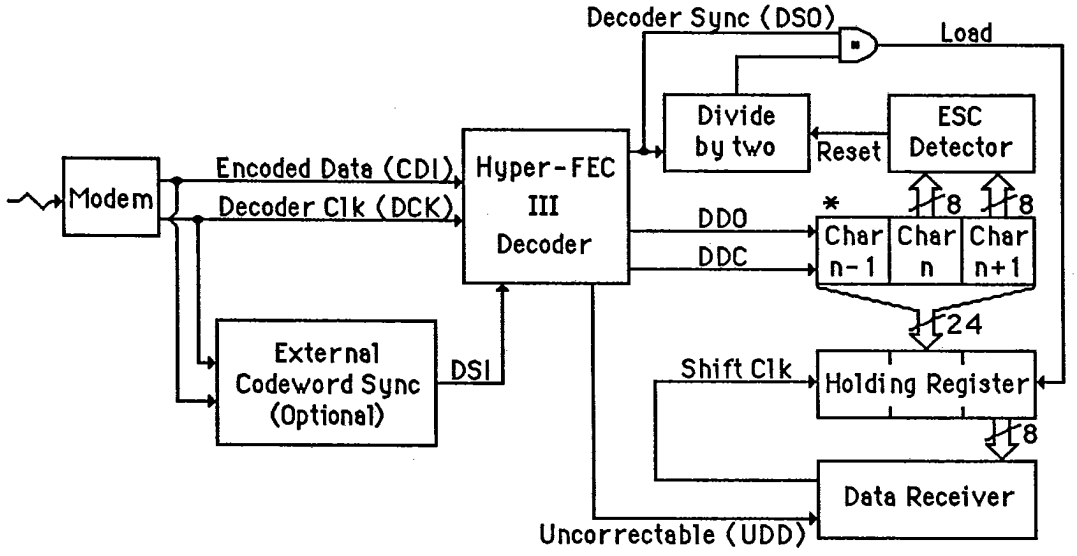



Figure 14. Using the Hyper-FEC III Decoder to decode the encoded 8-bit character.
Note: External Codeword Sync overrides the internal auto-sync, if used.

*24-bit Serial-to-Parallel Shift Register

**SPACE RESEARCH TECHNOLOGY, INC.**

1120 Capital of Texas Highway South
Building II, Suite 300
Austin, Texas 78746
Phone: (512) 329-1055
FAX: (512) 327-1274