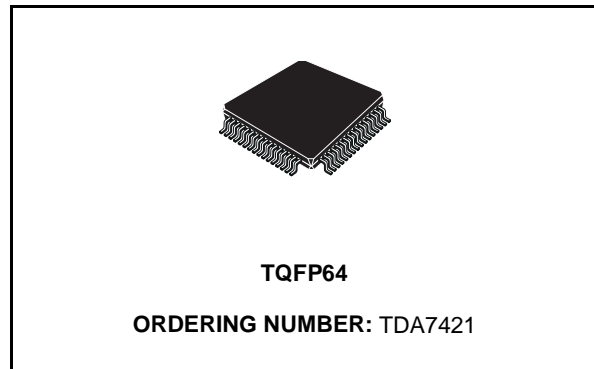




# TDA7421

## AM/FM TUNER FOR CAR RADIO AND Hi-Fi APPLICATIONS

- FRONT-END FOR AM/FM RECEIVERS
- UP-CONVERSION ARCHITECTURE FOR AM
- HIGH SPEED PLL WITH INLOCK DETECTOR FOR OPTIMIZED RDS APPLICATIONS
- SINGLE FREQUENCY REFERENCE FOR AM/FM
- AM/FM STATION DETECTOR
- $\mu$ P-CONTROLLED COMPENSATION OF EXTERNAL COMPONENTS SPREAD
- ADJUSTABLE AUDIO MUTE
- FULLY PROGRAMMABLE BY I<sup>2</sup>C BUS
- ADVANCED BICMOS TECHNOLOGY



### GENERAL DESCRIPTION

The TDA7421 is a high performance tuner circuit that integrates AM/FM sections, IF counter and PLL synthesizer on a single chip.

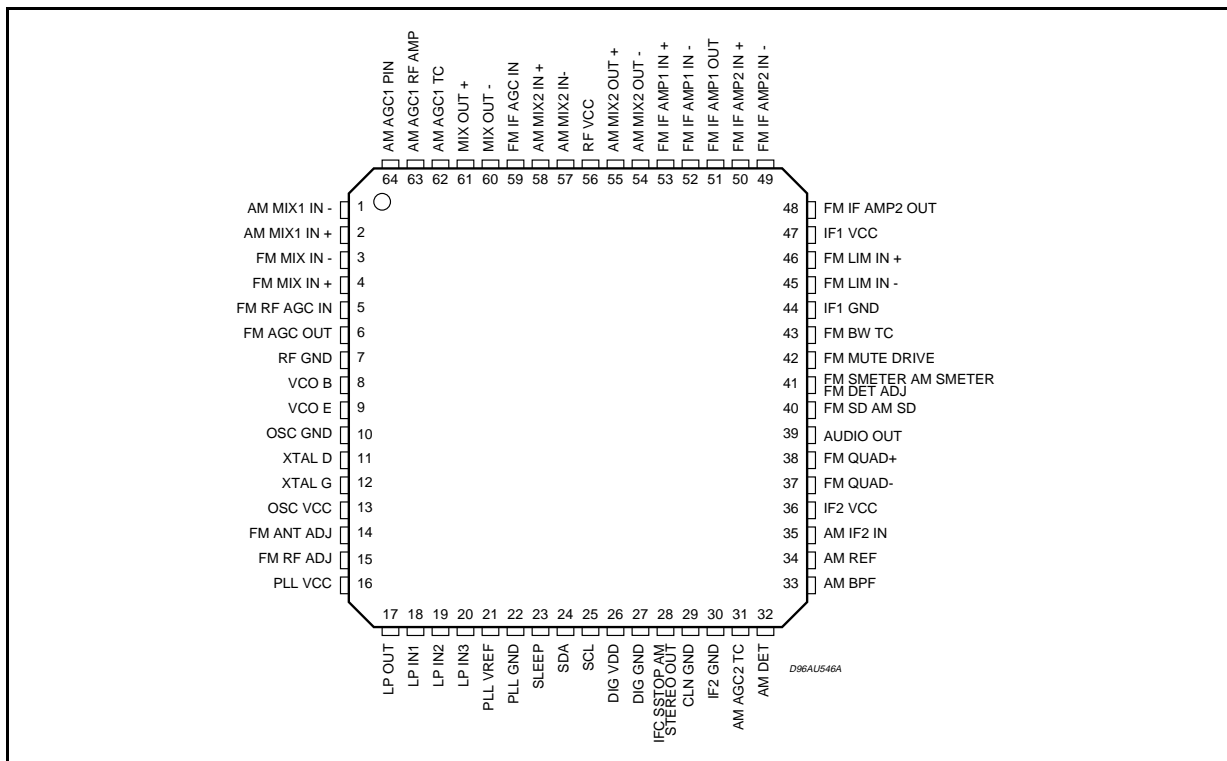
Use of BICMOS technology allows the implementation of tuning functions with a minimum of external components.

Value spread of external components can be fully

compensated by means of on-chip electrical adjustment controlled by external  $\mu$ P.

The Automatic Gain Control (AGC) operates on different sensitivities and bandwidths in order to improve sensitivity and dynamic range. I<sup>2</sup>C bus allows to control selected functions of the tuner (AGC and amplifiers gain, PLL and counters operation modes).

### PINS CONNECTION





**ABSOLUTE MAXIMUM RATINGS**

Symbol	Parameter	Value	Unit
T <sub>amb</sub>	Operating Temperature Range	-40 to 85	°C
T <sub>stg</sub>	Storage Temperature Range	-55 to 150	°C
V <sub>CC</sub>	Analog Supply Voltages (PLL, RF, IF1, IF2, OSC)	10.2	V
V <sub>DD</sub>	Digital Supply Voltage	5.5	V

**THERMAL DATA**

Symbol	Parameter	Value	Unit
R <sub>th j-amb</sub>	Thermal resistance Junction-Ambient	typ. 68	°C/W

**PIN DESCRIPTION**

N.	Name	Function
1	AM MIX1 IN -	Input "-" to the AM 1st mixer (differential input)
2	AM MIX1 IN +	Input "+" to the AM 1st mixer (differential input)
3	FM MIX IN -	Input "-" to the FM mixer (differential input)
4	FM MIX IN +	Input "+" to the FM mixer (differential input)
5	FM RF AGC IN	Input to the RF AGC circuit
6	FM AGC OUT	Voltage output to the FM AGC
7	RF GND	RF circuits ground
8	VCO B	Local oscillator input to the transistor base (two-pin oscillator)
9	VCO E	Local oscillator input to the transistor emitter (two-pin oscillator)
10	OSC GND	Oscillator ground
11	XTAL D	Crystal oscillator input to MOS drain (two-pin oscillator)
12	XTAL G	Crystal oscillator input to MOS gate (two-pin oscillator)
13	OSC VCC	Oscillator positive supply
14	FM ANT ADJ	Tuning varicap voltage for antenna FM filter
15	FM RF ADJ	Tuning varicap voltage for RF FM filter
16	PLL VCC	PLL positive supply
17	LP OUT	Op Amp output to PLL loop filters
18	LP IN1	PLL "N. 1" loop filter connection to Op Amp inverting input
19	LP IN2	PLL "N. 2" loop filter connection to Op Amp inverting input
20	LP IN3	PLL "N. 3" loop filter connection to Op Amp inverting input
21	PLL VREF	Voltage reference to Op Amp noninverting input
22	PLL GND	PLL ground
23	SLEEP	I <sup>2</sup> C bus disconnect signal
24	SDA	I <sup>2</sup> C bus data
25	SCL	I <sup>2</sup> C bus clock

## TDA7421

### PIN DESCRIPTION (continued)

N.	Name	Function
27	DIG GND	Digital circuits ground
28(*)	IFC SSTOP AM STEREO OUT	Search stop signal or Output (single ended) of AM IF amplifier
29	CLN GND	"Clean" ground
30	IF2 GND	IF 2nd ground
31	AM AGC2 TC	AM 2nd AGC time constant
32	AM DET	Connection to the capacitor of the AM diode-capacitor detector
33	AM BPF	Connection to the AM IF filter
34	AM REF	Reference voltage of AM IF amplifier
35	AM IF2 in	Input (single ended) of AM 2nd IF amplifier
36	IF2 VCC	IF 2nd positive supply
37	FM QUOD -	"-" Insertion pt. of FM quadrature network (differential)
38	FM QUAD +	"+" Insertion pt. of FM quadrature network (differential)
39	AUDIO OUT	Audio frequency output (single ended)
40 (*)	FM SD AM SD	FM Station detector output or AM Station detector output
41(*)	FM SMETER AM SMETER FM DET ADJ	FM S-meter output or AM S-meter output or FM detuning adjustment
42	FM MUTE DRIVE	FM mute time constant
43	FM BW TC	FM detuning detector time constant
44	IF1 GND	IF 1st ground
45	FM LIM IN -	Input "-" of FM limiter (differential input)
46	FM LIM IN +	Input "+" of FM limiter (differential input)
47	IF1 VCC	IF 1st positive supply
48	FM IF AMP2 OUT	Output (single ended) of the FM IF 2nd amplifier buffer
49	FM IF AMP2 IN -	Input "-" of the FM IF 2nd amplifier (differential input)
50	FM IF AMP2 IN +	Input "+" of the FM IF 2nd amplifier (differential input)
51	FM IF AMP1 OUT	Output (single ended) of the FM IF 1st amplifier buffer
52	FM IF AMP1 IN -	Input "-" of the FM IF 1st amplifier (differential input)
53	FM IF AMP1 IN +	Input "+" of the FM IF 1st amplifier (differential input)
54	AM MIX2 OUT -	Output "-" of the AM 2nd mixer (differential output)
55	AM MIX2 OUT +	Output "+" of the AM 2nd mixer (differential output)
56	RF VCC	RF stage positive supply
57	AM MIX2 IN -	Input "-" to the AM 2nd mixer (differential input)
58	AM MIX2 IN +	Input "+" to the AM 2nd mixer (differential input)
59	FM IF AGC IN	Input FM IF AGC circuit
60	MIX OUT -	Output "-" of the FM/AM 1st mixer (differential output)
61	MIX OUT +	Output "+" of the FM/AM 1st mixer (differential output)
62	AM AGC1 TC	AM 1st AGC time constant
63	AM AGC1 RF AMP	Voltage output of the AM 1st AGC, to the transistor of the RF AF amplifier
64	AM AGC1 PIN	Current output of the AM 1st AGC, to the PIN diodes antenna AM attenuator

(\*) Pin function is user-defined by software.

**ELECTRICAL CHARACTERISTICS****DC PARAMETERS** ( $T_{amb} = 25^{\circ}\text{C}$ ;  $V_{cc} = 8.5\text{V}$ ,  $V_{dd} = 5\text{V}$  unless otherwise specified)

Symbol	Parameter	Test Condition	Min.	Typ.	Max.	Unit
DIG $V_{dd}$	Digital Supply Voltage		4.75		5.25	V
DIG $I_{dd}$	Digital Supply Current	AM MODE	4.0	4.6	5.2	mA
		FM MODE	3.5	4.0	4.5	mA
PLL $V_{cc}$	PLL Supply Voltage		7.5		10	V
PLL $I_{cc}$	PLL Supply Current	AM MODE	1.2	1.6	2.0	mA
		FM MODE	2.5	3.0	3.5	mA
RF $V_{cc}$	RF Supply Voltage		7.5		10	V
RF $I_{cc}$	RF Supply Current	AM MODE	15.0	17.5	20.0	mA
		FM MODE	10.0	13.0	16.0	mA
IF1 $V_{cc}$	IF1 Supply Voltage		7.5		10	V
IF1 $I_{cc}$	IF1 Supply Current	AM MODE	2.2	2.7	3.2	mA
		FM MODE	16.0	19.5	23.0	mA
IF2 $V_{cc}$	IF2 Supply Voltage		7.5		10	V
IF2 $I_{cc}$	IF2 Supply Current	AM MODE	8.5	10.5	12.5	mA
		FM MODE	27.0	32.0	37.0	mA
OSC $V_{cc}$	Oscillator Supply Voltage		7.5		10	V
OSC $I_{cc}$	Oscillator Supply Current	AM MODE	14.5	17.0	19.5	mA
		FM MODE	11.0	14.0	17.0	mA
TOTAL $I_{cc}$	Total Supply Current	AM MODE	45.0	50.0	55.0	mA
		FM MODE	73.0	81.0	89.0	mA

**AC PARAMETERS**Ref: FM Test Circuit measure  $V_{osc}$  with high impedance FET probe**Voltage Controlled Oscillator (VCO)**

Symbol	Parameter	Test Condition	Min.	Typ.	Max.	Uni
$f_{VCOmin}$	Minimum VCO Frequency	$V_{turn} = 0$ , Europe/USA Japan		80.9 55	98.2 65.4	MHz MHz
$f_{VCOMax}$	Maximum VCO Frequency	$V_{turn} = V_{cc}$ , Europe/USA Japan	123.2 79.2	128 90		MHz MHz
$V_{osc}$	Oscillator Amplitude	$f_{osc} = 108.8\text{MHz}$ , Europe/USA $f_{osc} = 72.3\text{MHz}$ , Japan		106		dBu

**Reference Oscillator**Ref: AM Test Circuit measure  $V_{XTAL}$  with high impedance FET probe

Symbol	Parameter	Test Condition	Min.	Typ.	Max.	Uni
$f_{XTAL}$	Reference Frequency			10.25		MHz
$V_{XTAL}$	Oscillator Amplitude			108		dBu

**ELECTRICAL CHARACTERISTICS** (continued)**FM Section Global Performances**

Refer to Evaluation Circuit and enclosed curves (S+N/N, THD)

- RF Input:  $f_c = 98.1\text{MHz}$ , 75KHz dev., 1KHz mod., 60dBu

- Audio Output: BPF 20Hz - 20KHz

Symbol	Parameter	Test Condition	Min.	Typ.	Max.	Uni
S+N/N	Signal to Noise Ratio			68		dB
THD	Total Harmonic Distortion	deviation = 40KHz		0.3		%
$V_{OAF}$	Audio Output Level		350	400	450	mV <sub>RMS</sub>
US	Usable Sensitivity	antenna level at which S+N/N=30dB		4		dBu
AGC <sub>range</sub>	Range AGC FM		65			dB

**FM Front-end Electrical Adjustments**Ref: FM Test Circuit measure  $V_{ANTADJ}$  and  $V_{RFADJ}$  referred to  $V_{PLLOUT}$ 

Symbol	Parameter	Test Condition	Min.	Typ.	Max.	Uni
ANTADJ MAX OFF	Maximum FM Antenna Filter Adjustment Voltage Offset	$V_{PLLOUT} = 2.5\text{V}$ , ANA3-0 set to 1111	21	25	27	%
ANTADJ STEP OFF	FM Antenna Filter Adjustment Voltage Offset Step	$V_{PLLOUT} = 2.5\text{V}$ , ANA3-0 set to 1001	2.8	3.6	4.4	%
RFADJ MAX OFF	Maximum FM RF Filter Adjustment Voltage Offset	$V_{PLLOUT} = 2.5\text{V}$ , RFA3-0 set to 1111	21	25	27	%
RFADJ STEP OFF	FM RF Filter Adjustment Voltage Offset Step	$V_{PLLOUT} = 2.5\text{V}$ , RFA3-0 set to 1001	2.8	3.6	4.4	%

**FM Mixer**Ref: FM Test Circuit, measure input at  $V_{MIXFMIN}$ , output at  $V_{MIXOUT}$ 

Symbol	Parameter	Test Condition	Min.	Typ.	Max.	Unit
$Z_{IN,MIX}$	Single-ended input impedance (pin 3, pin4)	$f = 100\text{MHz}$		12		$\Omega$
$G_{MIX}$	Conversion Gain	$f_{IN} = 98.1\text{MHz}$		21.8		dB
$IP3_{MIX}$	3rd order intermodulation distortion intercept point	$f_d = 98.1\text{MHz}$ ; $f_{u1} = 98.2\text{MHz}$ ; $f_{u2} = 98.3\text{MHz}$ ;		104		dBu
$CP1_{MIX}$	1dB compression point	$f_{IN} = 98.1\text{MHz}$		90		dBu

**FM AGC**Ref: FM Test Circuit, measure input at  $V_{FMRFAGCIN}$ , and  $V_{FMIFAGCIN}$ , output at  $V_{FMAGCOUT}$ 

Symbol	Parameter	Test Condition	Min.	Typ.	Max.	Unit
$V_{RFAGCSTART}$	Open Loop Rf Agc Starting Point	$f_{RFAGCIN} = 98.1\text{MHz}$ Value of $V_{FMRFAGCIN}$ , at which $V_{FMAGCOUT} = 4\text{V}$	74	80	86	dBu
$R_{INRFAGC}$	Input Resistance			20		K $\Omega$
$V_{IFAGCSTART}$	Open Loop If Agc Starting Point	$f_{IFAGCIN} = 10.7\text{MHz}$ Value of $V_{FMIFAGCIN}$ , at which $V_{FMAGCOUT} = 4\text{V}$ FAGC2-0 set to 111	71	77	83	dBu
$R_{INIFAGC}$	Input Resistance			20		K $\Omega$
$R_{OUTFMAGC}$	Output Resistance			10		K $\Omega$

**ELECTRICAL CHARACTERISTICS** (continued)**FM IF Amplifier 1**

Ref: FM Test Circuit, measure input at VFMAMP1IN, output at VFMAMP1OUT

Symbol	Parameter	Test Condition	Min.	Typ.	Max.	Unit
R <sub>IN,AMP1</sub>	Input Resistance	f = 10.7MHz		330		Ω
R <sub>OUT,AMP1</sub>	Output Resistance	f = 10.7MHz		330		Ω
G <sub>TYP,AMP1</sub>	Typical Gain	f <sub>IN</sub> = 10.7MHz, FBH3-0 set to 0100	16.5	17.5	18.5	dB
G <sub>MIN,AMP1</sub>	Minimum Gain	f <sub>IN</sub> = 10.7MHz, FBH3-0 set to 0001	14.5	15.5	16.5	dB
G <sub>MAX,AMP1</sub>	Maximum Gain	f <sub>IN</sub> = 10.7MHz, FBH3-0 set to 0000	18.5	19.5	20.5	dB
IP3 <sub>AMP1</sub>	3rd Order Intermodulation Distortion Intercept Point	f <sub>d</sub> = 10.7MHz; f <sub>u1</sub> = 10.8MHz; f <sub>u2</sub> = 10.9MHz, FBH3-0 set to 0100		109		dBu
CP1 <sub>AMP1</sub>	1dB Compression Point	f <sub>IN</sub> = 10.7MHz; FBH3-0 set to 0100		96		dBu

**FM IF Amplifier 2**

Ref: FM Test Circuit, measure input at VFMAMP2IN, output at VFMAMP2OUT

Symbol	Parameter	Test Condition	Min.	Typ.	Max.	Unit
R <sub>IN,AMP2</sub>	Input Resistance	f = 10.7MHz		330		Ω
R <sub>OUT,AMP2</sub>	Output Resistance	f = 10.7MHz		330		Ω
G <sub>TYP,AMP2</sub>	Typical Gain	f <sub>IN</sub> = 10.7MHz, FBL3-0 set to 0100	5	6	7	dB
G <sub>MIN,AMP2</sub>	Minimum Gain	f <sub>IN</sub> = 10.7MHz, FBL3-0 set to 0001	3	4	5	dB
G <sub>MAX,AMP2</sub>	Maximum Gain	f <sub>IN</sub> = 10.7MHz, FBL3-0 set to 0000	7	8	9	dB
IP3 <sub>AMP2</sub>	3rd Order Intermodulation Distortion Intercept Point	f <sub>d</sub> = 10.7MHz; f <sub>u1</sub> = 10.8MHz; f <sub>u2</sub> = 10.9MHz, FBL3-0 set to 0100		122		dBu
CP1 <sub>AMP2</sub>	1dB Compression Point	f <sub>IN</sub> = 10.7MHz; FBL3-0 set to 0100		110		dBu

**FM Limiter, Field Strength Meter and Demodulator**

Ref: FM Test circuit, measure:

- Input at VFMLIMIN, f<sub>IN</sub> = 10.7MHz
- filtered FS Meter output at V<sub>SM,FILT</sub>
- shifted FS Meter output at V<sub>SM,SHIFT</sub> (FMADJ set to 0)
- demodulator adjustment output at V<sub>SM,SHIFT</sub> (FMADJ set to 1)

Symbol	Parameter	Test Condition	Min.	Typ.	Max.	Unit
R <sub>IN,LIM</sub>	Limiter Input Resistance			330		Ω
G <sub>LIM</sub>	Limiter Gain			90		dB
LS	Limiting Sensitivity			23		dBu
SM1	Smeter 1 at V <sub>SM,FILT</sub>	VFMLIMIN = 42dBu	0.1 <sup>(1)</sup>	0.25	0.5 <sup>(1)</sup>	V
SM2	Smeter 2 at V <sub>SM,FILT</sub>	VFMLIMIN = 77dBu	2.4 <sup>(1)</sup>	2.75	3.1 <sup>(1)</sup>	V
SM3	Smeter 3 at V <sub>SM,FILT</sub>	VFMLIMIN = 102dBu	4.0 <sup>(1)</sup>	4.35	4.7 <sup>(1)</sup>	V
SM <sub>MINSHIFT</sub>	Smeter Minimum Shift Voltage at V <sub>SM,SHIFT</sub> referred to V <sub>SM,FILT</sub>	VFMLIMIN = 70dBu, FSL4-0 set to 00000	0.25	0.3	0.35	V
SM <sub>MAXSHIFT</sub>	Smeter Maximum Shift Voltage at V <sub>SM,SHIFT</sub> referred to V <sub>SM,FILT</sub>	VFMLIMIN = 70dBu, FSL4-0 set to 11111	1.55	1.8	2.05	V
G <sub>DEM</sub>	Demodulator Conversion Gain	VFMLIMIN > LS		2		mV <sub>RMS</sub> /KHz
G <sub>DEMADJ</sub>	Demodulator Adjustment Conversion Gain	VFMLIMIN > LS, measured at V <sub>SM,SHIFT</sub> , FMADJ set to 1		14		mV <sub>RMS</sub> /KHz

NOTE1: Refer to Global application circuit; input at first Ceramic Filter in, FBH3-0 set to 0001, FBL3-0 set to 0001

**ELECTRICAL CHARACTERISTICS** (continued)**FM Audio Amplifier**

Ref: FM Test circuit, measure:

- Input at  $V_{FMLIMIN}$ , = 95dBu,  $f_{in}$  = 10.7MHz
- audio output at  $V_{AUDIO}$ , BPF 20Hz to 20KHz
- muting voltage at  $V_{MUTE, DRIVE}$

Symbol	Parameter	Test Condition	Min.	Typ.	Max.	Unit
$V_{MUTE}$	Mute Voltage	$V_{MUTE,DRIVE}$ for which $\Delta V_{AF} = -29dB$ , FMHIGH set to 0, AUM2-0 set to 111	2			V
$V_{PLAY}$	Play Voltage	$V_{MUTE,DRIVE}$ for which $\Delta V_{AF} = -1dB$ , FMHIGH set to 0, AUM2-0 set to 111			0.3	V
$G_{AMP,PLAY}$	Audio Amplifier Gain in Play Conditions	$V_{MUTE,DRIVE} < V_{PLAY}$		9		dB
$G_{AMP,MUTEMAX}$	Audio Amplifier Highest Gain in Mute Condition	$V_{MUTE,DRIVE} > V_{MUTE}$ , FMHIGH set to 1, AUM2-0 set to 001		6.5		dB
$G_{AMP,MUTEMIN}$	Audio Amplifier Lowest Gain in Mute Condition	$V_{MUTE,DRIVE} > V_{MUTE}$ , FMHIGH set to 0, AUM2-0 set to 111		-21		dB
$V_{AF}$	AF Output Level	$f_{DEV} = 75KHz$ , $f_{MOD} = 1KHz$ , $V_{MUTE,DRIVE} < V_{MUTE}$	350 <sup>(1)</sup>	400	450 <sup>(1)</sup>	mV <sub>RMS</sub>
THD	AFTotal Harmonic distortion	$f_{DEV} = 75KHz$ , $f_{MOD} = 1KHz$ , $V_{MUTE,DRIVE} < V_{MUTE}$		0.5		%
S+N/N	AF Signal to Noise Ratio	$f_{DEV} = 75KHz$ , $f_{MOD} = 1KHz$ , $V_{MUTE,DRIVE} < V_{MUTE}$	68 <sup>(1)</sup>	75		%
AMR	Amplitude Modulation Rejection	AM modulation depth 30%, $f_{MOD} = 1KHz$ , with respect to FM modulated signal with $f_{DEV} = 40KHz$ , $V_{MUTE,DRIVE} < V_{MUTE}$	60 <sup>(1)</sup>	67		dB
AUDIO <sub>curr</sub>	Audio Out Current Capability		5			mA
MUTE R <sub>out</sub>	Mute Drive Output Resistance			1		K $\Omega$

NOTE1: Refer to Global application circuit; input at first Ceramic Filter in, FBH3-0 set to 0001, FBL3-0 set to 0001

**FM QUALITY DETECTORS****Field Strength Detector**

Ref: FM Test Circuit, measure:

- Input at  $V_{FMLIMIN}$ ,  $f_{in}$  = 10.7MHz, CW
- output at  $V_{MUTE,DRIVE}$

Symbol	Parameter	Test Condition	Min.	Typ.	Max.	Unit
FSD <sub>MIN</sub>	Field Strength Detector Minimum Threshold	$V_{FMLIMIN}$ level at which $V_{MUTE,DRIVE} = V_{MUTE}$ , FSM3-0 set to 0000		40		dBu
FSD <sub>MAX</sub>	Field Strength Detector Maximum	$V_{FMLIMIN}$ level at which $V_{MUTE,DRIVE} = V_{MUTE}$ , FSM3-0 set to 1111		60		dBu



**ELECTRICAL CHARACTERISTICS** (continued)**Detuning Detector**

Ref: FM Test Circuit, measure:

- Inputs at VFMLIMIN, CW

- output at VMUTE,DRIVE

Symbol	Parameter	Test Condition	Min.	Typ.	Max.	Unit
DDSTART	Detuning Detector Starting Point	frequency shift from 10.7MHz at which VMUTE,DRIVE = VPLAY		±23		KHz
DDSLOPE,MIN	Detuning Detector Minimum Muting Slope	frequency shift from 10.7MHz + DDSTART, at which VMUTE,DRIVE = VMUTE, BWM2-0 set to 100, FMRECSEEK set to 0	22.5	30	37.5	KHz
DDSLOPE,MAX	Detuning Detector Maximum Muting Slope	frequency shift from 10.7MHz + DDSTART, at which VMUTE,DRIVE = VMUTE, BWM2-0 set to 001, FMRECSEEK set to 0	7.5	10	12.5	KHz
DDTRC	Detuning Detector Time Constant Ratio	ratio of "reception" mode integration time constant inside the Detuning Detector with respect to "seek" mode		34/6		s/s

**Adjacent Channel Detector**

Ref: FM Test Circuit, measure:

- Inputs at VFMLIMIN: desired 10.7MHz, 95dBu CW; undesired 10.8MHz CW

- output at VMUTE,DRIVE

- BWM2-0 set to 001

Symbol	Parameter	Test Condition	Min.	Typ.	Max.	Unit
ACD <sub>MAX</sub>	Adjacent Channel Quality Detector Maximum Sensitivity Threshold	amplitude of undesired signal at which VMUTE,DRIVE = VMUTE, HDM4-0 set to 11111		91		dBu
ACD <sub>MIN</sub>	Adjacent Channel Quality Detector Minimum Sensitivity Threshold	amplitude of undesired signal at which VMUTE,DRIVE = VMUTE, HDM4-0 set to 00000		94.8		dBu

**Field Strength Station Detector**

Ref: FM Test Circuit, measure:

- Inputs at VFMLIMIN: desired 10.7MHz, CW

- output at VFMSD

- FMRECSEEK set to 1

Symbol	Parameter	Test Condition	Min.	Typ.	Max.	Unit
FSSD <sub>MIN</sub>	Field Strength Station Detector Minimum Threshold	VFMLIMIN level at which VFMSD = 2.5, FSM4-0 set to 00000		24		dBu
FSSD <sub>MAX</sub>	Field Strength Station Detector Maximum Threshold	VFMLIMIN level at which VFMSD = 2.5, FSM4-0 set to 11111		76		dBu

**Detuning Station Detector**

Ref: FM Test Circuit, measure:

- Input at VFMLIMIN, CW;

- output at VFMSD

- FMRECSEEK set to 1

Symbol	Parameter	Test Condition	Min.	Typ.	Max.	Unit
DSD	Detuning Station Detector Threshold	frequency shift from 10.7MHz at which VFMSD = 2.5V		23		KHz

**ELECTRICAL CHARACTERISTICS** (continued)**Adjacent Channel Station Detector**

Ref: FM Test Circuit, measure:

- Input at  $V_{FMLIMIN}$ : desired 10.7MHz, 95dBu CW; undesired 10.8MHz CW
- output at  $V_{FMDS}$
- FMRECSEEK set to 1

Symbol	Parameter	Test Condition	Min.	Typ.	Max.	Unit
ACSD <sub>MAX</sub>	Adjacent Channel Detector Maximum Sensitivity Threshold	amplitude of undesired signal at which $V_{FMDS} = 2.5V$ , HDM4-0 set to 11111		92.5		dBu
ACD <sub>MIN</sub>	Adjacent Channel Detector Minimum Sensitivity Threshold	amplitude of undesired signal at which $V_{FMDS} = 2.5V$ , HDM4-0 set to 00000		94.9		dBu

**AM Section Global Performances**

Refer to Evaluation Circuit and enclosed curves (S+N/N, THD)

- RF Input:  $f_c = 1MHz$ ,  $f_{mod} = 1KHz$ ,  $m = 0.3$ ;
- Audio Output: BPF 20Hz - 20KHz

Symbol	Parameter	Test Condition	Min.	Typ.	Max.	Unit
$V_{IN\ MIN}$	Maximum Sensitivity	$V_{INRF} = 74dBu$ ; $\Delta V_{AF} = -20dB$		20		dBu
$V_{IN\ US}$	Usable Sensitivity	S+N/N = 20dB		31		dBu
$\Delta V_{is}$	AGC Range	$V_{INRF} = 74dBu$ ; $\Delta V_{AF} = -10dB$		50		dB
S+N/N	Signal to Noise Ratio	$V_{INRF} = 74dBu$	46.0	53.0		dB
$\alpha_{IMAG}$	Image Rejection	$f_1 = 1.9MHz$ $f_2 = 22.4MHz$				dB
$\alpha_{TW}$	Tweet	$V_{INRF} = 74dBu$ ; $f_1 = 900KHz$ ; $f_2 = 1350KHz$		1.2		dB
THD	Total Harmonic Distortion	$V_{INRF} = 74dBu$ ; $m = 0.3$		0.45	1.0	%
		$V_{INRF} = 74dBu$ ; $m = 0.8$		1.73		%
		$V_{INRF} = 120dBu$ ; $m = 0.3$		0.33		%
$V_{AF}$	Audio Output Level	$V_{INRF} = 74dBu$	137	167	197	mV <sub>RMS</sub>
$V_{AMST}$	AM IF2 Output level	$V_{INRF} = 74dBu$		106		dBu

**AM Mixer 1**Ref: AM Test Circuit, measure input at  $V_{MIX2AMIN}$ , output at  $V_{MIXOUT}$ 

Symbol	Parameter	Test Condition	Min.	Typ.	Max.	Unit
R <sub>INMIX1</sub>	Input Resistance			1.2		K $\Omega$
G <sub>MIX1</sub>	Conversion Gain	$f_{IN} = 1MHz$	7.5	8.5	9.5	dB
IP3 <sub>MIX1</sub>	3rd Order Intermodulation Distortion Intercept Point	$f_d = 1MHz$ ; $f_{u1} = 1.1MHz$ ; $f_{u2} = 1.2MHz$ ;		115		dBu
CP1 <sub>MIX1</sub>	1dB Compression Point	$f_{IN} = 1MHz$		98.7		dBu

**ELECTRICAL CHARACTERISTICS** (continued)**AM Wide & Narrow AGC**Ref: AM Test Circuit, input at  $V_{MIX1AMIN}$ , and  $V_{MIX2AMIN}$ , output at  $V_{AMAGC1AMP}$ , and  $V_{AMAGC1PIN}$ 

Symbol	Parameter	Test Condition	Min.	Typ.	Max.	Unit
$V_{WAGCTYP}$	Open Loop WIDE AGC Typical Starting Point	$f_{WAGCIN} = 1\text{MHz}$ , AAG3-0 set to 1000; $V_{MIX1AMIN}$ at which $V_{AMAGC1AMP} = 2.5\text{V}$		91.3		dBu
$V_{WAGCMIN}$	Open Loop WIDE AGC Minimum Starting Point	$f_{WAGCIN} = 1\text{MHz}$ , AAG3-0 set to 0000; $V_{MIX1AMIN}$ at which $V_{AMAGC1AMP} = 2.5\text{V}$		80.6		dBu
$V_{WAGCMAX}$	Open Loop WIDE AGC Maximum Starting Point	$f_{WAGCIN} = 1\text{MHz}$ , AAG3-0 set to 1111; $V_{MIX1AMIN}$ at which $V_{AMAGC1AMP} = 2.5\text{V}$		95.6		dBu
$V_{NAGCTYP}$	Open Loop NARROW AGC Typical Starting Point	$f_{NAGCIN} = 10.7\text{MHz}$ , AAG3-0 set to 1000; $V_{MIX2AMIN}$ at which $V_{AMAGC1AMP} = 2.5\text{V}$		93.2		dBu
$V_{NAGCMIN}$	Open Loop NARROW AGC Minimum Starting Point	$f_{NAGCIN} = 10.7\text{MHz}$ , AAG3-0 set to 0000; $V_{MIX2AMIN}$ at which $V_{AMAGC1AMP} = 2.5\text{V}$		82.8		dBu
$V_{NAGCMAX}$	Open Loop NARROW AGC Maximum Starting Point	$f_{NAGCIN} = 10.7\text{MHz}$ , AAG3-0 set to 1111; $V_{MIX2AMIN}$ at which $V_{AMAGC1AMP} = 2.5\text{V}$		97.4		dBu
$R_{OUTAMAGC1}$	Output Resistance			23.3		$\text{K}\Omega$
$I_{AMAGC1PIN}$	Maximum Pin-diode Current	$f_{WAGCIN} = 1\text{MHz}$ ; $V_{MIX1AMIN} = 90\text{dBu}$ ; AAG3-0 set to 0000		1.4		mA

**AM Mixer 2**Ref: AM Test Circuit, measure input at  $V_{MIX2AMIN}$ , output at  $V_{MIX2OUT}$ , (switches must be in position 2 for AGC measurements).

Symbol	Parameter	Test Condition	Min.	Typ.	Max.	Unit
$R_{INMIX2}$	Input Resistance			5		$\text{K}\Omega$
$G_{MIX2}$	Maximum conversion Gain	$f_{IN} = 10.7\text{MHz}$		19.6		dB
$IP3_{MIX2}$	3rd Order Intermodulation Distortion Intercept Point	$f_d = 10.7\text{MHz}$ ; $f_{u1} = 10.8\text{MHz}$ ; $f_{u2} = 10.9\text{MHz}$ ;		122		dBu
$CP1_{MIX2}$	1dB Compression Point	$f_{IN} = 10.7\text{MHz}$		90.7		dBu
$AGC_{MIXCP}$	Central Point of AGC2 Intervention on Mixer 2	$f_{IN} = 10.7\text{MHz}$ ; $V_{MIX2AMIN} = 52\text{dBu}$ ; Value of $V_{MIX2OUT}$		61.2		dBu
$AGC_{MIXSP}$	AGC2 Starting Point on Mixer 2	$f_{IN} = 10.7\text{MHz}$ ; Value of $V_{MIX2AMIN}$ for which $V_{MIX2OUT}$ is $AGC_{MIXCP} - 3\text{dB}$		40		dBu
$AGC_{MIXR}$	AGC2 Range on Mixer 2	$f_{IN} = 10.7\text{MHz}$ ; Range of $V_{MIX2AMIN}$ for which $V_{MIX2OUT}$ is $AGC_{MIXCP} \pm 3\text{dB}$		24		dB

**ELECTRICAL CHARACTERISTICS** (continued)**AM IF2 Amplifier**

Ref: AM Test Circuit, measure input at VIP2AMPIN, output at VIP2AMPOUT, (switches must be in position 1),  
 $f_{IN} = 450\text{KHz}$ .

Symbol	Parameter	Test Condition	Min.	Typ.	Max.	Unit
RIN,IF2AMP	Input Resistance			2		K $\Omega$
GIF2AMP	Maximum Gain	VIF2AMPIN = 10dBu		51		dB
AGCAMPSCP	Central Point of AGC2 Intervention on IF2 Amp	VIF2AMPIN = 72dBu; Value of VIF2AMPOUT		115		dBu
AGCAMPSP	AGC2 Starting Point on IF2 Amp	Value of VIF2AMPIN for which VIF2AMPOUT is AGCAMPSCP - 3dB		63		dBu
AGCAMPBR	AGC2 Range on IF2 Amp	$f_{IN} = 10.7\text{MHz}$ ; Range of VMIX2AMIN = for which VMIX2OUT is AGCMIXCP $\pm 3\text{dB}$	36			dB
AGCTCR	AGC2 Time Constant Ratio	Ratio of AGC2 "reception" Time Constant and "seek" Time Constant		150/5		s/s
IFAMST	AM IF2 Output Level at pin 28	VIF2AMPIN = 72dBu; AMSTEREO set to 1	104	106	108	dBu
IFAMSTcurr	Current Capability of pin 28	AMSTEREO set to 1		150		$\mu\text{A}$

**AM Field Strength Meter and Field Strength Station Detector**

Ref: AM Test Circuit, measure at VMIX2AMIN, outputs at VAMSMETER and at VAMSD (switches in position 2),  
 -  $f_{IN} = 10.7\text{KHz}$ .  
 - AMSEEK set to 1

Symbol	Parameter	Test Condition	Min.	Typ.	Max	Unit
AMSM1	AM Smeter 1 at VAMSMETER	VMIX2AMIN = 35dBu	2.2	2.89	3.6	V
AMSM2	AM Smeter 2 at VAMSMETER	VMIX2AMIN = 65dBu	2.5	3.26	4.0	V
AMSM3	AM Smeter 3 at VAMSMETER	VMIX2AMIN = 95dBu	3.0	3.73	4.5	V
AMSDMIN	Station Detector Minimum Threshold	VMIX2AMIN at which VAMSD = 2.5V, ASS3-0 set to 0000		44		dBu
AMSDMAX	Station Detector Maximum Threshold	VMIX2AMIN at which VAMSD = 2.5V, ASS3-0 set to 1111		64		dBu

**IF Counter Output**

Ref: AM & FM Test Circuit, measure at pin 28

Symbol	Parameter	Test Condition	Min.	Typ.	Max	Unit
IFCFM	FM IFC Sensitivity	VFMLIMIN at which Vpin 28 = 2.5V, FMRECSEEK set to 1, EW2-0 set to 101, IFS2-0 set to 010		34		dBu
IFCAM	AM IFC Sensitivity	VIF2AMPIN at which Vpin 28 = 2.5V, AMSEEK set to 1, EW2-0 set to 011, IF2-0 set to 100, AMFM STBY1-0 set to 10		29		dBu
IFCcurrent	IFC Current Capability			150		$\mu\text{A}$

**ELECTRICAL CHARACTERISTICS** (continued)  
**Loop Filter Input Output**  
(LP\_IN1, LP\_IN2, LP\_IN3, LP\_OUT)

Symbol	Parameter	Test Condition	Min.	Typ.	Max.	Unit
-I <sub>IN</sub>	Input Leakage Current	V <sub>IN</sub> = GND; PD <sub>out</sub> = Tristate 1)	-2	0	2	μA
I <sub>IN</sub>	Input Leakage Current	V <sub>IN</sub> = V <sub>DD</sub> ; PD <sub>out</sub> = Tristate	-2	0	2	μA
V <sub>OL</sub>	Output Voltage Low	I <sub>IN</sub> = -0.2mA; V <sub>CC</sub> = 8.5V			0.5	V
V <sub>OH</sub>	Output Voltage High	I <sub>OUT</sub> = 0.2mA; V <sub>CC</sub> = 8.5V	8			V
I <sub>OUT</sub>	Output Current Sink	V <sub>PLL</sub> = 8.5V;	10			mA
I <sub>OUT</sub>	Output Current Source	V <sub>out</sub> = 0.5 to 8V	10			mA

### I<sup>2</sup>C Bus Interface

Symbol	Parameter	Test Condition	Min.	Typ.	Max	Unit
f <sub>SCL</sub>	SCL Clock Frequency			100	500	KHz
t <sub>AA</sub>	SCL Low to SDA Data Valid			300		ns
t <sub>buf</sub>	Time the Bus Must Be Free for the New Transmission			4.7		μs
t <sub>HD-STA</sub>	START Condition hold Time			4.0		μs
t <sub>LOW</sub>	Clock Low Period			4.7		μs
t <sub>HIGH</sub>	Clock High Period			4.0		μs
t <sub>SU-SDA</sub>	Start Condition Setup Time			4.7		μs
t <sub>HD-DAT</sub>	Data Input Hold Time			0		μs
t <sub>SU-DAT</sub>	Date Input Setup Time			250		ns
t <sub>R</sub>	SDA & SCL Rise Time					μs
t <sub>F</sub>	SDA & SCL Full Time					μs
t <sub>SU-STO</sub>	Stop Condition Setup Time			4.7		μs
t <sub>DH</sub>	DATA OUT Time			300		ns
V <sub>IL</sub>	Input Low Voltage				1	V
V <sub>IH</sub>	Input High Voltage		3			V

(1) depends upon filter circuitry

(2) depends upon application circuit

(3) depends only upon IF2 ceramic filter



### FM SECTION

Featuring a single conversion configuration, it comprises a multi-stage IF limiter whose gain is I<sup>2</sup>C controlled and a quadrature demodulator with detuning and adjacent channel detectors. Signal meter and stop station functions are also supported

### AM SECTION

AM signal is converted by means of UP-DOWN configuration (IF1 = 10.7MHz, IF2 = 450KHz) and MW/LW bands are covered.

### PLL SECTION

Three operating modes are available:

PM0	PM1	Operating Mode
0	0	Standby
1	0	AM
0	1	not used
1	1	FM

They are user programmable with the mode PM registers.

#### Standby mode

It stops all functions. This allows low current consumption without loss of information in all registers. The pin LP-OUT is forced to 0V in power on. All data registers are set to FE (11111110). The oscillator runs even in stand-by mode.

#### FM and AM Operation

The FM or AM signal applies to a 32/33 prescaler, which is controlled by a 5 bit counter (A). The 5 bit register (PC0 to PC4) controls this divider.

The output of the prescaler connects to a 11 bit divider (B). The 11 bit register (PC5 to PC15) controls the divider 'B'.

#### THREE STATE PHASE COMPARATOR

The phase comparator generates a phase error signal according to phase difference between f<sub>SYN</sub> and f<sub>REF</sub>. This phase error signal drives the charge pump current generator.

#### CHARGE PUMP CURRENT GENERATOR

This stage generates signed pulses of current. The phase error signal decides the duration and polarity of those pulses.

The current absolute values are programmable

by A0, A1, A2 registers for high current and B0, B1 registers for low current.

#### LOW NOISE CMOS OP-AMP

An internal voltage divider at pin V<sub>REF</sub> connects the positive input of the low noise Op-Amp.

The charge pump output connects the negative input. This internal amplifier in cooperation with external components can provide an active filter. The negative input is switchable to three input pins (LPIN 1, LPIN 2 and LPIN 3), to increase the flexibility in application.

This feature allows two separate active filters for different applications.

A logical "1" in the LPIN 1/2 register activates pin LPIN 1, otherwise pin LPIN 2 is active. While the high current mode is activated LPIN 3 is switched on.

#### INLOCK DETECTOR

The charge pump is switched in low current mode as the truth table and the related figure shows.

CURRHIGH	LOCKENA	LOCK (by inlock detector)	Charge Pump Current
0	X	X	low current
1	1	1	low current
1	1	0	High current
1	0	1	High current
1	0	0	High current

The charge pump is forced in low current mode when a phase difference of 10-40 usec is reached.

A phase difference larger than the programmed values will switch the charge pump immediately in the high current mode.

Few programmable delays are available for inlock detection.

#### IF COUNTER SYSTEM FOR AM/FM

The IF counter mode is controlled by IFCM register:

IFCM1	IFCM0	FUNCTION
0	0	NOT USED
0	1	FM MODE
1	0	AM MODE
1	1	NOT USED

A sample timer to generate the gate signal for the main counter is built with a 14 bit programmable counter to have the possibility to use any fre-

**ADDRESS ORGANIZATION** (PLL and IF Counter)

		MSB							LSB
FUNCTION	SUBAD	BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
PLL CHARGE PUMP	00H	LPIN1/2	CURRH	B1	B0	A3	A2	A1	A0
PLL COUNTER	01H	PC7	PC6	PC5	PC4	PC3	PC2	PC1	PC0
PLL COUNTER	02H	PC15	PC14	PC13	PC12	PC11	PC10	PC9	PC8
PLL REF COUNTER	03H	RC7	RC6	RC5	RC4	RC3	RC2	RC1	RC0
PLL REF COUNTER	04H	RC15	RC14	RC13	RC12	RC11	RC10	RC9	RC8
PLL LOCK DETECT	05H	LDENA	-	D3	D2	D1	D0	PM1	PM0
IFC REF COUNTER	06H	IRC7	IRC6	IRC5	IRC4	IRC3	IRC2	IRC1	IRC0
IFC REF COUNTER	07H	IFCM1	IFCM0	IRC13	IRC12	IRC11	IRC10	IRC9	IRC8
IFC CONTROL	08H	IFENA	-	-	-	-	EW2	EW1	EW0
IFC CONTROL	09H	IFS2	IFS1	IFS0	CF4	CF3	CF2	CF1	CF0

quency. In FM mode a 6.25 KHz, in AM mode a 1KHz signal is generated. This counter is followed by an asynchronous divider to generate several sampling times.

**Intermediate Frequency Main Counter (IFMC)**

This counter is a 13-21 bit synchronous autoreload down-counter. Four bits are programmable to have the possibility for an adjust to the frequency of the IF filter.

The counter length is automatically adjusted to the chosen sampling time and the counter mode. At the start the counter will be loaded with a defined value which is an equivalent to the divider value ( $t_{sample} \cdot f_{IF}$ ).

If a correct frequency is applied to the IF counter frequency inputs IF-AM and IF-FM, at the end of the sampling time the main counter is changing its state from 0 to 1FFFFFFH.

This is detected by a control logic. The frequency range inside which a successful count results is detected is adjustable setting bits EW 0, 1, 2.

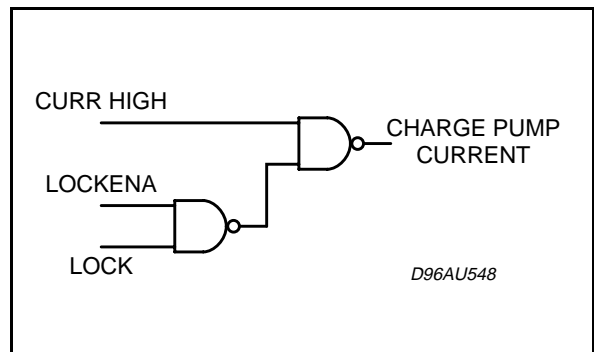
**Up-down counter filter**

The information coming from the IF main counter control logic is shifted into a 5 bit up down counter circuit clocked by the sampling time signal. At the start (rising edge of the IFENA signal) the counter is set to 10H and the SSTOP signal is forced to "1".

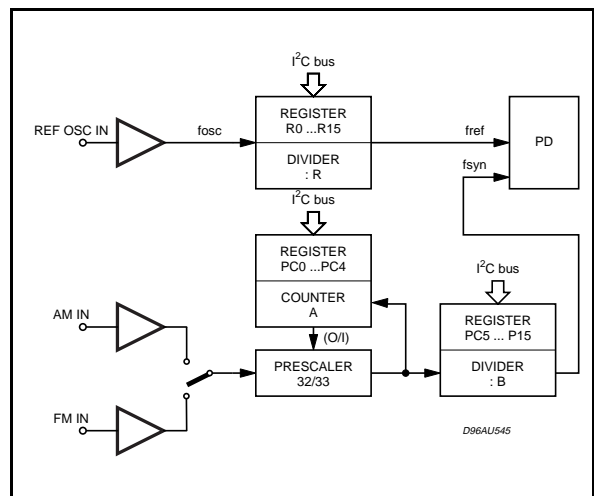
Only when the counter reaches the value 10H - step, SSTOP goes to "0".

SSTOP will be "1" again, if the counter reaches the value 10h + step.

**Charge Pump Logic**



**FM and AM operation (swallow mode)**





$$t_{tim} = (IFRC + 1) / f_{osc}$$

$$t_{cnt} = (CF + 1697) / f_{IF} \quad \text{FM mode}$$

$$t_{cnt} = (CF + 44) / f_{IF} \quad \text{AM mode}$$

Counter result succeeded:

$$t_{tim} > t_{cnt} - t_{err} \text{ and}$$

$$t_{tim} > t_{cnt} + t_{err}$$

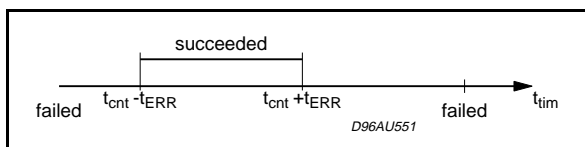
Counter result failed:

$$t_{tim} < t_{cnt} + t_{err} \text{ OR}$$

$$t_{tim} > t_{cnt} - t_{err}$$

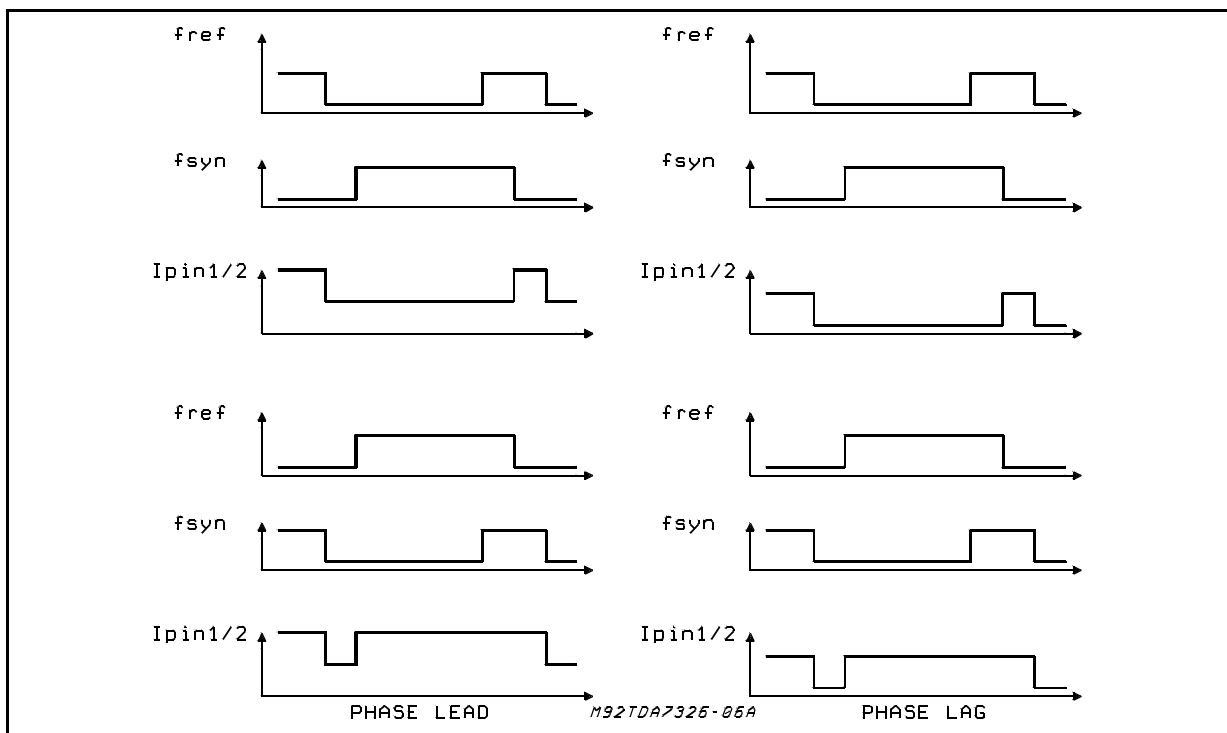
where:

- $t_{tim}$  = IF time cycle time
- $t_{cnt}$  = IF counter cycle time
- $t_{err}$  = discrimination window (controlled by the EW registers)



The precision of the measurements is adjustable

### Phase Comparator



by controlling the discrimination window. This is adjustable by programming the control registers EW0...EW2.

The measurement time per cycle is adjustable by setting the register IFS0 - IFS2.

The center frequency of the discrimination window is adjustable by the control register "CF0" to "CF4". The available values are reported in databyte specification

### I<sup>2</sup>C BUS INTERFACE

#### General Description

The TDA7421 supports the I<sup>2</sup>C bus protocol. This protocol defines the devices sending data into the bus as transmitter and the receiving device as the receiver.

The device that controls the transfer is a master and the device being controlled is the slave. The master will always initiates data transfer and provide the clock to transmit or receive operations.

#### Data Transition

Data transition on the SDA line must only occur when the clock SCL is low. SDA transitions while SCL is high will be interpreted as START or STOP condition.

#### Start Condition

A start condition is defined by a HIGH to LOW transition of the SDA line while SCL is at a stable HIGH level. This START condition must precede any command and initiate a data transfer onto the bus.

The TDA7421 continuously monitors the SDA and SCL lines for a valid START and will not respond to any command if this condition has not been met.

**Stop condition**

A STOP condition is defined by a LOW to HIGH transition of the SDA while the SCL line is at a stable HIGH level. This condition terminates the communication between the devices and forces the bus interface of the TDA7421 into the initial condition.

**Acknowledge**

Indicates a successful data transfer. The transmitter will release the bus after sending 8 bits of data. During the 9th clock cycle the receiver will pull the SDA line to LOW level to indicate it has received the eight bits of data correctly.

**Data transfer**

During data transfer the TDA7421 samples the SDA line on the leading edge of the SCL clock. Therefore, for proper device operation the SDA line must be stable during the SCL LOW to HIGH transition.

**Device Addressing**

To start the communication between two devices,

the bus master must initiate a start instruction sequence, followed by an eight bit word corresponding to the address of the device it is addressing. The most significant 6 bits of the slave address identify the device type.

The TDA7421 device code is fixed as "110001".

The next significant bit is used either to address the tuner section (1) or the PLL section (0) of the chip.

Following a START condition the master sends slave address word; the TDA7421 will "acknowledge" after this first transmission and wait for a second word (the word address field).

This 8 bit address field provides an access to any of the 8 internal addresses. Upon receipt of the word address the TDA7421 slave device will respond with an "acknowledge".

At this time, all the following words transmitted to the TDA7421 will be considered as data.

The internal address will be automatically incremented. After each word receipt the TDA7421 will answer with an "acknowledge".

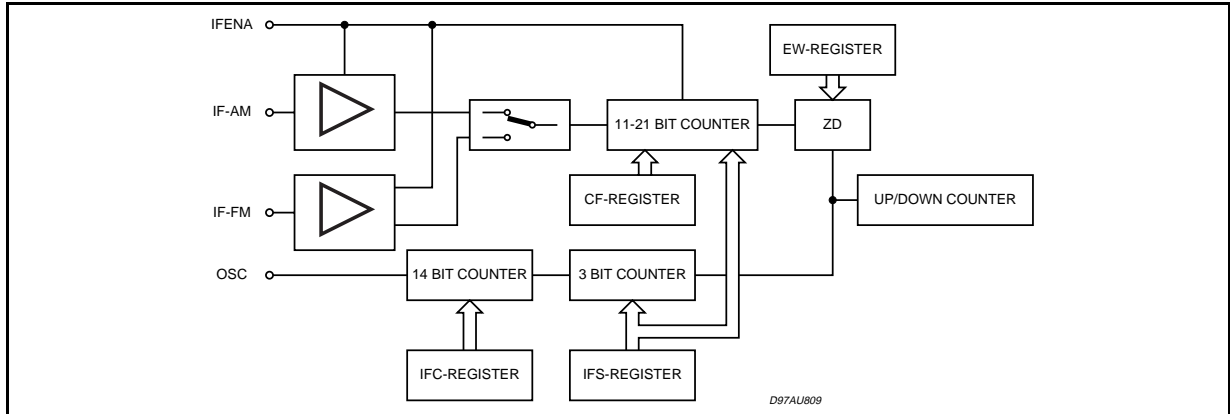
The interface protocol comprises:

- a subaddress byte
- a sequence of data (N-bytes + acknowledge)
- a stop condition (P)
- a start condition (S)
- a chip address byte

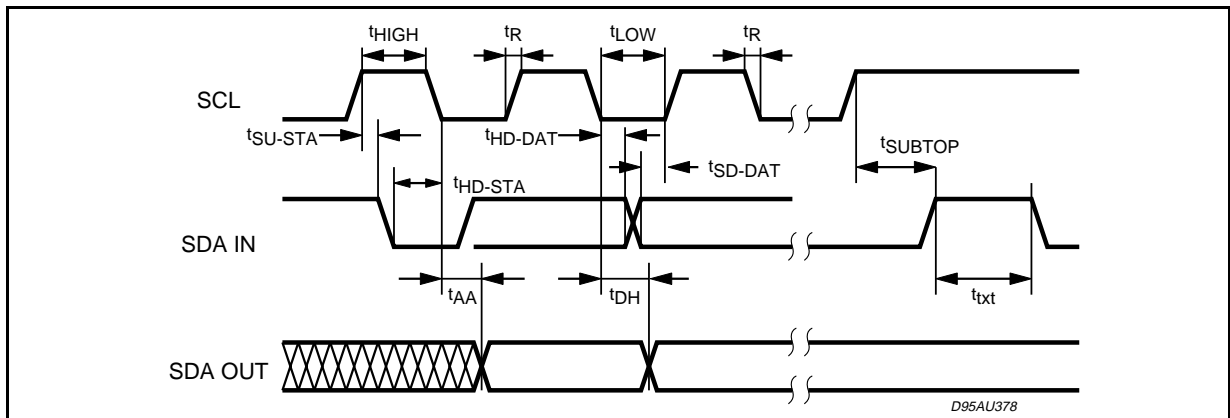
**CONTROL REGISTER FUNCTION**

REGISTER NAME	FUNCTION
PC	Programmable Counter for VCO Frequency
RC	Reference Counter PLL
IRC	Reference Counter IF
IFCM	IF Counter Mode
EW	Frequency Error Window
IFENA	Enable IF Counter
CF	Center Frequency IF Counter
IFS	Sampling Time IF Counter
PM	Stby, FM, AM, AM swallow mode (PLL Mode)
D	Programmable Delay for Lock Detector
LPIN1/2	Loop Filter Input Select
A	Charge Pump High Current
B	Charge Pump Low Current
LDENA	Lock Detector Enable
CURRH	Set Current High

**IF Counter Block Diagram**

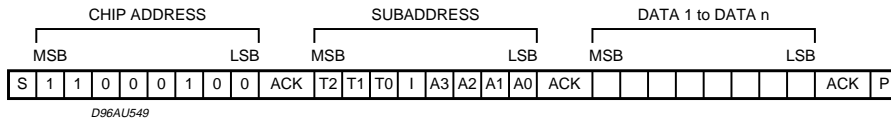


**I<sup>2</sup>C Bus Timing Diagram**

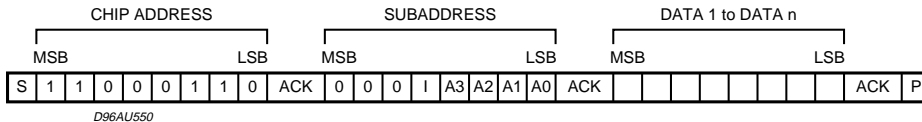


**Frame Example**

For addressing the PLL part:



for the TUNER part:



ACK = Acknowledge  
 S = Start  
 P = Stop

I = Page mode  
 T2, T1, T0 = used in test mode (for PLL only, for TUNER addressing they must be 0)  
 A3, A2, A1, A0 = Mode selection

**TUNER SUBADDRESS**

MSB				LSB				FUNCTION
X	X	X	I	A3	A2	A1	A0	
				0	0	0	0	STATUS
				0	0	0	1	FM STOP STATION / FM IF AGC
				0	0	1	0	FM SMETER SLIDER
				0	0	1	1	AM AGC1 / AM STOP STATION
				0	1	0	0	IFT1 / IFT2
				0	1	0	1	FRONT END ADJUSTMENT
				0	1	1	0	FM DEMODULATOR ADJUSTMENT
				0	1	1	1	FM IF BUFFERS
				1	0	0	0	FM AUDIO MUTE GAIN / FM SOFT MUTE
				1	0	0	1	FM HOLE DETECTOR / FM DETUNING
			0					Page mode disabled
			1					Page mode enabled
0	0	0						must be "0"

**PLL SUBADDRESS**

MSB				LSB				FUNCTION
T3	T2	T1	I	A3	A2	A1	A0	
				0	0	0	0	Charge pump control
				0	0	0	1	PLL counter 1 (LSB)
				0	0	1	0	PLL counter 2 (MSB)
				0	0	1	1	PLL reference counter 1 (LSB)
				0	1	0	0	PLL reference counter 2 (MSB)
				0	1	0	1	PLL lockdetector control and PLL mode select
				0	1	1	0	IFC reference counter 1 (LSB)
				0	1	1	1	IFC reference counter 2 (MSB) and IFC mode select
				1	0	0	0	IF counter control 1
				1	0	0	1	IF counter control 2
			0					page mode DISABLED
			1					page mode enabled

T1, T2, T3 are used for testing the PLL, in application mode they have to be "0".



## PLL DATA BYTE SPECIFICATION

## CHARGE PUMP CONTROL

MSB				LSB				FUNCTION
D7	D6	D5	D4	D3	D2	D1	D0	
				0	0	0	0	High current = 0mA
				0	0	0	1	High current = 0.5mA
				0	0	1	0	High current = 1.0mA
				0	0	1	1	High current = 1.5mA
				0	1	0	0	High current = 2.0mA
				0	1	0	1	High current = 2.5mA
				0	1	1	0	High current = 3.0mA
				0	1	1	1	High current = 3.5mA
				1	0	0	0	High current = 4.0mA
				1	0	0	1	High current = 4.5mA
				1	0	1	0	High current = 5.0mA
				1	0	1	1	High current = 5.5mA
				1	1	0	0	High current = 6.0mA
				1	1	0	1	High current = 6.5mA
				1	1	1	0	High current = 7.0mA
				1	1	1	1	High current = 7.5mA
		0	0					Low current = 0µA
		0	1					Low current = 15µA
		1	0					Low current = 100µA
		1	1					Low current = 115µA
	0							Select low Current
	1							Select high Current
0								Select loop filter 1
1								Select loop filter 2
LPIN1/2	CURRH	B1	B0	A3	A2	A1	A0	Subaddress = 00H

## PLL COUNTER 1 (LSB)

MSB				LSB				FUNCTION
D7	D6	D5	D4	D3	D2	D1	D0	
0	0	0	0	0	0	0	0	LSB = 0
0	0	0	0	0	0	0	1	LSB = 1
0	0	0	0	0	0	1	0	LSB = 2
all combinations allowed								•••
1	1	1	1	1	1	0	0	LSB = 252
1	1	1	1	1	1	0	1	LSB = 253
1	1	1	1	1	1	1	0	LSB = 254
1	1	1	1	1	1	1	1	LSB = 255
PC7	PC6	PC5	PC4	PC3	PC2	PC1	PC0	Bit name Subaddress = 01H

**PLL COUNTER 2 (MSB)**

MSB							LSB		FUNCTION
D7	D6	D5	D4	D3	D2	D1	D0		
0	0	0	0	0	0	0	0	MSB = 0	
0	0	0	0	0	0	0	1	MSB = 256	
0	0	0	0	0	0	1	0	MSB = 512	
all combinations allowed							•••		
1	1	1	1	1	1	0	0	MSB = 64768	
1	1	1	1	1	1	0	1	MSB = 65024	
1	1	1	1	1	1	1	0	MSB = 65280	
1	1	1	1	1	1	1	1	MSB = 65536	
PC15	PC14	PC13	PC12	PC11	PC10	PC9	PC8	Bit name <span style="float:right">Subaddress = 02H</span>	

Swallow mode:  $f_{vco}/f_{syn} = LSB + MSB + 32$

**PLL REFERENCE COUNTER 1 (LSB)**

MSB							LSB		FUNCTION
D7	D6	D5	D4	D3	D2	D1	D0		
0	0	0	0	0	0	0	0	LSB = 0	
0	0	0	0	0	0	0	1	LSB = 1	
0	0	0	0	0	0	1	0	LSB = 2	
all combinations allowed							•••		
1	1	1	1	1	1	0	0	LSB = 252	
1	1	1	1	1	1	0	1	LSB = 253	
1	1	1	1	1	1	1	0	LSB = 254	
1	1	1	1	1	1	1	1	LSB = 255	
RC7	RC6	RC5	RC4	RC3	RC2	RC1	RC0	Bit name <span style="float:right">Subaddress = 03H</span>	

**PLL REFERENCE COUNTER 2 (MSB)**

MSB							LSB		FUNCTION
D7	D6	D5	D4	D3	D2	D1	D0		
0	0	0	0	0	0	0	0	MSB = 0	
0	0	0	0	0	0	0	1	MSB = 256	
0	0	0	0	0	0	1	0	MSB = 512	
all combinations allowed							•••		
1	1	1	1	1	1	0	0	MSB = 64768	
1	1	1	1	1	1	0	1	MSB = 65024	
1	1	1	1	1	1	1	0	MSB = 65280	
1	1	1	1	1	1	1	1	MSB = 65536	
RC15	RC14	RC13	RC12	RC11	RC10	RC9	RC8	Bit name <span style="float:right">Subaddress = 04H</span>	

$f_{osc}/f_{REF} = LSB + MSB + 1$

## LOCK DETECTOR &amp; PLL MODE CONTROL

MSB							LSB		FUNCTION
D7	D6	D5	D4	D3	D2	D1	D0		
						0	0	PLL standby mode	
						0	1	PLL AM	
						1	0	not used	
						1	1	PLL FM mode	
				0	0			PD phase difference threshold 10ns	
				0	1			PD phase difference threshold 20ns	
				1	0			PD phase difference threshold 30ns	
				1	1			PD phase difference threshold 40ns	
		0	0					Not used in application mode	
		0	1					Activation delay = $4 \cdot f_{ref}$	
		1	0					Activation delay = $6 \cdot f_{ref}$	
		1	1					Activation delay = $8 \cdot f_{ref}$	
0								No lock detector controlled chargepump	
1								Lock detector controlled chargepump	
LDENA		D3	D2	D1	D0	PM1	PM0	Bit name                      Subaddress = 05H	

## IF COUNTER REFERENCE CONTROL 1 (LSB)

MSB							LSB		FUNCTION
D7	D6	D5	D4	D3	D2	D1	D0		
0	0	0	0	0	0	0	0	LSB = 0	
0	0	0	0	0	0	0	1	LSB = 1	
0	0	0	0	0	0	1	0	LSB = 2	
all combinations allowed								•••	
1	1	1	1	1	1	0	0	LSB = 252	
1	1	1	1	1	1	0	1	LSB = 253	
1	1	1	1	1	1	1	0	LSB = 254	
1	1	1	1	1	1	1	1	LSB = 255	
IRC7	IRC6	IRC5	IRC4	IRC3	IRC2	IRC1	IRC0	Bit name                      Subaddress = 06H	

## IF COUNTER REFERENCE CONTROL 2 (MSB) AND IF COUNTER MODE SELECT

MSB							LSB		FUNCTION
D7	D6	D5	D4	D3	D2	D1	D0		
0	0	0	0	0	0	0	0	MSB = 0	
0	0	0	0	0	0	0	1	MSB = 256	
0	0	0	0	0	0	1	0	MSB = 512	
all combinations allowed							•••		
		1	1	1	1	0	1	MSB = 15616	
		1	1	1	1	1	0	MSB = 15872	
		1	1	1	1	1	1	MSB = 16128	
0	0							NOT USED IN APPLICATION MODE	
0	1							IF counter FM mode	
1	0							IF counter AM mode	
1	1							not used	
IFCM1	IFCM0	IRC13	IRC12	IRC11	IRC10	IRC9	IRC8	Bit name Subaddress = 07H	

$$f_{osc}/f_{tim} = LSB + MSB + 1$$

## IF COUNTER CONTROL 1

MSB							LSB		FUNCTION
D7	D6	D5	D4	D3	D2	D1	D0		
					0	0	0	don't use	
					0	0	1	don't use	
					0	1	0	don't use	
					0	1	1	EW delta f = ±6.25KHz (FM); ±1KHz (AM)	
					1	0	0	EW delta f = ±12.5KHz (FM); ±2KHz (AM)	
					1	0	1	EW delta f = ±25KHz (FM); ±4KHz (AM)	
					1	1	0	EW delta f = ±50KHz (FM); ±8KHz (AM)	
					1	1	1	EW delta f = ±100KHz (FM); ±16KHz (AM)	
0								IF counter disabled / stand by	
1								IF counter enabled	
IFENA					EW2	EW1	EW0	Bit name Subaddress = 08H	



## IF COUNTER CONTROL 2

MSB			LSB					FUNCTION
D7	D6	D5	D4	D3	D2	D1	D0	
			0	0	0	0	0	fcenter = 10.60000MHz (FM) 448KHz (AM)
			0	0	0	0	1	fcenter = 10.60625MHz (FM) 449KHz (AM)
			0	0	0	1	0	fcenter = 10.61250MHz (FM) 450KHz (AM)
			0	0	0	1	1	fcenter = 10.61875MHz (FM) 451KHz (AM)
			0	0	1	0	0	fcenter = 10.62500MHz (FM) 452KHz (AM)
			0	0	1	0	1	fcenter = 10.63125MHz (FM) 453KHz (AM)
			0	0	1	1	0	fcenter = 10.63750MHz (FM) 454KHz (AM)
			0	0	1	1	1	fcenter = 10.64375MHz (FM) 455KHz (AM)
			0	1	0	0	0	fcenter = 10.65000MHz (FM) 456KHz (AM)
			0	1	0	0	1	fcenter = 10.65625MHz (FM) 457KHz (AM)
			0	1	0	1	0	fcenter = 10.66250MHz (FM) 458KHz (AM)
			0	1	0	1	1	fcenter = 10.66875MHz (FM) 459KHz (AM)
			0	1	1	0	0	fcenter = 10.67500MHz (FM) 460KHz (AM)
			0	1	1	0	1	fcenter = 10.68125MHz (FM) 461KHz (AM)
			0	1	1	1	0	fcenter = 10.68750MHz (FM) 462KHz (AM)
			0	1	1	1	1	fcenter = 10.69375MHz (FM) 463KHz (AM)
			1	0	0	0	0	fcenter = 10.70000MHz (FM) 464KHz (AM)
			1	0	0	0	1	fcenter = 10.70625MHz (FM) 465KHz (AM)
			1	0	0	1	0	fcenter = 10.71250MHz (FM) 466KHz (AM)
			1	0	0	1	1	fcenter = 10.71875MHz (FM) 467KHz (AM)
			1	0	1	0	0	fcenter = 10.72500MHz (FM) 468KHz (AM)
			1	0	1	0	1	fcenter = 10.73125MHz (FM) 469KHz (AM)
			1	0	1	1	0	fcenter = 10.73750MHz (FM) 470KHz (AM)
			1	0	1	1	1	fcenter = 10.74375MHz (FM) 471KHz (AM)
			1	1	0	0	0	fcenter = 10.75000MHz (FM) 472KHz (AM)
			1	1	0	0	1	fcenter = 10.75625MHz (FM) 473KHz (AM)
			1	1	0	1	0	fcenter = 10.76250MHz (FM) 474KHz (AM)
			1	1	0	1	1	fcenter = 10.76875MHz (FM) 475KHz (AM)
			1	1	1	0	0	fcenter = 10.77500MHz (FM) 476KHz (AM)
			1	1	1	0	1	fcenter = 10.78125MHz (FM) 477KHz (AM)
			1	1	1	1	0	fcenter = 10.78750MHz (FM) 478KHz (AM)
			1	1	1	1	1	fcenter = 10.79375MHz (FM) 479KHz (AM)
0	0	0						tsample = 20.48ms (FM mode); 128ms (AM; MODE)
0	0	1						tsample = 10.24ms (FM mode); 64ms (AM; MODE)
0	1	0						tsample = 5.12ms (FM mode); 32ms (AM; MODE)
0	1	1						tsample = 2.56ms (FM mode); 16ms (AM; MODE)
1	0	0						tsample = 1.28ms (FM mode); 8ms (AM;MODE)
1	0	1						tsample = 640μs (FM mode); 4ms (AM;MODE)
1	1	0						tsample = 320μs (FM mode); 2ms (AM; MODE)
1	1	1						tsample = 160μs (FM mode); 1ms (AM; MODE)
IFS2	IFS1	IFS0	CF4	CF3	CF2	CF1	CF0	bit name <span style="float: right;">Subaddress = 09H</span>

## TUNER DATA BYTE SPECIFICATION

## ADDRESS ORGANIZATION (Tuner AM/FM)

FUNCTION	SUBAD	MSB							LSB	
		BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0	
STATUS	00H	TESTON	FMMUTE	FMADJ	FMHIGH	AMSTER EO	AMSEEK / FM RECSEEK	AM/FM/ STBY	AM/FM/ STBY	
FM STOP STATION/ FM IF AGC	01H	FAG2	FAG1	FAG0	FSS4	FSS3	FSS2	FSS1	FSS0	
FM SMETER SLIDER	02H	FSL4	FSL3	FSL2	FSL1	FSL0	-	-	-	
AM AGC1/AM STOP STATION	03H	ASS3	ASS2	ASS1	ASS0	AAG3	AAG2	AAG1	AAG0	
IFT1/IFT2	04H	T2A3	T2A2	T2A1	T2A0	T1A3	T1A2	T1A1	T1A0	
FRONT END ADJUSTMENT	05H	ANA3	ANA2	ANA1	ANA0	RFA3	RFA2	RFA1	RFA0	
FM DEMODULATOR ADJUSTMENT	06H	SDD	DEM6	DEM5	DEM4	DEM3	DEM2	DEM1	DEM0	
FM IF BUFFERS	07H	FBL3	FBL2	FBL1	FBL0	FBH3	FBH2	FBH1	FBH0	
FM SOFT MUTE/ FM AUDIO MUTE GAIN	08H	FSM3	FSM2	FSM2	FSM0	-	AUM2	AUM1	AUM0	
FM HOLE DETECTOR /FM DETUNING DETECTOR	09H	BWM2	BWM1	BWM0	HDM4	HDM3	HDM2	HDM1	HDM0	

**STATUS** (subaddress 00H)

MSB				LSB				FUNCTION
S7	S6	S5	S4	S3	S2	S1	S0	
TESTON	FMMUTE	FMADJ	FMHIGH	AM STEREO	AM SEEK/FM RECSEEK	AM/FM/STBY	AM/FM/STBY	
X	X	X	X	X	X	0	0	STAND-BY
0	0	0	0	X	0	0	1	FM ON, RECEPTION, DEEP MUTE
0	0	0	0	X	1	0	1	FM ON, SEEK, DEEP MUTE
0	0	0	1	X	0	0	1	FM ON, RECEPTION, SHALLOW MUTE
0	0	0	1	X	1	0	1	FM ON, SEEK SHALLOW MUTE
0	0	1	X	X	X	0	1	FM ON FOR DEMOD ADJUSTM, DEMOD ON
0	1	1	X	X	X	0	1	FM ON FOR DEMOD ADJUSTMENT DEMOD MUTED
0	X	X	X	0	0	1	0	AM ON (Japan), RECEPTION, IFC OUT SELECTED
0	X	X	X	0	1	1	0	AM ON (Japan), SEEK, IFC OUT SELECTED
0	X	X	X	1	0	1	0	AM ON (Japan), RECEPTION AM STEREO OUT SELECTED
0	X	X	X	1	1	1	0	AM ON (Japan), SEEK, AM STEREO OUT SELECTED
0	X	X	X	0	0	1	1	AM ON (EU, US), RECEPTION, IFC OUT SELECTED
0	X	X	X	0	1	1	1	AM ON (EU, US), SEEK, IFC OUT SELECTED
0	X	X	X	1	0	1	1	AM ON (EU, US), RECEPTION AM STEREO OUT SELECTED
0	X	X	X	1	1	1	1	AM ON (EU, US), SEEK, AM STEREO OUT SELECTED
1						X	X	PLL TEST OUTPUT ENABLED

AM TURN ON SEQUENCE AT POWER ON: it is necessary to cycle through ST-BY for a correct operation.

**FM STOP STATION / FM IF AGC (subaddress 01H)**

MSB							LSB	FUNCTION
FAG2	FAG1	FAG0	FAG4	FSS3	FSS2	FSS1	FSS0	
fmifagc MSB	fmifagc	fmifagc LSB	fmstop station MSB	fmstop station	fmstop station	fmstop station	fmstop station LSB	<b>FM STOP STATION THRESHOLD</b>
			0	0	0	0	0	Maximum sensitivity
			X	X	X	X	X	•••
			1	1	1	1	1	Minimum sensitivity
all combinations allowed								
								<b>FM IF AGC THRESHOLD</b>
0	0	0						Maximum sensitivity
X	X	X						•••
1	1	0						Minimum sensitivity
1	1	1						Keying AGC disabled
all combinations allowed								

**FM SMETER SLIDER (subaddress 02H)**

MSB					LSB			FUNCTION
FSL4	FSL3	FSL2	FSL1	FSL0				
fmsmeter slider MSB	fmsmeter slider			fmsmeter slider LSB				
								<b>FM SMETER SLIDER THRESHOLD (mV)</b>
0	0	0	0	0				300 (baseline)
0	0	0	0	1				348.4 (+48.4)
0	0	0	1	0				396.8 (+96.8)
0	0	1	0	1				493.6 (+193.6)
0	1	0	0	0				687.2 (+387.2)
1	0	0	0	0				1074.4 (+774.4)
1	1	1	1	1				1800 (top)
all combinations allowed								

**AM STOP STATION / AM AGC1** (subaddress 03H)

MSB				LSB				FUNCTION
ASS3	ASS2	ASS1	ASS0	AAG3	AAG2	AAG1	AAG0	
amstopstation MSB	amstopstation		amstopstation LSB	amagc1 MSB	amagc1	amagc1	amagc1 LSB	<b>AM AGC1 THRESHOLD</b>
				0	0	0	0	Maximum sensitivity
				X	X	X	X	•••
				1	1	1	1	Minimum sensitivity
				all combinations allowed				<b>AM STOP STATION THRESHOLD</b>
0	0	0	0					Maximum sensitivity
X	X	X	X					•••
1	1	1	1					Minimum sensitivity
all combinations allowed								

**IFT1/ IFT2** (subaddress 04H)

MSB				LSB				FUNCTION
T2A3	T2A2	T2A1	T2A0	T1A3	T1A2	T1A1	T1A0	
IFT2 adjust MSB	IFT2 adjust	IFT2 adjust	IFT2 adjust LSB	IFT1 adjust MSB	IFT1 adjust	IFT1 adjust	IFT1 adjust LSB	<b>ADJUSTMENT CAPACITOR</b>
				0	0	0	0	0
				0	0	0	1	$C_{ift1}$
				0	0	1	0	$2C_{ift1}$
				0	1	0	0	$4C_{ift1}$
				1	0	0	0	$8C_{ift1}$
				1	1	1	1	$15C_{ift1}$
				all combinations allowed				
0	0	0	0					0
0	0	0	1					$C_{ift2}$
0	0	1	0					$2C_{ift2}$
0	1	0	0					$4C_{ift2}$
1	0	0	0					$8C_{ift2}$
1	1	1	1					$15C_{ift2}$
all combinations allowed								

## FRONT END ADJUSTMENT (subaddress 05H)

MSB				LSB				FUNCTION
ANA3	ANA2	ANA1	ANA0	RFA3	RFA2	RFA1	RFA0	
ant adjustm MSB	ant adjustm	ant adjustm	ant adjustm LSB	RF adjustm MSB	RF adjustm	RF adjustm	RF adjustm LSB	Voffset RF varicap / VPLL
				X	0	0	0	0
				0	0	0	1	-3.6%
				0	0	1	0	-7.2%
				0	1	0	0	-14.3%
				0	1	1	1	-25%
				1	0	0	1	3.6%
				1	0	1	0	7.2%
				1	1	0	0	14.3%
				1	1	1	1	25%
all combinations allowed								
								V offset antenna varicap / VPLL
X	0	0	0					0
0	0	0	1					-3.6%
0	0	1	0					-7.2%
0	1	0	0					-14.3%
0	1	1	1					-25%
1	0	0	1					3.6%
1	0	1	0					7.2%
1	1	0	0					14.3%
1	1	1	1					25%
all combinations allowed								

## FM DEMODULATOR ADJUSTMENT (subaddress 06H)

MSB							LSB		FUNCTION
SDD	DEM6	DEM5	DEM4	DEM3	DEM2	DEM1	DEM0		
SD disable	demadj MSB	demadj	demadj	demadj	demadj	demadj	demadj LSB	<b>ADJUSTMENT CAPACITOR</b>	
	0	0	0	0	0	0	0	0	
	0	0	0	0	0	0	1	$C_{demod}$	
	0	0	0	0	0	1	0	$2C_{demod}$	
	0	0	0	0	1	0	0	$4C_{demod}$	
	0	0	0	1	0	0	0	$8C_{demod}$	
	0	0	1	0	0	0	0	$16C_{demod}$	
	0	1	0	0	0	0	0	$32C_{demod}$	
	1	0	0	0	0	0	0	$64C_{demod}$	
	1	1	1	1	1	1	1	$127C_{demod}$	
all combinations allowed									
<b>SD DISABLE</b>									
0								SD ENABLED	
1								SD DISABLED (High impedance output)	

## FM IF BUFFERS (subaddress 07H)

MSB							LSB		FUNCTION
FBL3	FBL2	FBL1	FBL0	FBH3	FBH2	FBH1	FBH0		
buff2 gain MSB	buff2 gain	buff2 gain	buff2 gain LSB	buff1 gain MSB	buff1 gain MSB	buff1 gain	buff1 gain LSB	<b>BUFFER 1 GAIN (dB)</b>	
				0	0	0	0	19.5	
				0	0	0	1	15.5	
				0	0	1	0	16.5	
				0	1	0	0	17.5	
				1	0	0	0	18.5	
all else not allowed									
<b>BUFFER 2 GAIN (dB)</b>									
0	0	0	0					8	
0	0	0	1					4	
0	0	1	0					5	
0	1	0	0					6	
1	0	0	0					7	
all else not allowed									

## FM SOFT MUTE / FM AUDIO MUTE GAIN (subaddress 08H)

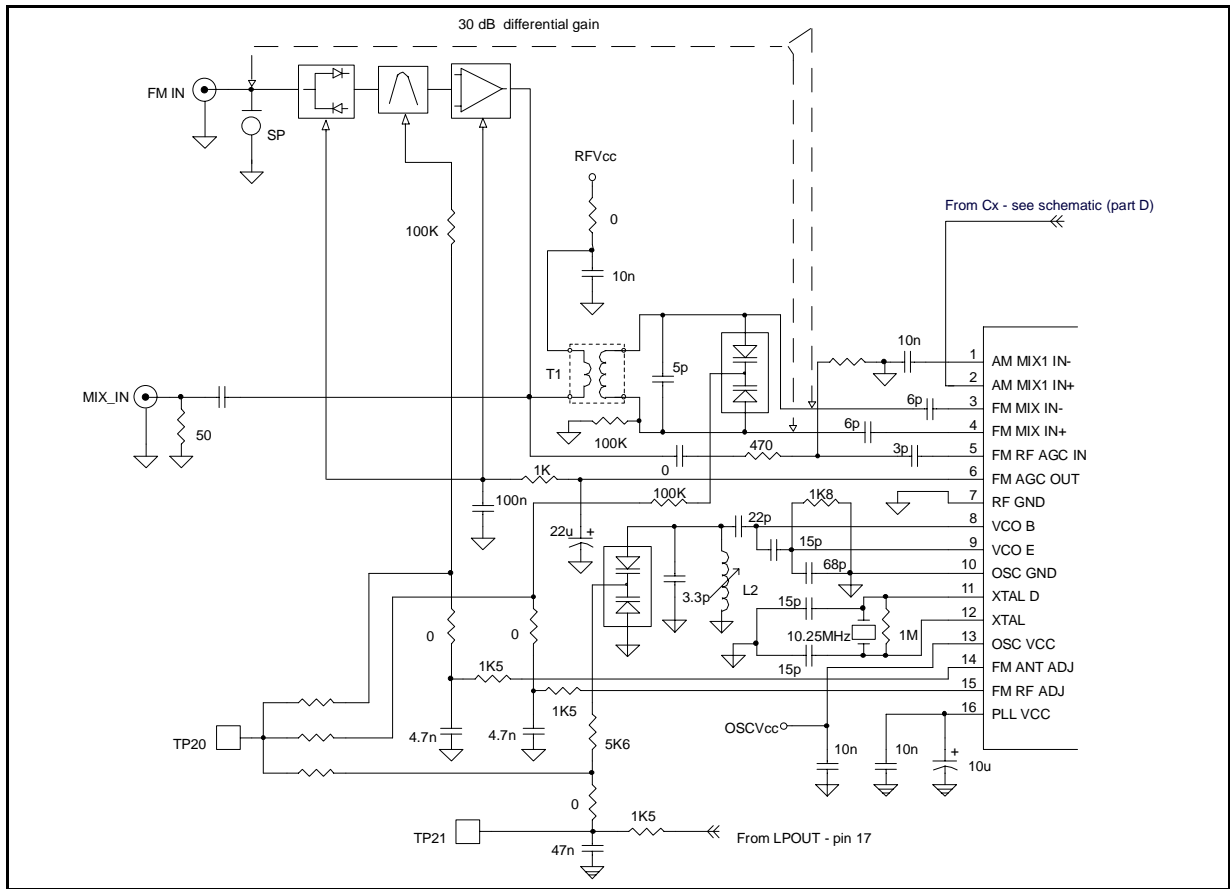
MSB				LSB			FUNCTION	
FSM3	FSM2	FSM1	FSM0		AUM2	AUM1	AUM0	
fmsftmute MSB	fmsftmute	fmsftmute	fmsftmute LSB		buff1 gain MSB	buff1 gain	buff1 gain LSB	<b>FM SOFT MUTE THRESHOLD</b>
0	0	0	0					Maximum sensitivity
X	X	X	X					•••
1	1	1	1					Minimum sensitivity
all combinations allowed								<b>Audio max mute atten. (dB) with bit FMHIGH byte 0 = 1</b>
					0	0	1	-2.5
					0	1	0	-5
					1	0	0	-7.5
					0	1	1	-10
					1	1	0	-12.5
					1	1	1	-15
								<b>Audio max mute atten. (dB) with bit FMHIGH byte 0 = 0</b>
					0	0	1	-17.5
					0	1	0	-20
					1	0	0	-22.5
					0	1	1	-25
					1	1	0	-27.5
					1	1	1	-30
					all else not allowed			

## FM HOLE DETECTOR / FM DETUNING DETECTOR (subaddress 09H)

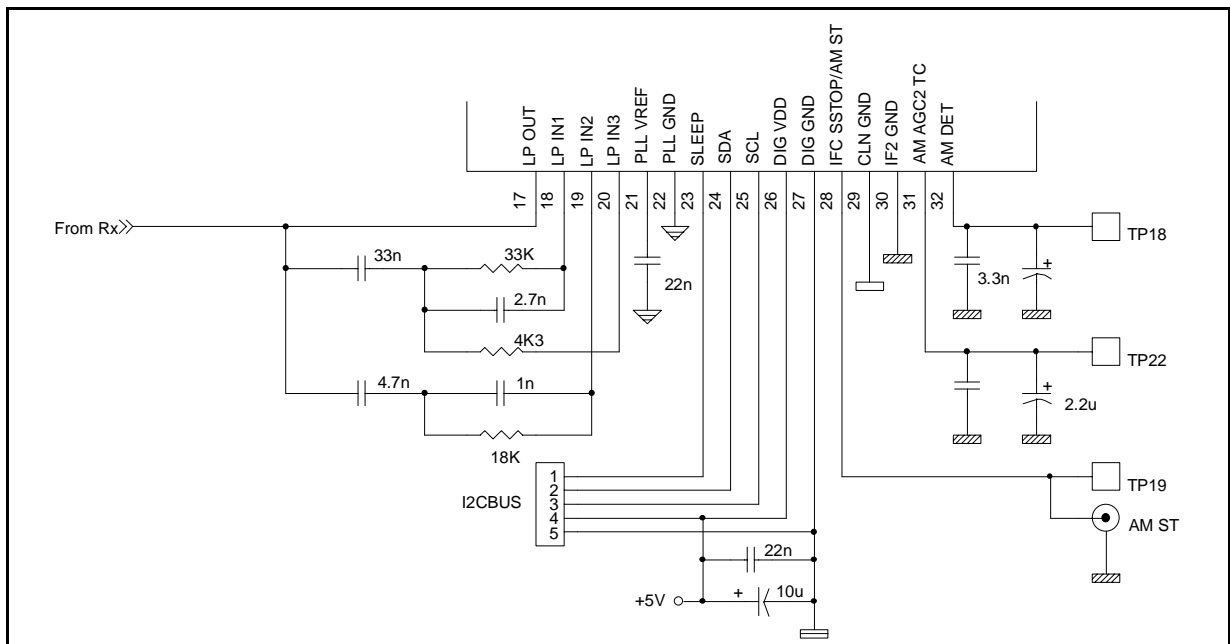
MSB				LSB				FUNCTION
BWM2	BWM1	BWM0	HDM4	HDM3	HDM2	HDM1	HDM0	
BW MSB	BW	BW LSB	Hole det MSB	Hole det	Hole det	Hole det	Hole det LSB	<b>MUTING SENSITIVITY</b>
			0	0	0	0	0	Minimum (deep hole)
			X	X	X	X	X	•••
			1	1	1	1	1	Maximum (shallow hole)
all combinations allowed								
RECEPTION								<b>DETUNING MUTE RANGE</b>
0	0	1						10 (KHz)
0	1	0						15 (KHz)
1	0	0						30 (KHz)
all else not allowed								
SEEK								<b>CLAMPING WINDOW</b>
0	0	0						Minimal Window
X	X	X						Intermediate values
1	1	1						Maximal Window
all combinations allowed								



Evaluation Board Schematic Circuit (part A)

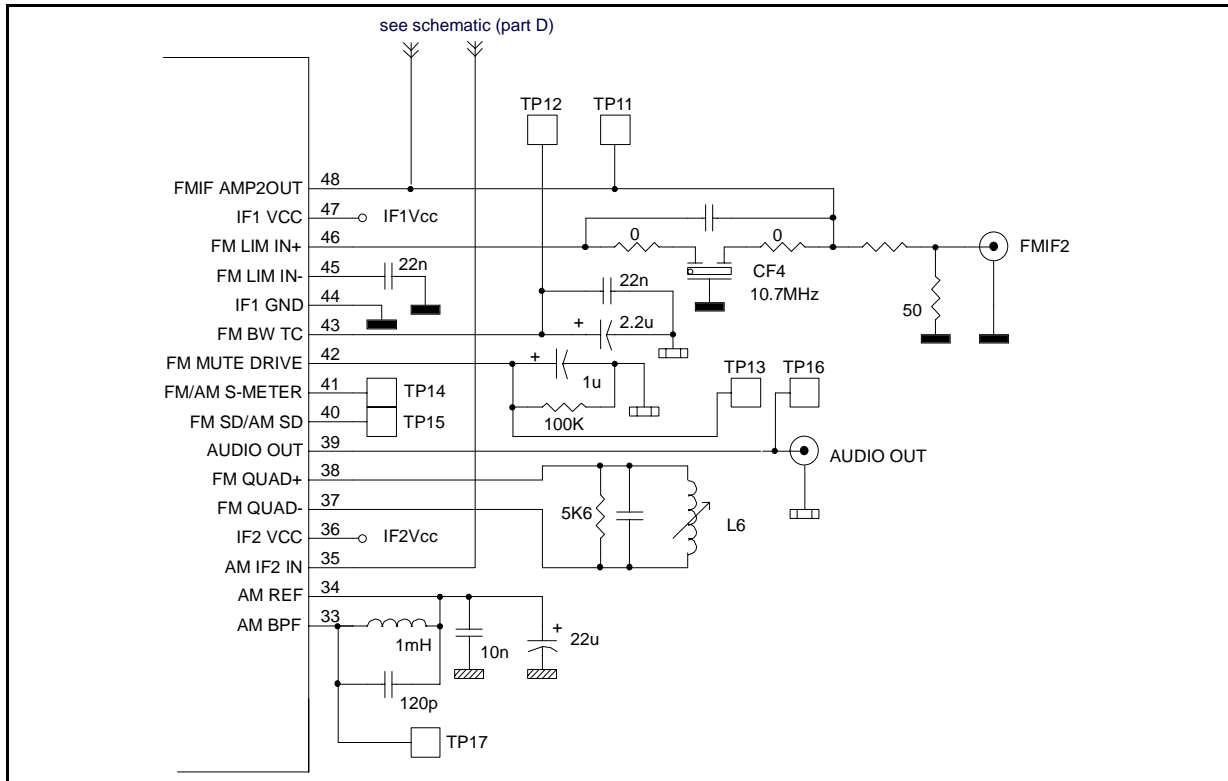


Evaluation Board Schematic Circuit (part B)

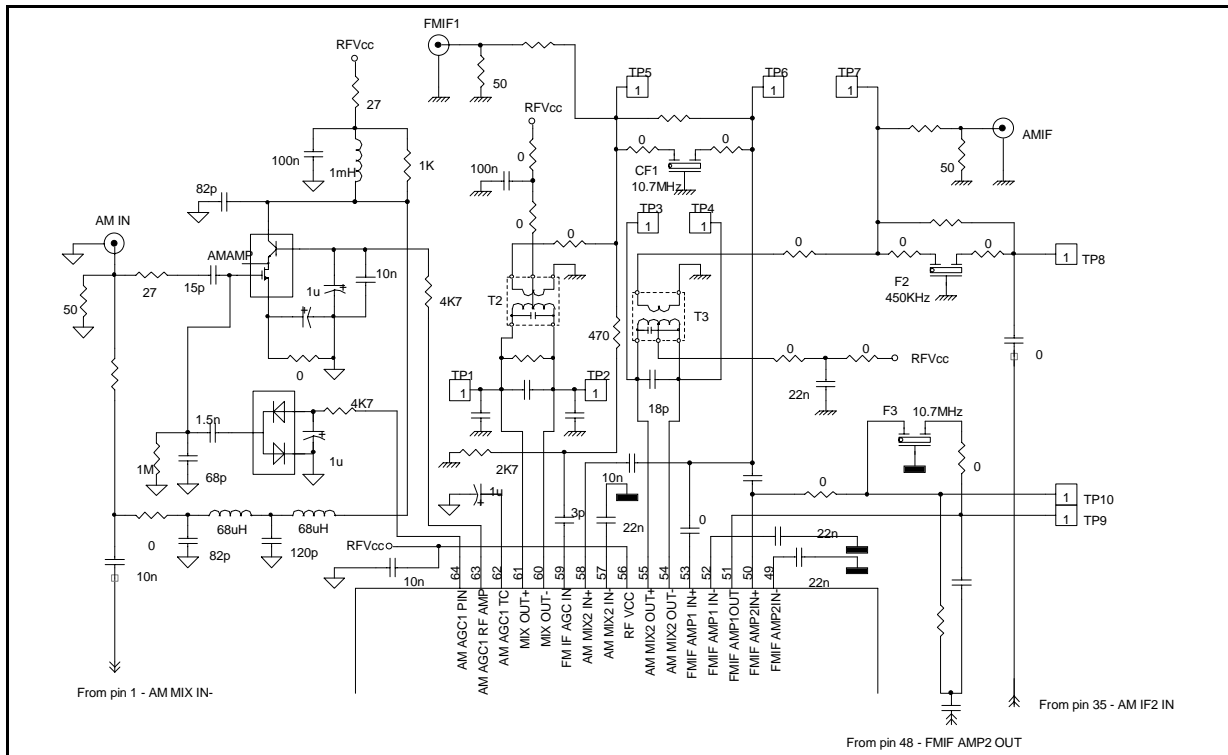


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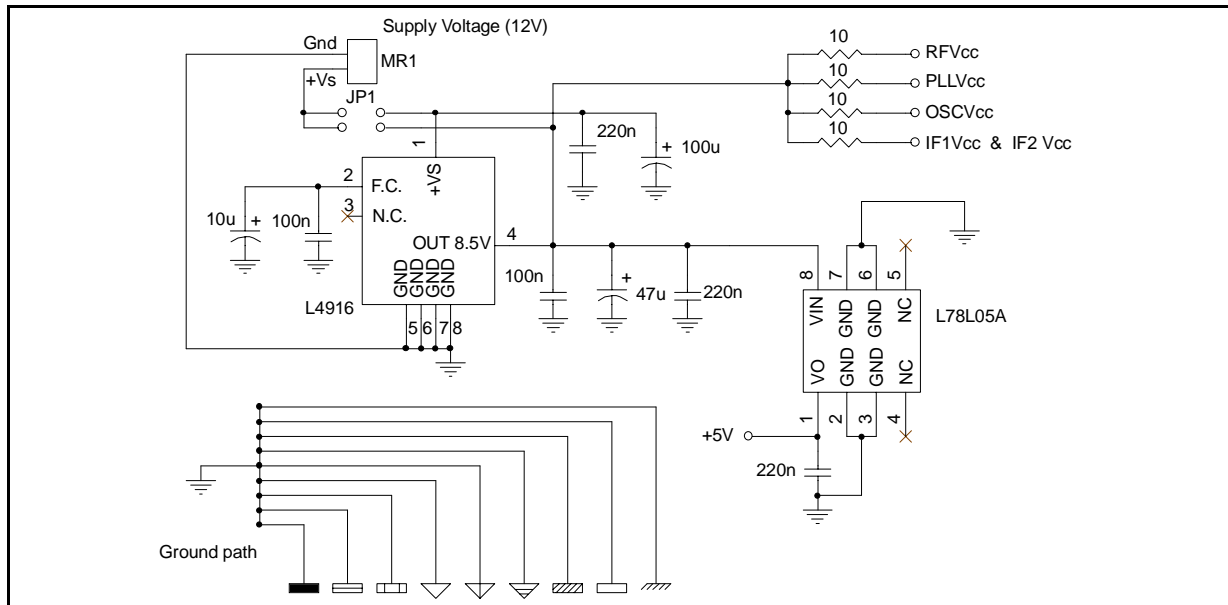
## Evaluation Board Schematic Circuit (part C)



## Evaluation Board Schematic Circuit (part D)



## Evaluation Board Schematic Circuit (part E)



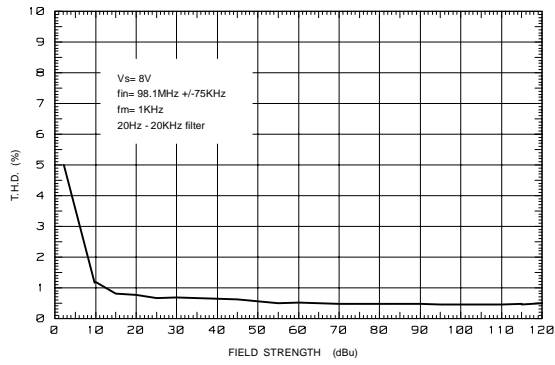
## Notes:

- The components shown on the evaluation board schematic without the part value, are required only for measurements between intermediate input/outputs:
- Parts description:

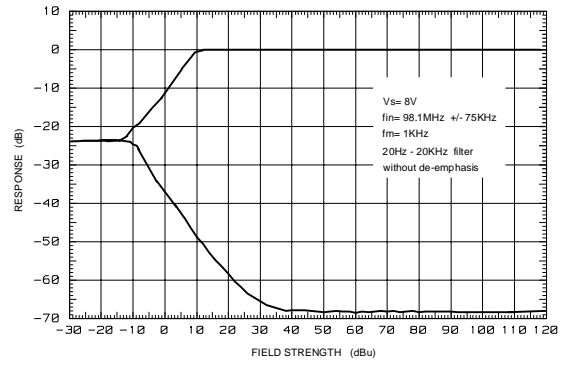
CF1	Ceramic filter 10.7MHz, 180KHz BW
CF3-CF4	Ceramic filter 10.7MHz, 150KHz BW
CF2	Ceramic filter 450KHz, 6KHz BW
T1	FM RF transformer Unloaded Q= 103 3-1= 3 1/2T - 6-4= 1T 0.12φ2UEW CTUNING(3-1)= 24pF @ 100MHz
T2	AM/FM IF1 transformer Unloaded Q= 70 1-3= 13T - 1-5= 6 1/2T - 5-3= 6 1/2T - 4-6= 2T 0.08φ2UEW CINT(1-2) = CINT(2-3) = 82pF; CEXT(1-3) = 10pF
T3	AM IF2 transformer Unloaded Q= 40 1-3= 178T - 1-2= 89T - 2-3= 89T - 4-6= 33T 0.05φ2UEW CINT(1-3) = 180pF; CEXT(1-3) = 20pF
L2	Oscillator coil Unloaded Q= 80 6-4= 2 1/2T 0.12φ2UEW CTUNING(6-4)= 36.8pF @ 100MHz
L6	Demodulator Coil Unloaded Q= 35 6-4= 27T 0.1φ2UEW CINT(4-6)= 47pF; CEXT(4-6) = 13.5pF

# TDA7421

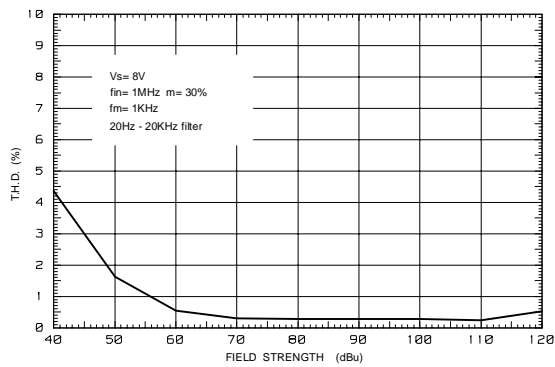
## FM THD



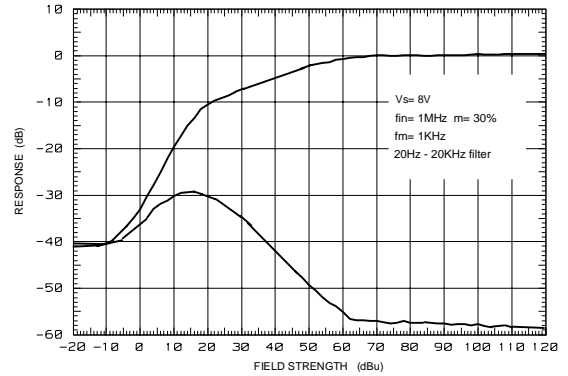
## FM S+N/N



## AM THD

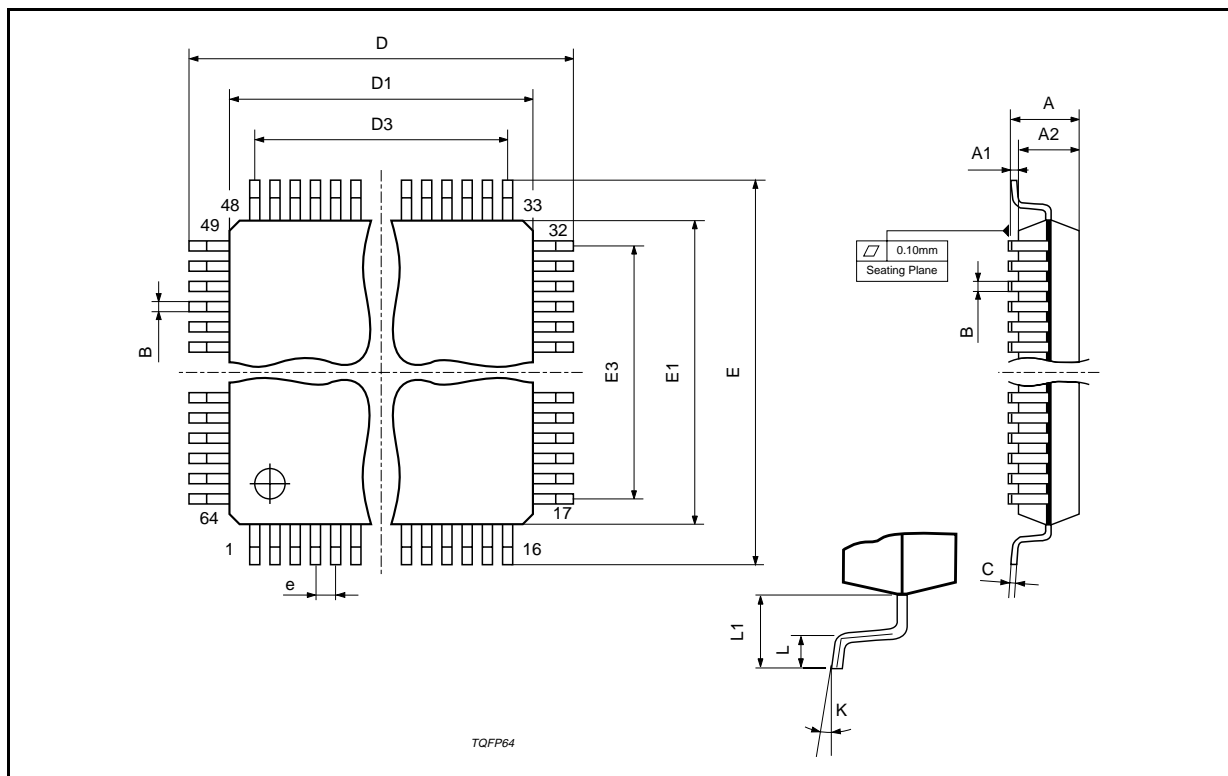


## AM S+N/N



## TQFP64 PACKAGE MECHANICAL DATA

DIM.	mm			inch		
	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.
A			1.60			0.063
A1	0.05		0.15	0.002		0.006
A2	1.35	1.40	1.45	0.053	0.055	0.057
B	0.18	0.23	0.28	0.007	0.009	0.011
C	0.12	0.16	0.20	0.0047	0.0063	0.0079
D		12.00			0.472	
D1		10.00			0.394	
D3		7.50			0.295	
e		0.50			0.0197	
E		12.00			0.472	
E1		10.00			0.394	
E3		7.50			0.295	
L	0.40	0.60	0.75	0.0157	0.0236	0.0295
L1		1.00			0.0393	
K	0°(min.), 7°(max.)					



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