622 Mbit/s MUX/DeMUX Chip Set GD16131/GD16132

General Description

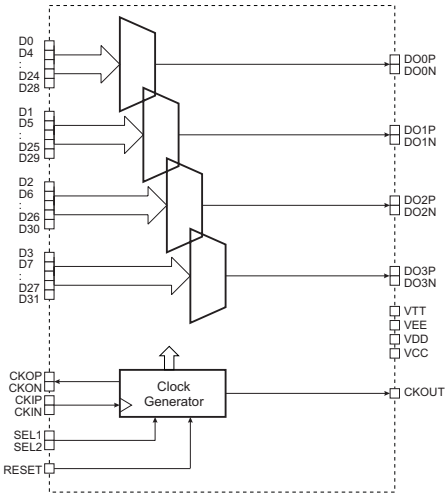
The GD16131, 32:4 / Quad 8:1 MUX and the GD16132, 4:32 / Quad 1:8 DeMUX are intended for use in 2.5 Gbit/s transmission systems. The high-speed interface is designed to accommodate the requirements of the GD16554 (4:1 MUX) and the GD16543 (1:4 DeMUX) both meeting CCITT specifications at 2.5 Gbit/s SDH STM-16. The GD16131 and GD16162 take care of the interface between the high-speed devices differential ECL level I/O's at 622 Mbit/s and lower speed CMOS gate arrays at 78 Mbit/s. Hence they are dual supply devices shifting levels between true ECL and TTL.

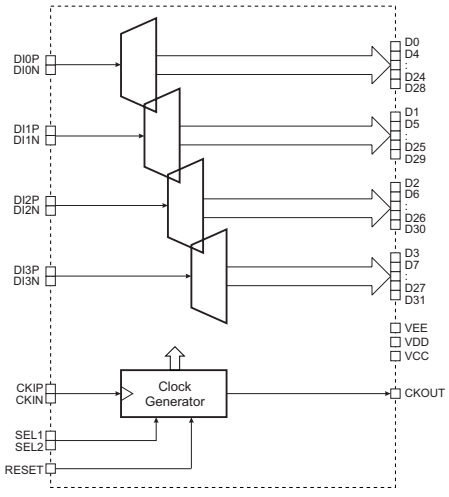
The GD16131 and GD16132 are made as four identical blocks of 8 bit and a clock driver circuit. The 8 bit blocks are implemented as shift registers to obtain the best speed/power ratio of the process technology used. Also this means easy clock distribution with small delay between incoming and outgoing signals. For the GD16131 the 622 Mbit/s data outputs are re-timed at the chip edge to cut down delay from clock-in to data-out, allowing counter directional clocking.

Thus the on-chip delay, except output buffer load dependant delay, is kept below 1 ns. A 622 MHz output clock with close timing relation to the data outputs also allows co-directional clocking. On both MUX and DeMUX, the subdivided 78 MHz clock are also re-timed at the chip edge to cut down delay from the 622 MHz input clock. The phase relation between low-speed data and the subdivided output clock are selectable in four phases.

The GD16131 and GD16132 are packaged in 68 pin Multi Layer Ceramic (MLC) packages, yielding excellent high-speed signal accommodation and thermal conditions. The chip set is designed for an operating temperature between –5 °C and +85 °C, case temperature. With power consumption of 1.3 W typical for both GD16131 and GD16132, only little or no heat sink is required.

Bit naming convention
Naming of pins on parallel ports is made assuming the transfer bit order to be increasing starting with position D0, D1, ..., D31.





Features

GD16131

- Quad 8:1 MUX
- All high-speed I/O's are differential, ECL level.
- All low-speed I/O's are TTL level, outputs drive 10 pF at 78 MHz.
- Subdivided output clock to data relation selectable in four phases.
- Dual supply: +5 V, -5.2 V.
- 68 pin MLC flat package.
- High-speed pins on single side of package for easy PCB routing.
- Power consumption: 1.3 W typical.

GD16132

- Quad 1:8 DeMUX
- All high-speed I/O's are differential, ECL level.
- All low-speed I/O's are TTL level, outputs drive 10 pF at 78 MHz.
- Subdivided output clock to data relation selectable in four phases.
- Dual supply: +5 V, -5.2 V.
- 68 pin MLC flat package.
- High-speed pins on single side of package for easy PCB routing.
- Power consumption: 1.3 W typical.

Function Description

GD16131 - MUX

The first bit shifted out is the one with the lowest number. The first internal 8:1 MUX of the GD16131 services bits 0-4-8-12-16-20-24-28. Neighboring input pins in the pin-out go to the same MUX.

GD16132 - DeMUX

The first bit received is shifted out on the lowest pin number. The first of the 4 internal 1:8 DeMUX of the GD16132 drives outputs 0-4-8-12-16-20- 24-28. Neighboring output pins go to the same DeMUX.

Pin List – GD16131

Mnemonic:	Pin No.:	Pin Type:	Description:
D0 .. D31	22, 32, 56, 66, 23, 33, 54, 64, 24, 36, 53, 63, 25, 37, 50, 62, 27, 39, 49, 61, 28, 40, 47, 59, 29, 41, 46, 58, 30, 42, 45, 57	TTL IN	Parallel data input port to MUX.
DO0P, DO0N DO1P, DO1N DO2P, DO2N DO3P, DO3N	10, 11 7, 8 5, 6 2, 3	ECL OUT	Differential serial data outputs from MUX.
CKIP, CKIN	12, 13	ECL IN	Differential clock input, 622 MHz.
CKOP, CKON	15, 16	ECL OUT	Differential clock output with timing related to data outputs, 622 MHz.
CKOUT	44	TTL OUT	Subdivided output clock, 78 MHz. Maximum load 10 pF.
SEL1, SEL2	19, 20	TTL IN	CKOUT clock phase select: SEL2 SEL1 0 0 T_{DEL} = 0° 0 1 T_{DEL} = 270° (-90)° 1 0 T_{DEL} = 180° 1 1 T_{DEL} = 90°
RESET	67	TTL IN	Test reset. Not needed on power up, the device is self synchronising. Reset is used for test only.
VDD	4, 9, 14, 21, 26, 31, 38, 43, 48, 55, 60, 65	PWR	0 V power for core and ECL I/O.
VCC	18, 52	PWR	+5 V power for core and TTL I/O. All power pins must be connected. Decoupling should be made close to package body.
VEE	1, 34, 51	PWR	-5.2 V power for core and ECL I/O. All power pins must be connected. Decoupling should be made close to package body .
NC	17, 35, 68		Not Connected

Pin List – GD16132

Mnemonic:	Pin No.:	Pin Type:	Description:
D0 .. D31	29, 41, 45, 57, 28, 40, 46, 58, 27, 39, 47, 59, 25, 37, 49, 61, 24, 36, 50, 62, 23, 33, 53, 63, 22, 32, 54, 64, 20, 30, 56, 66	TTL OUT	Parallel data output from DeMUX. Maximum load 10 pF.
DI0P, DI0N DI1P, DI1N DI2P, DI2N DI3P, DI3N	10, 11 12, 13 2, 3 5, 6	ECL IN	Differential serial data inputs.
CKIP, CKIN	7, 8	ECL IN	Differential clock input, 622 MHz.
CKOUT	42	TTL OUT	Subdivided output clock, 78 MHz. Maximum load 10 pF.
SEL1, SEL2	16, 15	TTL IN	CKOUT clock phase select: SEL2 SEL1 0 0 T_{DEL} = 0° 0 1 T_{DEL} = 270° (-90)° 1 0 T_{DEL} = 180° 1 1 T_{DEL} = 90°
RESET	67	TTL IN	Test reset. Not needed on power up, the device is self synchronising. Reset is used for test only.
VDD	4, 9, 14, 21, 26, 31, 38, 43, 48, 55, 60, 65	PWR	0 V power for core and ECL I/O.
VCC	1, 34, 35, 52, 68	PWR	+5 V power for core and TTL I/O. All power pins must be connected. Decoupling should be made close to package body.
VEE	17, 51	PWR	-5.2 V power for core and ECL I/O. All power pins must be connected. Decoupling should be made close to package body.
NC	18, 19, 44		Not Connected.

Package Pinout

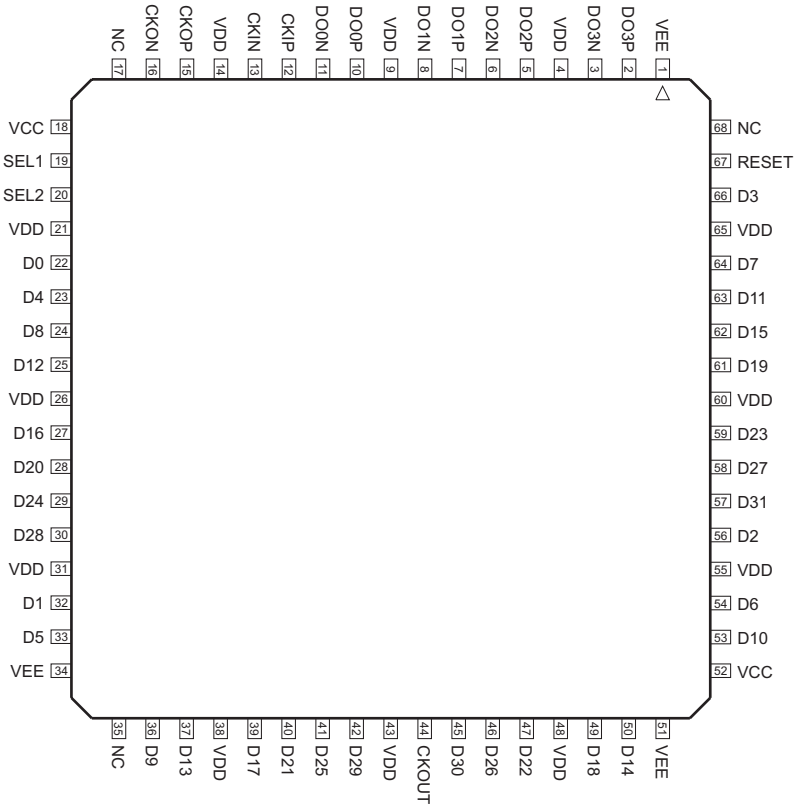


Figure 1. *Package Pinout, GD16131 – Top View*

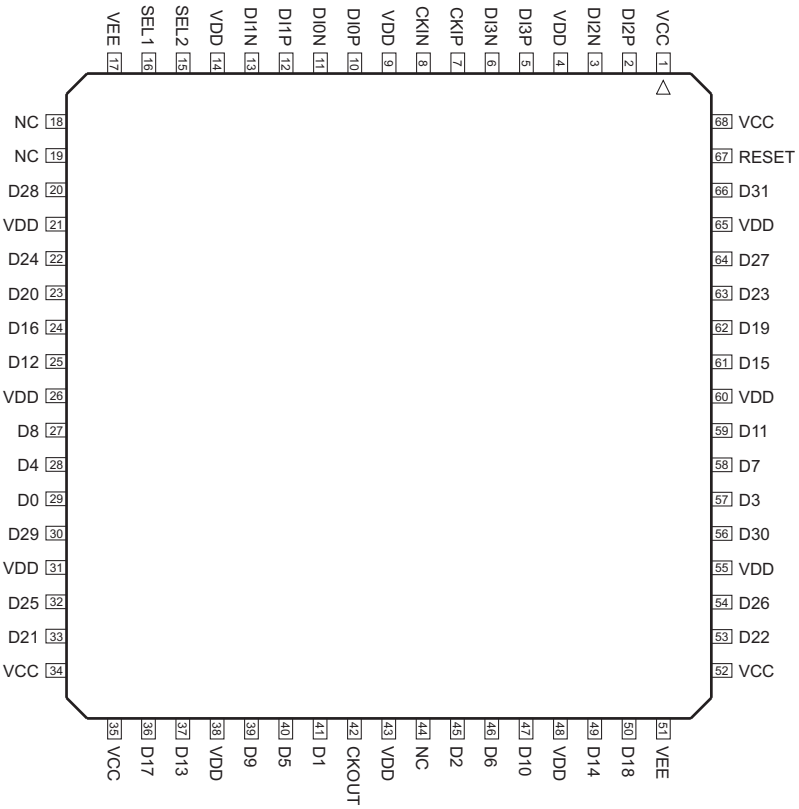


Figure 2. *Package Pinout, GD16132 – Top View*

Maximum Ratings

These are the limits beyond which the component may be damaged.
All voltages in table are referred to VDD.
All currents in table are defined positive out of the pin.

Symbol:	Characteristic:	Conditions:	MIN.:	TYP.:	MAX.:	UNIT:
V_{EE}	Negative Supply		-7		0	V
V_{CC}	Positive Supply		0		+7	V
$V_{O\ max\ ECL}$	Output Voltage	ECL	V_{EE} -0.5		0.5	V
$V_{O\ max\ TTL}$	Output Voltage	TTL	-0.5		V_{CC} +0.5	V
$I_{O\ max\ ECL}$	Output Current	ECL			40	mA
$I_{O\ max\ TTL}$	Output Current	TTL			20	mA
$V_{I\ max\ ECL}$	Input Voltage	ECL	V_{EE} -0.5		0.5	V
$V_{I\ max\ TTL}$	Input Voltage	TTL	-0.5		V_{CC} +0.5	V
$I_{I\ max\ ECL}$	Input Current	ECL	-1.0		1.0	mA
$I_{I\ max\ TTL}$	Input Current	TTL	-1.0		1.0	mA
T_S	Operating Temperature	Channel	-55		+150	°C
T_O	Storage Temperature		-65		+175	°C
$\theta_{j\text{-}a}$	Thermal Resistance	Junction - Case		6		°C/W

DC Characteristics

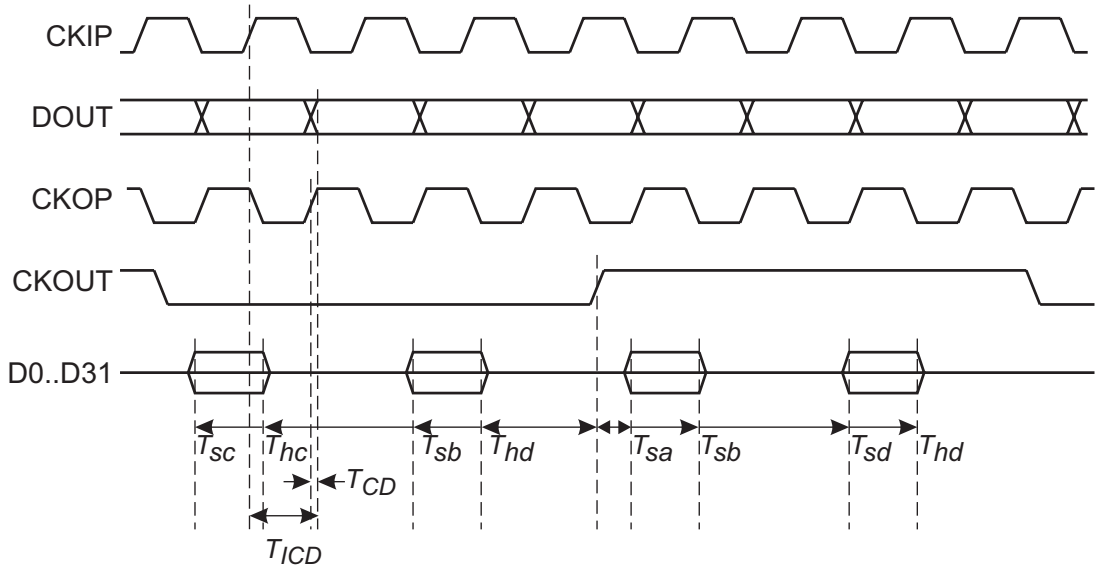
T_{CASE} = - 5 °C to +85 °C, appropriate heat sinking may be required.
All voltages in table are referred to VDD.
All currents in table are defined positive out of the pin.

Symbol:	Characteristic:	Conditions:	MIN.:	TYP.:	MAX.:	UNIT:
V_{EE}	Negative Supply Voltage		-5.40	-5.20	-5.00	V
V_{CC}	Positive Supply Voltage		4.75		5.25	V
$I_{EE,GD16131}$	Negative Supply Current (GD16131)				-286	mA
$I_{CC,GD16131}$	Positive Supply Current (GD16131)				26	mA
$I_{EE,GD16132}$	Negative Supply Current (GD16132)				-234	mA
$I_{CC,GD16132}$	Positive Supply Current (GD16132)				78	mA
V_{IH} , *ECL*	ECL Input HI Voltage		-1100		-700	mV
V_{IL} , *ECL*	ECL Input LO Voltage	Note 1	V_{TT}		-1500	mV
I_{IH} , *ECL*	ECL Input HI Current	$V_{IH\ max}$			25	µA
I_{IL} , *ECL*	ECL Input LO Current	$V_{IL\ max}$	-25			µA
V_{OH} , *ECL*	ECL Output HI Voltage	Note 2	-1000		-500	mV
V_{OL} , *ECL*	ECL Output LO Voltage	Note 2	V_{TT} - 100		-1600	mV
I_{OH} , *ECL*	ECL Output HI Current	Note 3	20	23	30	mA
I_{OL} , *ECL*	ECL Output LO Current	Note 3	-2	5	8	mA
V_{IH} , *TTL*	TTL Input HI Voltage		2		V_{CC}	V
V_{IL} , *TTL*	TTL Input LO Voltage		0		0.8	V
I_{IH} , *TTL*	TTL Input HI Current	$V_{IH\ max}$			100	µA
I_{IL} , *TTL*	TTL Input LO Current	$V_{IL\ min}$	-100			µA
V_{OH} , *TTL*	TTL Output HI Voltage	I_{OH} = *3 mA*	2.4		V_{CC}	V
V_{OL} , *TTL*	TTL Output LO Voltage	I_{OL} = *3 mA*	0		0.8	V

Note 1: V_{TT} = -2.0 V.
Note 2: R_{load} = 50 Ω to V_{TT}.
Note 3: Not tested, consistent with V_{OH} and V_{OL} tests.

AC Characteristics – GD16131

T_{CASE} = -5 °C to +85 °C, appropriate heat sinking may be required.

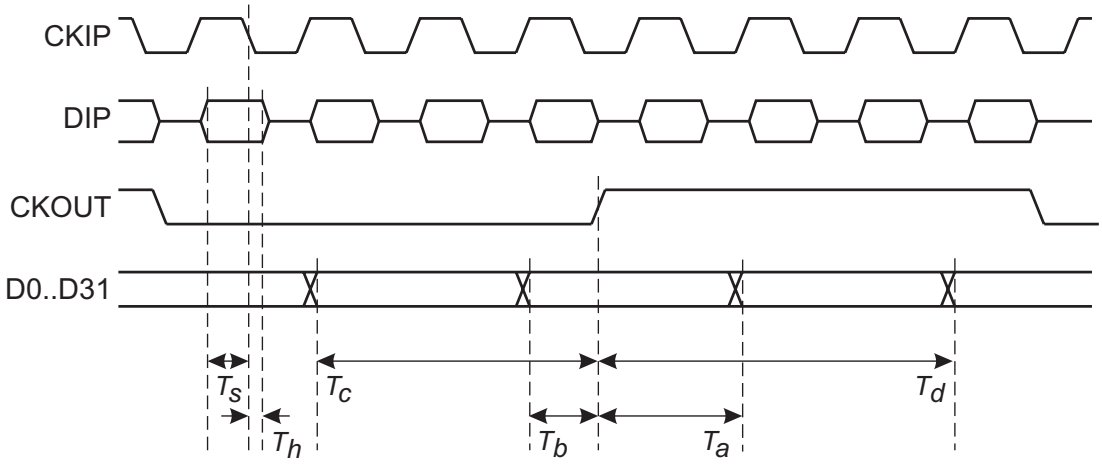


Symbol:	Characteristic:	Conditions:	MIN.:	TYP.:	MAX.:	UNIT:
T_{ICD}	DoxP/N output from CKIP/N		300	530	920	ps
T_{CD}	CKOP/N shift from DoxP/N		-100		100	ps
T_{sa}	Dyy set-up from CKOUT	SEL2/1: 0,0	-2000			ps
T_{ha}	Dyy hold from CKOUT	SEL2/1: 0,0			500	ps
T_{sb}	Dyy set-up from CKOUT	SEL2/1: 0,1	3X -2000			ps
T_{hb}	Dyy hold from CKOUT	SEL2/1: 0,1			3X +500	ps
T_{sc}	Dyy set-up from CKOUT	SEL2/1: 1,0	2X -2000			ps
T_{hc}	Dyy hold from CKOUT	SEL2/1: 1,0			2X +500	ps
T_{sd}	Dyy set-up from CKOUT	SEL2/1: 1,1	X -2000			ps
T_{hd}	Dyy hold from CKOUT	SEL2/1: 1,1			X +500	ps

Note: The value X is dependant of the clock frequency: X = 1/F × 1/4 × 8 = 2/F

AC Characteristics – GD16132

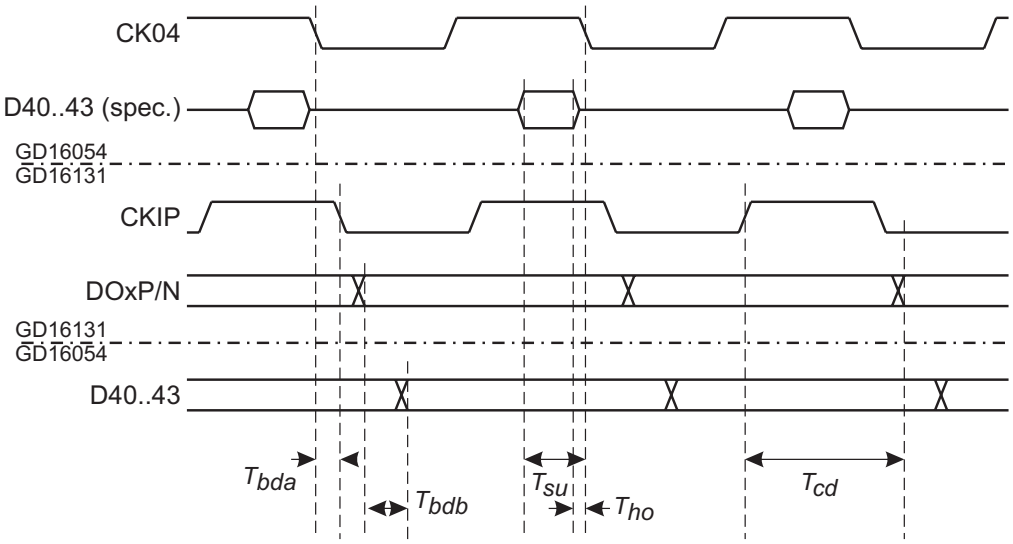
T_{CASE} = -5 °C to +85 °C, appropriate heat sinking may be required.

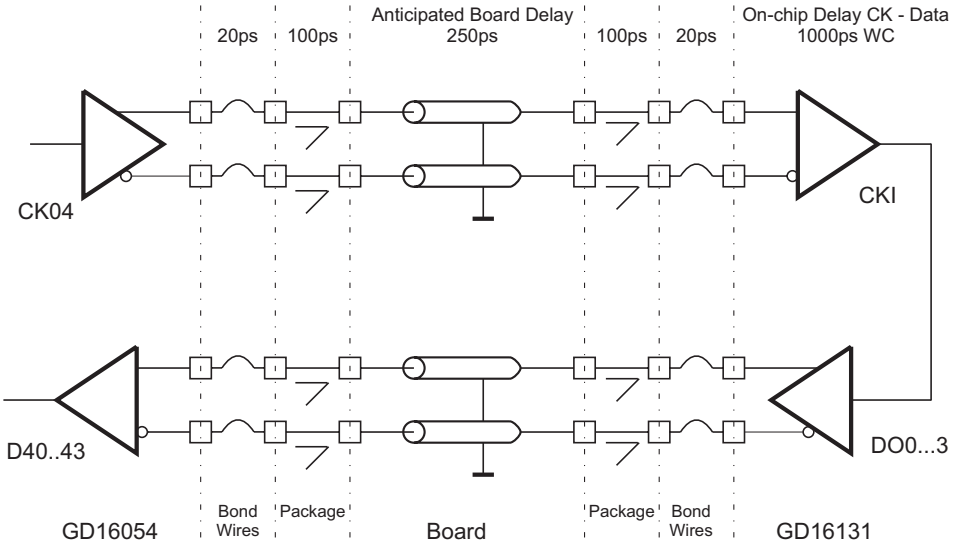


Symbol:	Characteristic:	Conditions:	MIN.:	TYP.:	MAX.:	UNIT:
T_S	DIxP/N output from CKIP/N		800			ps
T_h	DIxP/N hold from CKIP/N				0	ps
T_a	Dyy output from CKOUT	SEL2/1: 0,0	250		1500	ps
T_b	Dyy output from CKOUT	SEL2/1: 0,1	3X +250		3X+1500	ps
T_c	Dyy output from CKOUT	SEL2/1: 1,0	2X +250		2X+1500	ps
T_d	Dyy output from CKOUT	SEL2/1: 1,1	X +250		X+1500	ps

Note: The value X is dependant of the clock frequency: X = 1/F × 1/4 × 8 = 2/F

Counter-directional Clocking Schema – GD16131/GD16054





Symbol:	Characteristic:	Conditions:	MIN.:	TYP.:	MAX.:	UNIT:
T_{bd}	Board propagation delay between GD16554 and GD16131 (sum of clock and data del.)	Note 1	0		400	ps
T_{su}	GD16054 Data Input set-up from Clock Output	Note 1	280	400	600	ps
T_{ho}	GD16054 Data Input hold from Clock Output	Note 1	-175	-250	-375	ps
T_{cd}	GD16131 Data Output from Clock Input	Note 1	300	530	920	ps

Note 1: The above figures are based on layout parameters extractions and best assumptions. They give a hint of the magnitude of the figures and feasibility of the Counter-Directional clocking method. The maximal T_{bd} is calculated as follows:

$T_{bd}\ max = T_{bda}\ max + T_{bdb}\ max = 1.5 \times 1/622\text{MHz} - 4 \times (T_{pack} + T_{bond}) - T_{su}\ max - T_{cd}\ max$
$0 > T_{bd}\ min = 0.5 \times 1/622\text{MHz} - 4 \times (T_{pack} + T_{bond}) + T_{ho}\ min - T_{cd}\ min$

All efforts to keep T_{cd} as low as possible have been made. Please note that T_{bd} is the total round-trip board delay for both clock and data path.

Package Outline

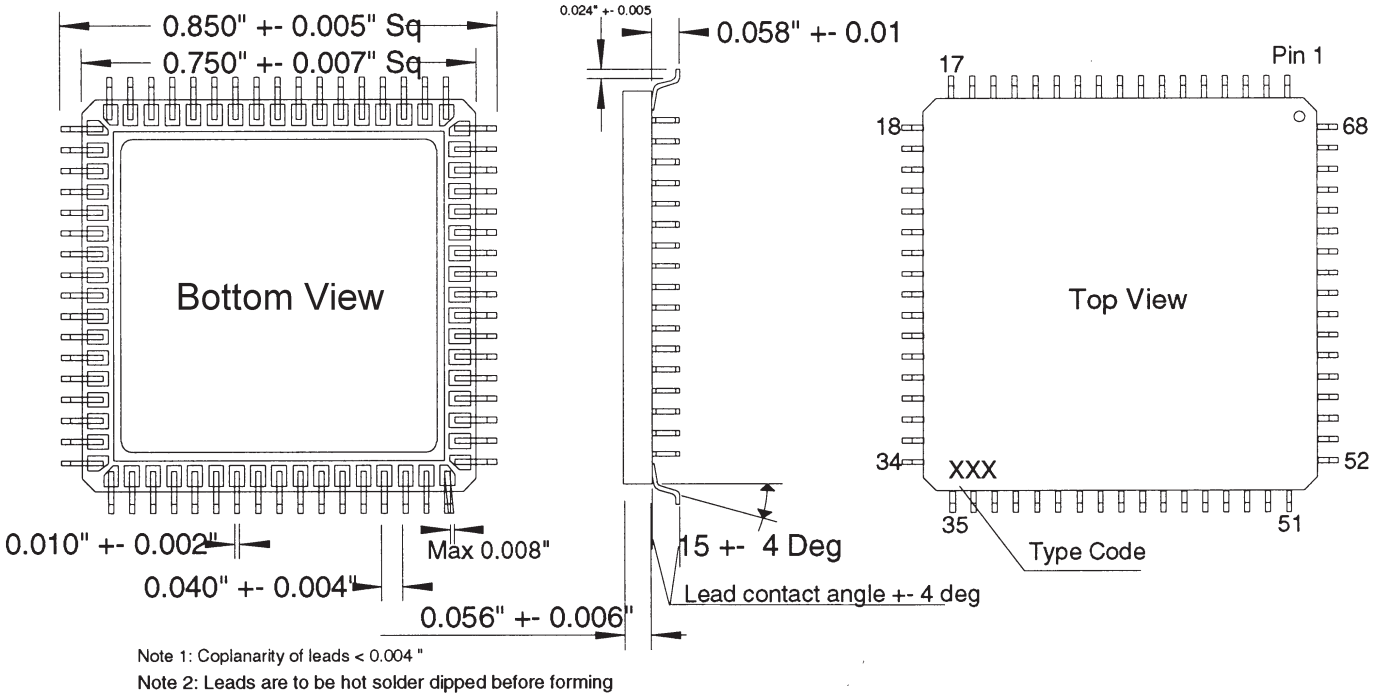


Figure 3. *Package 68 pin MLC (Gullwings) - All dimensions are in inch.*

Device Marking

Figure 4. *Device Marking - Bottom View*

Ordering Information

To order, please specify as shown below:

Product Name:	Type:	Package Type:	Case Temperature Range:
GD16131-GLP	MUX	68 pin MLC	-5...+85 °C
GD16132-GLP	DeMUX	68 pin MLC	-5...+85 °C

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