EISA 9010BV

EISA Bus Master Interface Chip for National SONIC-T DP83934 or SONIC DP83932 LAN Controller*

September 1992
Patent Pending

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Features

- **EISA Bus Master Interface for National DP83932 or DP83934 Ethernet Controller**
- **Supports EISA Burst Mode Data rates to 33 MBytes/sec**
- **BIOS PROM and Node ID PROM support**
- **25 MHz or 33 MHz Clock**
- **Direct connect to System Bus of all Host Interface Control Signals**
- **Low power CMOS in 128 Pin Plastic QFP Package**

General Description

The EISA 9010BV is designed to provide the most compact, inexpensive and highest performance EISA bus master interface for adapter boards that use the DP83932/4 LAN controller from National Semiconductor.

Use of the PLX Technology 90X0 series of bus master chips minimizes hardware and software development costs and time because similar adapter hardware and driver designs can be used for EISA, AT or Micro Channel applications.

The EISA 9010BV is an enhanced version of the EISA 9010. The EISA 9010BV may not function in boards designed for the EISA 9010. Please consult PLX for more information.

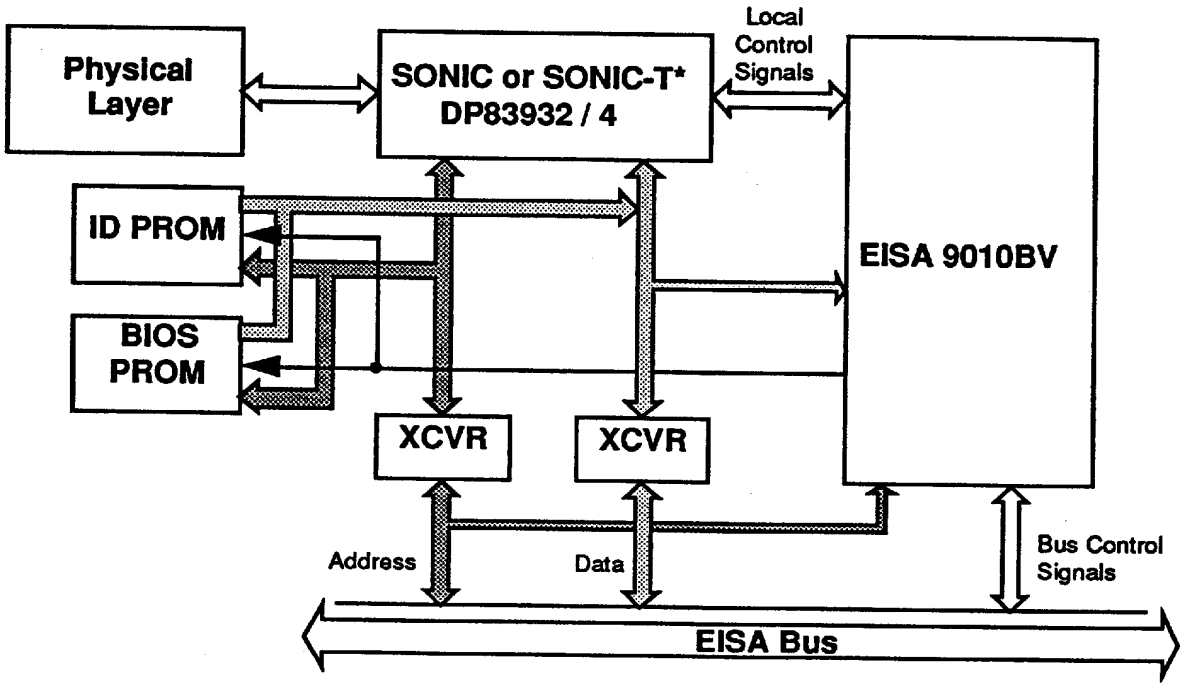

FIGURE 1. Typical Adapter Block Diagram

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SECTION 1 - INTRODUCTION

EISA 9010BV GENERAL DESCRIPTION

The EISA 9010BV is designed to provide the most compact, inexpensive and highest performance EISA bus interface for boards which use the National Semiconductor DP83932/4.

EISA bus master adapters which use National Semiconductor LAN controllers and the EISA 9010BV offer substantial performance advantages over slave adapters as LAN performance is significantly enhanced by the more efficient protocol processing of the DP83932/4. The bus master implementation frees the host processor from managing bus data transfer operations, which improves overall system performance.

Using the PLX Technology 9000 series of bus master chips also reduces total hardware and software development costs for LAN adapter manufacturers designing EISA, Micro Channel and AT compatible boards. In addition to the EISA 9010BV interface chip, PLX Technology provides the MCA 9010 and AT 9010, which are Micro Channel and AT bus master chips that have local interfaces identical to the EISA 9010BV. Therefore, by using the 9000 series, similar hardware designs and software drivers can be used for all three buses; EISA, AT and Micro Channel.

The EISA 9010BV is an enhanced version of the EISA 9010. The EISA 9010BV may not function in boards designed for the EISA 9010. Contact PLX for differences which may affect your board design.

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EISA 9010BV FUNCTIONS

Data Transfer Modes

The EISA 9010BV supports 32 bit Burst Data Transfers at up to 33 Megabytes per second of instantaneous data transfer rate. In addition, the EISA 9010BV supports slave mode for initialization of registers and access to other adapter board slave devices such as BIOS ROM, Node ID PROM or other memory and I/O devices.

Configuration Registers

The EISA 9010BV contains five internal configuration registers. The configuration registers contain configuration data which is loaded from the host during I/O setup. Included in these registers are the interrupt request level, PREEMPT timer configuration, Port select data, data size, I/O address decode bits, and PROM address decode bits. The EISA 9010BV also provides four external user bits for application specific configuration information.

The EISA card ID information is supplied externally to the EISA 9010BV and is contained in the Node ID PROM.

Specific EISA 9010BV functions

EISA 9010BV major functions include:

1. **Master Control Signal Protocol Converter.** The chip converts all handshakes of the local controller to EISA signals.
2. **Slave controller.** The EISA 9010BV includes an EISA slave interface for control of adapter board slave devices.
3. **Address decoder.** The EISA 9010BV decodes host address bits LA16-LA13, LA11-LA2 and contains an enable pin for an external LA31-LA17 or LA24-LA17 address decoder. The EISA 9010BV decodes these addresses to generate chip selects and access configuration registers.
4. **Interrupt generator.** The EISA 9010BV can generate one of four host interrupts from one local interrupt, programmable through configuration registers.
5. **External Buffer Controller.** The EISA 9010BV generates all buffer enable and direction signals for external address and data transceivers.
6. **Clock.** The EISA 9010BV runs from crystal or TTL oscillator and generates a 25 MHz or 33 MHz clock for external and internal use.
7. **User programmable configuration bits.** The EISA 9010BV provides up to four external bits which can be configured through the configuration registers.
8. **Bus drivers.** All control signals generated by the EISA 9010BV drive the EISA bus directly, without requiring external drivers.
9. **PREEMPT Timer.** Through the configuration registers the user may program a maximum time, 55 BCLKs or 23 BCLKs, which the adapter may hold the bus.
10. **BURST Transfer Address Controller.** During EISA BURST transfers, the EISA 9010BV generates A(2-9) to provide pipelined addresses required by the EISA bus.
11. **Adapter ID mapping.** The adapter ID number is mapped into I/O space to allow the option to implement the adapter ID in an ID PROM.

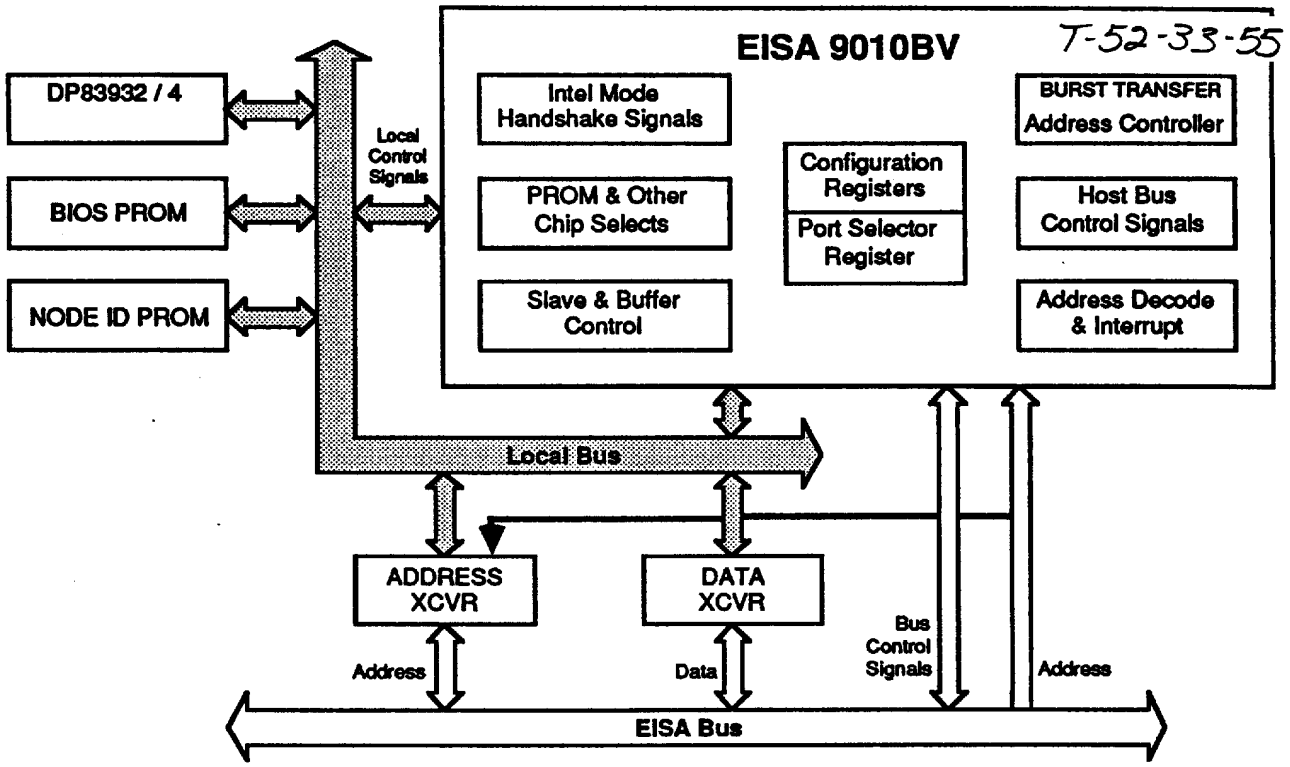

FIGURE 2. EISA 9010BV Functional Block Diagram

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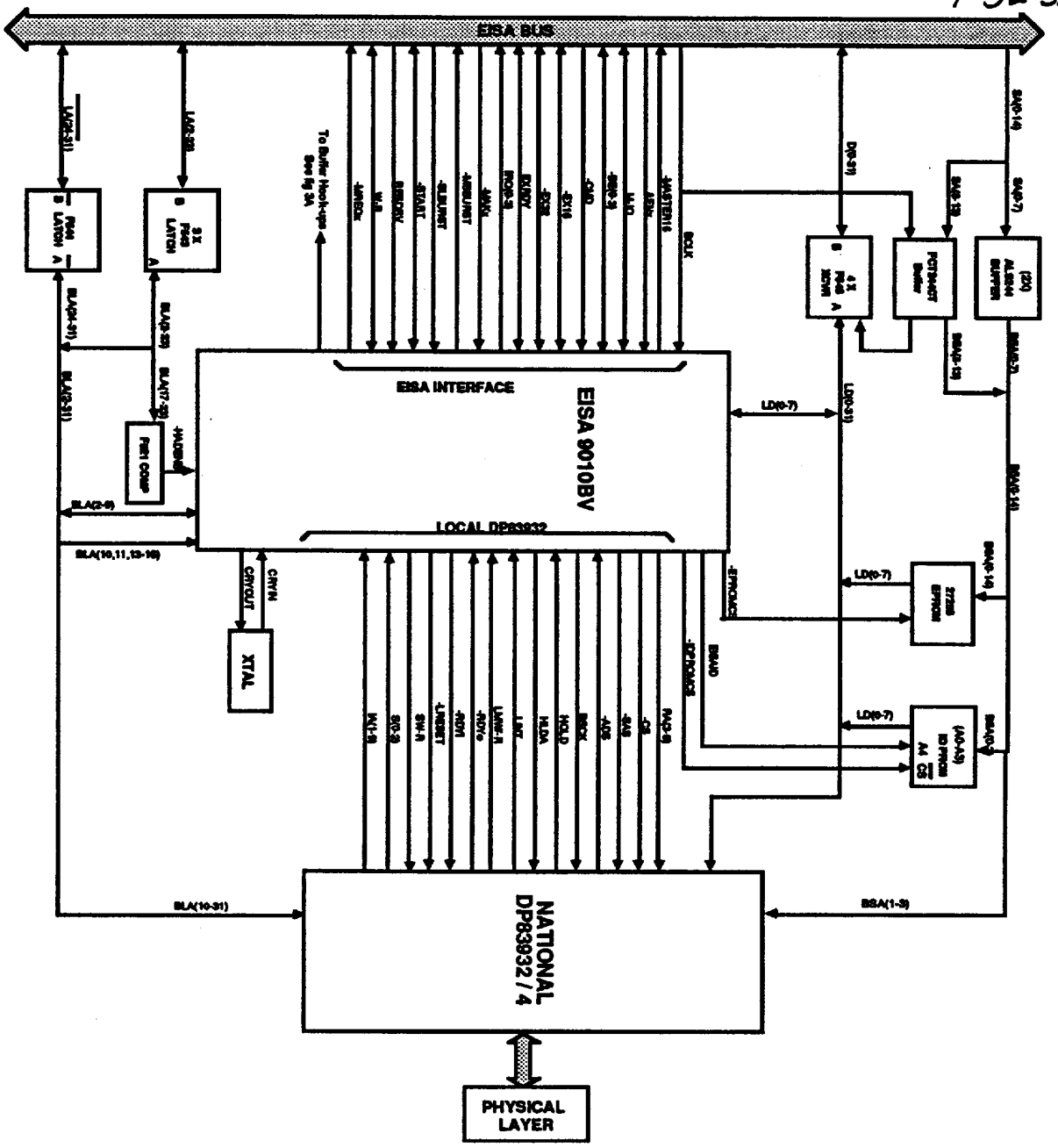

Figure 3. Low Cost EISA Direct Bus Master

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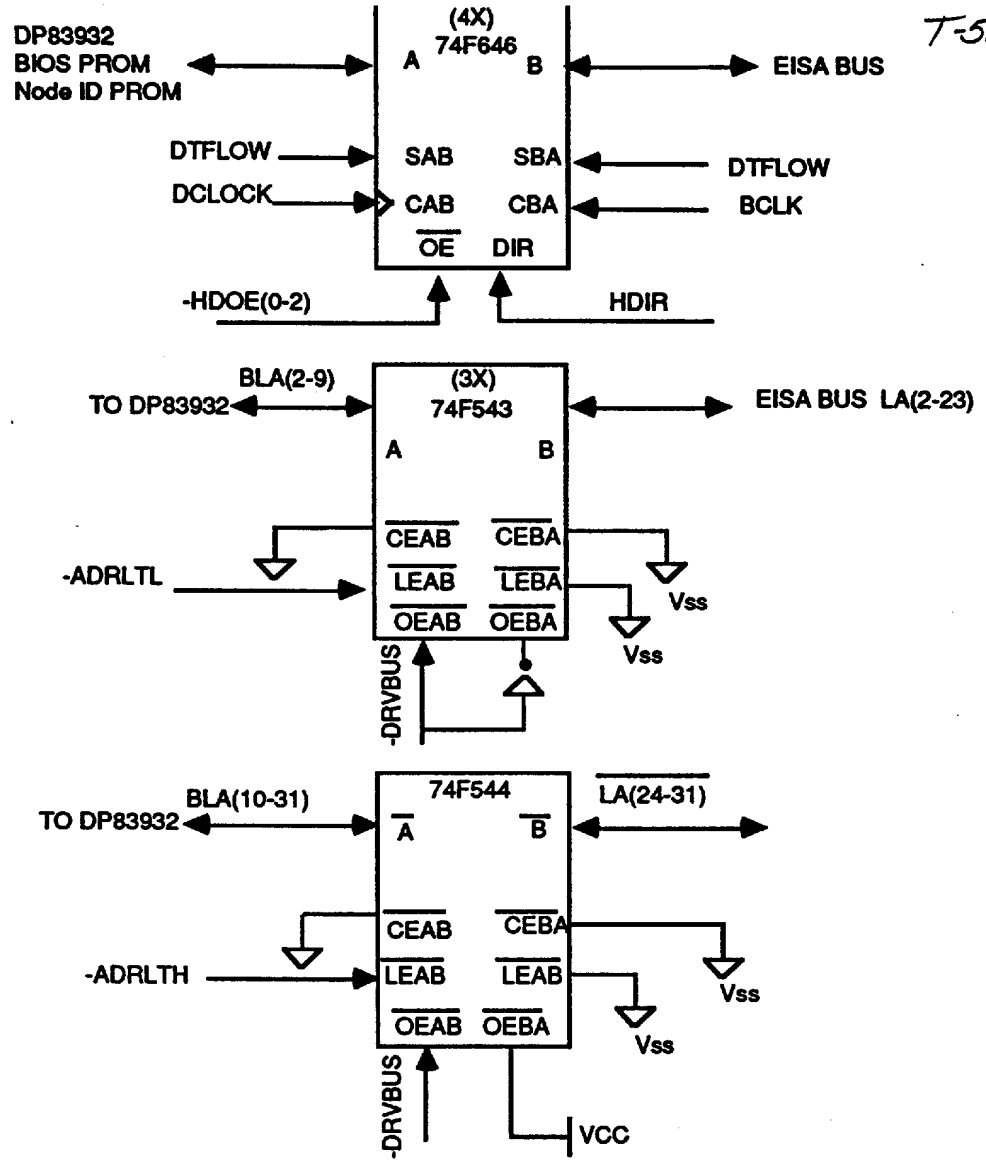

BUFFER HOOK-UPS
FIGURE 3A

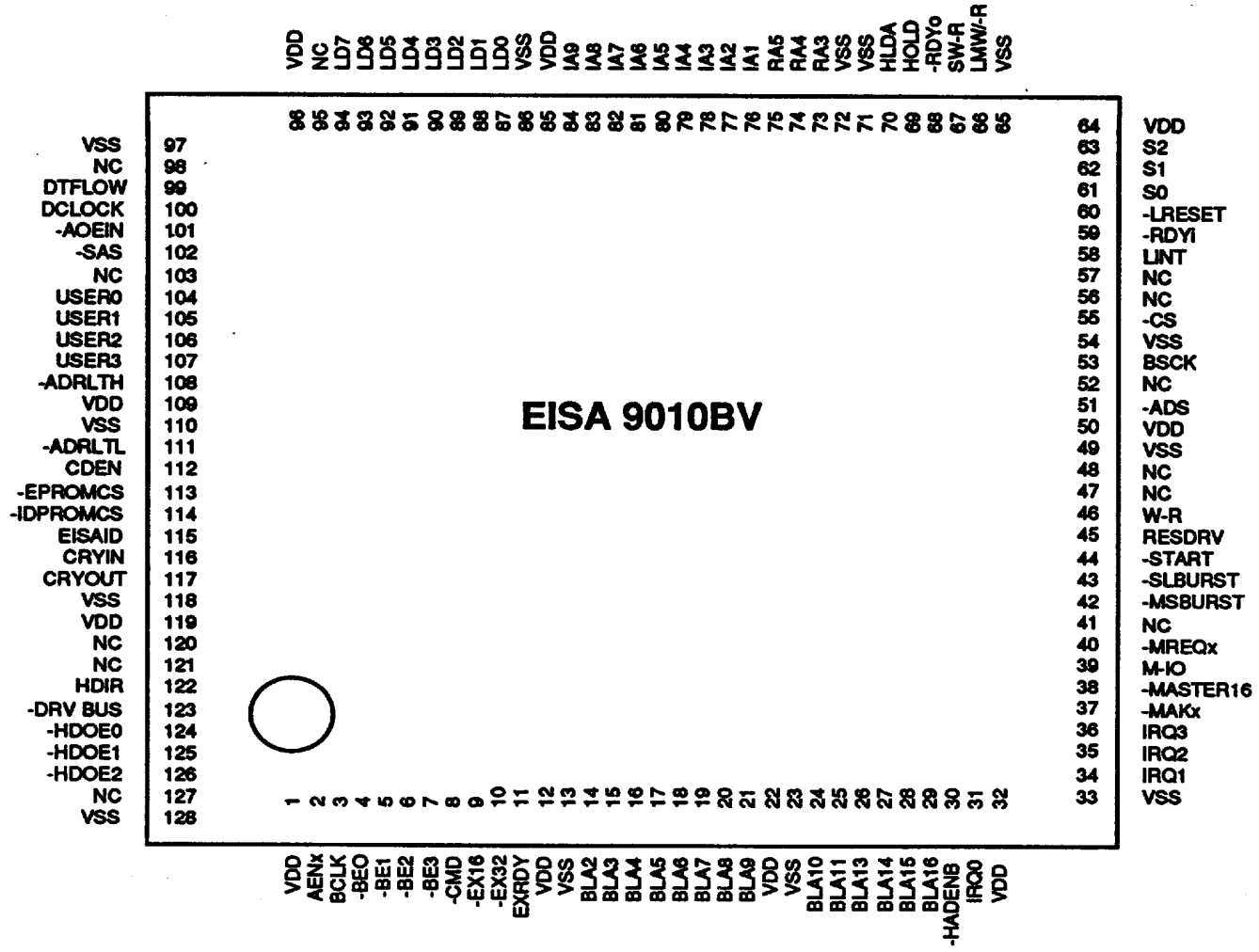

Figure 4.
Pin Out

SECTION 2 - CONFIGURATION REGISTERS AND ADDRESS DECODING T-52-33-55

The EISA 9010BV decodes the EISA Address signals to select the -CS signal, the Node ID PROM (the EISA board ID is included in the Node ID PROM), the BIOS PROM and the EISA 9010BV's five internal configuration registers. These five registers provide essential configuration information to the EISA 9010BV and the Ethernet adapter board. They are loaded at power-up and may be accessed dynamically through I/O slave cycles.

The -CS, Node ID PROM and four of the five configuration registers may be accessed through an ISA I/O adress as well as an EISA slot specific address. The EISA 9010BV offers the option of using ISA addressing to simplify converting software drivers written for AT boards to EISA board drivers. For boards with software drivers which use EISA specific addressing, the AT addressing mode is not required. Bit 4 in Register 1 enables ISA addressing.

ADDRESS DECODING

In accordance with the EISA specification, "z" refers to the slot number.

-CS Address. This signal may be activated on either a slot-specific basis or through an ISA decode procedure. Bit 4 in Configuration Register 1 enables the ISA addressing mode.

If slot-specific decode mode is selected , then -CS is selected by Address 0z000h to 0z050h.

If the ISA slot-specific address mode is selected (Bit 4 of Register 1= 1), then-CS is selected by the ISA Address indicated in Register 1, Bits 5-7, in addition to the slot-specific addresses.

EISA ID and Node ID PROM Address Both the EISA ID and the Ethernet Address reside in the same ID PROM. The four byte EISA ID and the Node ID PROM are selected through the EISA ID, -IDPROMCS, LA(2-11) and SA(0-3) signals as follows:

EISA Address (LA 2-11)	-IDPROMCS	EISA ID (A4)	System Address (SA3-0)	
0zC80h-83h	Active(0)	Active(1)	0h	EISA ID, First Byte
	Active(0)	Active(1)	1h	EISA ID, Second Byte
	Active(0)	Active(1)	2h	EISA ID, Third Byte
	Active(0)	Active(1)	3h	EISA ID, Fourth Byte
0zC90h-97h	Active(0)	Inactive(0)	0-5h	6 Ethernet ID Bytes
	Active(0)	Inactive(0)	6-7h	Spare PROM Bytes

Note: The EISA ID pin of the EISA 9010BV and -IDPROMCS signals are decoded from the EISA address and byte enable signals. The EISA ID pin of the EISA 9010BV should be connected to the PROM address pin A4. The System Address (SA) signals are connected to the ID PROM through buffers as shown in figure 3. A typical PROM address map is as follows:

PROM Address A4-A0 (EISA ID plus SA3-0)	Data
00 - 05h	6 Ethernet ID Bytes
06 - 07h	Spare PROM Bytes
08 - 0Fh	Not used
10h	EISA ID, First Byte
11h	EISA ID, Second Byte
12h	EISA ID, Third Byte
13h	EISA ID, Fourth Byte
14 - 1Fh	Not used

-EPROMCS Address This BIOS PROM chip select is decoded from address bits LA(13-16) and -HADENB. The LA(13-16) bits are programmable in Configuration Register 2, Bits 2-5. -HADENB is an input to the EISA 9010BV which is an external decode of LA(23-17) or LA(31-17).

Configuration Register Address The five configuration registers reside in the EISA configuration space at 0zC8Xh where "z" is the slot number and "X" is the register address.

CONFIGURATION REGISTERS

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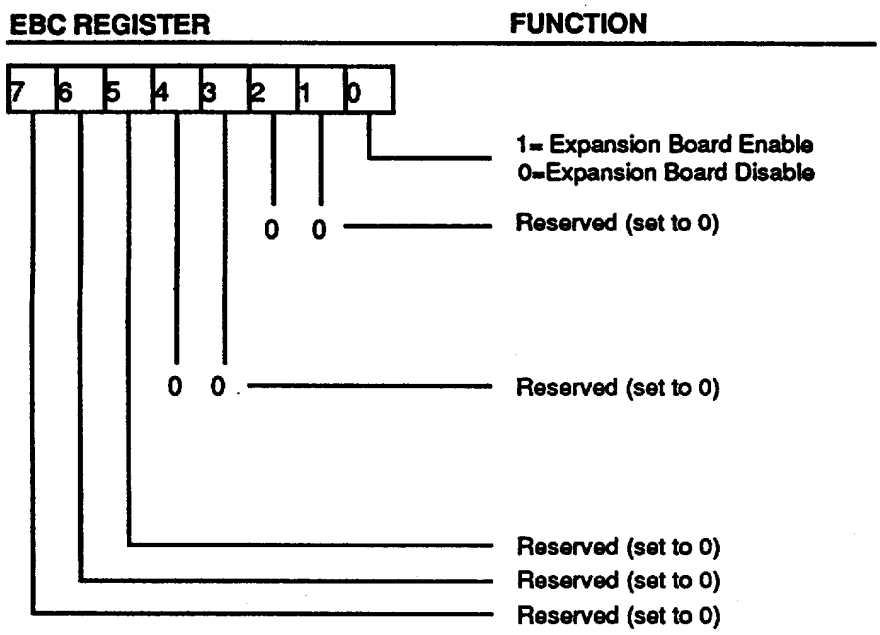
EBC Register- Expansion Board Control Bits Register; at 0zC84h



Bit 0 - Enables Expansion Board

Bit 1-7 - Reserved

All register bits default to 0.

Register 0 ; at 0zC88h

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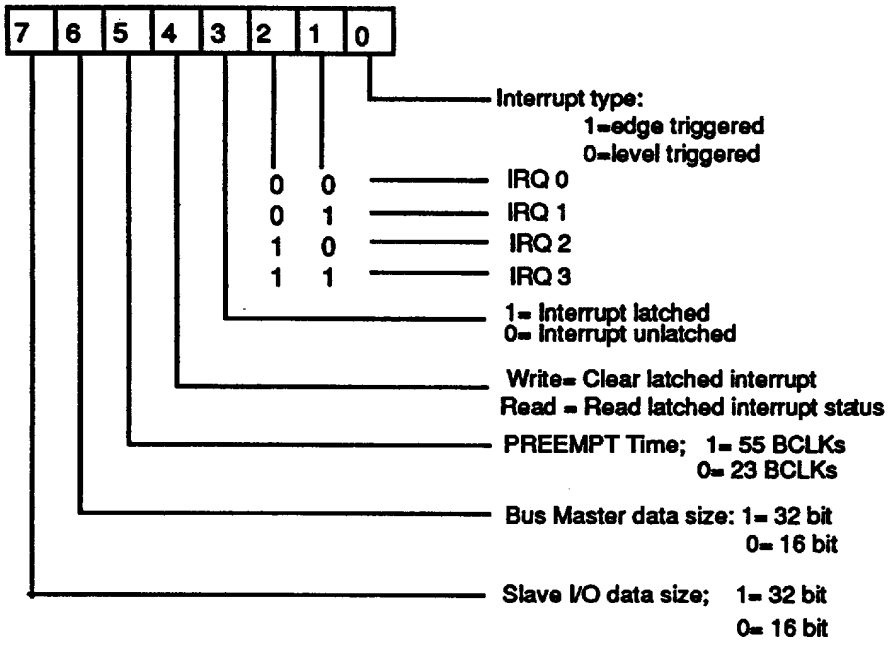
This register contains configuration data that is written by the host during I/O set-up.

WRITE / READ

REGISTER 0 **FUNCTION**



Bit 0 - Interrupt types: This bit defines whether the IRQ0-IRQ3 are level sensed or edge triggered.

Bit 0= 1, edge triggered

Bit 0= 0, level triggered (default)

Bit 1,2 - These bits select which EISA interrupt level is used when the DP83932/4 asserts its interrupt request line.

Bit 3 - This bit specifies whether the interrupt is latched or unlatched; 1= latched mode. 0= unlatched mode (default)

Bit 4 - The user can write this bit to 0 to clear the latch mode interrupt and read this bit for latched interrupt status.

Bit 5 - This bit specifies the amount of time the EISA 9010BV may hold the bus after a PREEMPT condition. When this bit is set to 1, the EISA 9010BV allows the DP83932/4 to hold the bus 55 BCLKs after PREEMPT. At this point, the EISA 9010BV removes HLDA to the DP83932/4 which allows the DP83932/4 nine BCLKs to release the bus. When this bit is set to 0, the EISA 9010BV holds the bus for 23 BCLKs after PREEMPT before removing HLDA.

Bit 6 - This bit specifies the data width for bus master transfers. If this bit is set to 1, the bus master data size is 32 bits. If set to zero, the bus master data size is 16 bits. The DP83932/4 is normally set to 32 bits.

Bit 7 - This bit specifies the data width for slave access to the DP83932/4. This bit is dependent on the DP83932/4 and I/O board. When set to 1, the slave I/O data size is 32 bits. When set to 0, the data size is 16 bits. The DP83932/4 is normally set to 16 bits.

All register bits default to 0.

Register 1 ; at I/O address 0zC89h

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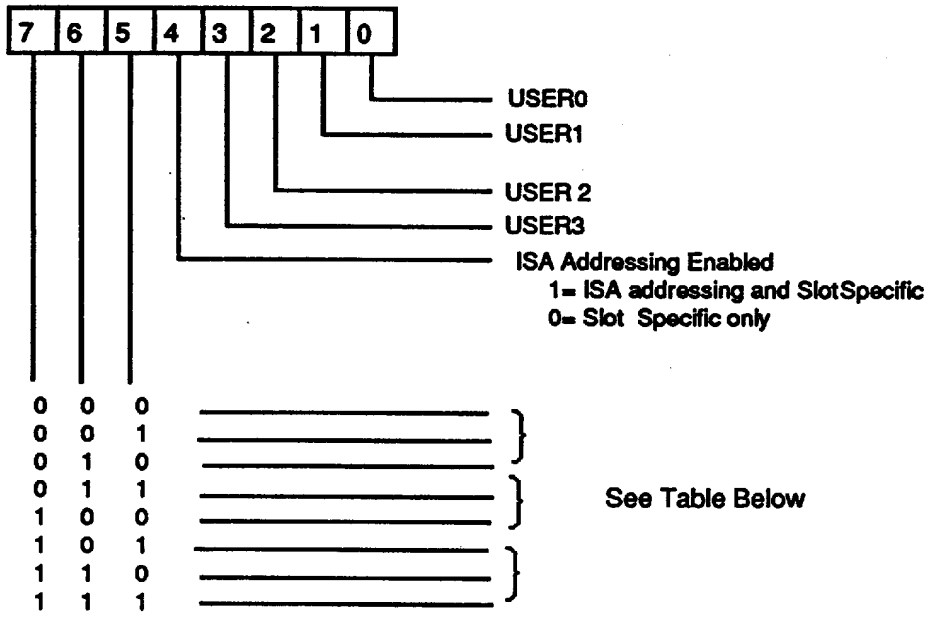
This register is loaded at power-up during I/O board configuration. It is used to control external logic through bits 0-3. Register 1 also contains the ISA alias I/O address decode range to select the I/O address of the board in ISA mode.

WRITE / READ

REGISTER 1 **FUNCTION**



BITS 7 6 5	Base Range	-CS	EBC Register	Reg 0	Reg 1	Reg 2	Reg 3	Node ID	EISA ID
0 0 0	100-11F	110-11F	Not Accessible	108	109	10A	10F	100-105	Not Accessible
0 0 1	120-13F	130-13F	"	128	129	12A	12F	120-125	"
0 1 0	140-15F	150-15F	"	148	149	14A	14F	140-145	"
0 1 1	160-17F	170-17F	"	168	169	16A	16F	160-165	"
1 0 0	300-31F	310-31F	"	308	309	30A	30F	300-305	"
1 0 1	320-33F	330-33F	"	328	329	32A	32F	320-325	"
1 1 0	340-35F	350-35F	"	348	349	34A	34F	340-345	"
1 1 1	DISABLED	-	-	-	-	-	-	-	-

Bits 0-3 - These bits connect directly to the USER_PINs and allow Configuration Register control of external logic.

Bits 5-7 - These bits select the I/O address of the board in ISA mode.

All register bits default to 0.

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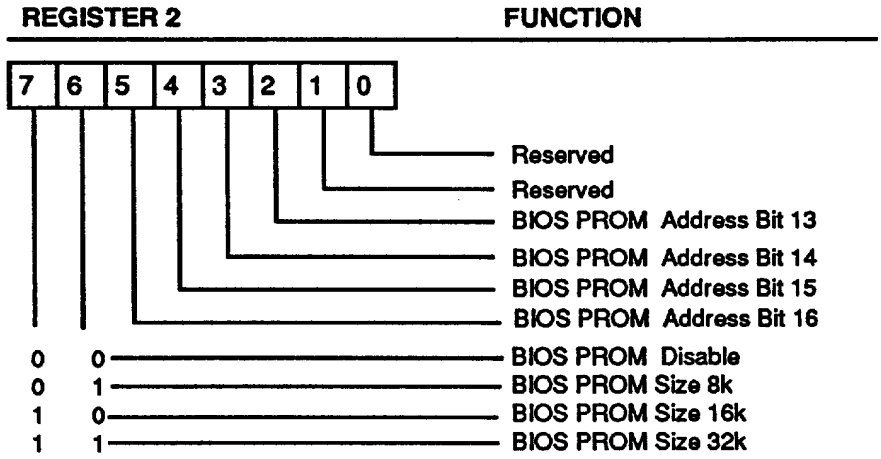
Register 2; at I/O address 0zC8Ah

This register selects the BIOS PROM address range and the BIOS PROM size. The BIOS PROM starting address and size is placed in this register during card configuration. For BIOS PROM selection, address bits A23-A13 are specified below:

A23	A22	A21	A20	A19	A18	A17	A16	A15	A14	A13
0	0	0	0	1	1	0	bit5	bit4	bit3	bit2

The adapter board must externally decode address bits LA23-LA17 and connect the result of this decode to the -HADENB pin of the EISA 9010BV. For 32 bit addresses the board must externally decode address bits LA31-LA17. Note that the BIOS PROM starting address must be on a memory boundary equal to the size of the BIOS PROM.

WRITE / READ



Bits 0-1 - Reserved

Bits 2-5 - These bits are compared against host addresses LA13-LA16 for determining a BIOS PROM access.

Bits 6-7 - These bits specify the BIOS PROM size as indicated above.

All register bits default to 0.

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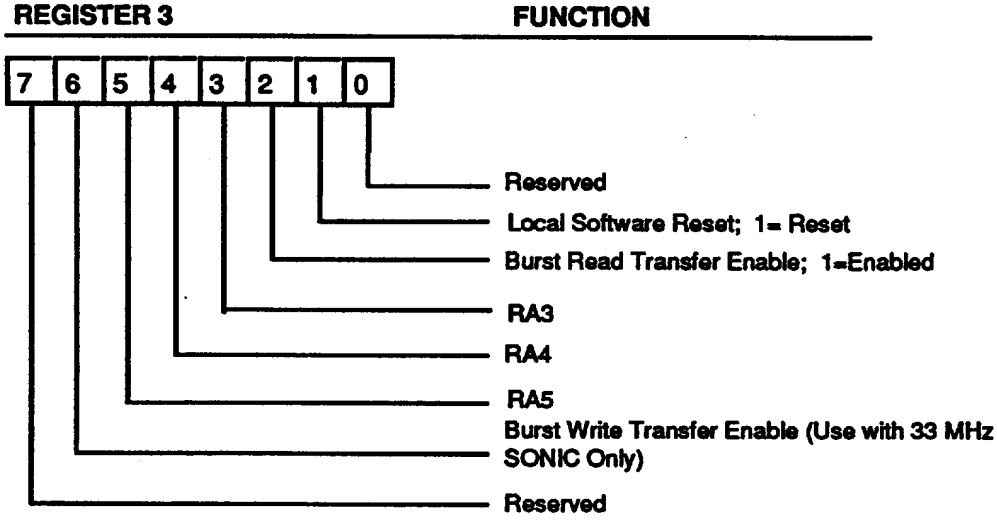
Register 3; at I/O address 0zC8Fh

This register enables EISA bus bursting and software RESET operation. It also contains DP83932/4 PORT select information. It is loaded at power-up during board configuration.



Bit 0 - Reserved

Bit 1 - When this bit is set to 1, it allows the system to RESET the EISA 9010BV by software. The contents of the EISA 9010BV's registers will not be RESET. The default condition is 0.

Bit 2 - EISA Burst Read transfer mode is enabled. 25 MHz or faster DP83932/4 is required.

Bits 3-5 - Address bits which provide DP83932/4 PORT select information.

Bit 6 - EISA Burst Write Transfer Mode is enabled. This mode should be used only with 33 MHz SONIC or SONIC-T controller.

Bit 7 - Reserved

All register bits default to 0.

SECTION 3 - PIN SUMMARY

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Pin Summary

Table 3.1 gives a summary of the host bus pins for the EISA 9010BV device. The Host Interface consists of the pins for the EISA bus. Table 3.2 gives a summary of the local interface pins. The Local interface consists of the pins for the DP83932/4 interface. The following abbreviations are used:

I/O - Input and Output Pin
I - Input Pin Only
O - Output Pin Only
TS - Three-state Pin
OC - Open Collector Pin
TP - Totem Pole Pin

Table 3.1 Host Interface - EISA Bus Pin Summary

Pin Names	Number of Signals	Input/ Output	Pin Type	Pin Drive (mA)
AENx	1	I	-	-
BCLK	1	I	-	-
-BE(0-3)	4	I/O	TS	24
-CMD	1	I	-	-
-EX16	1	I/O	OC	24
-EX32	1	I/O	OC	24
EXRDY	1	I/O	OC	24
IRQ(0-3)	4	O	OC/TP*	6
-MAKx	1	I	-	-
-MASTER16	1	O	OC	24
M-IO	1	I/O	TS	24
-MREQx	1	O	TP	6
-MSBURST	1	O	TS	24
-SLBURST	1	I	-	-
-START	1	I/O	TS	24
RESDRV	1	I	-	-
W-R	1	I/O	TS	24
TOTAL PINS	23			

* OC in level triggered mode, TP in edge triggered mode.

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Table 3.2. Local Bus Pin Summary for National Semiconductor DP83932/4

Pin Names	Number of Signals	Input/ Output	Pin Type	Pin Drive (mA)
-ADS	1	I	-	-
BSCK	1	O	TP	4
CDEN	1	O	TP	4
CRYIN	1	I	-	-
CRYOUT	1	O		
-CS	1	O	TP	4
EISAID	1	O	TP	4
HLDA	1	O	TP	4
HOLD	1	I	-	-
LINT	1	I	-	-
RA(3-5)	3	O	TP	4
LMW/-R	1	I	-	-
-EPROMCS	1	O	TP	4
-IDPROMCS	1	O	TP	4
-RDYi	1	O	TP	4
-RDYo	1	I	-	-
-LRESET	1	O	TP	4
S(0-2)	3	I	-	-
SW-R	1	O	TP	4
-SAS	1	O	TP	4
USER(0-3)	4	O	TP	4
TOTAL PINS	28			

Table 3.3 Buffer Control, Address and Data Pins

Pin Names	Number of Signals	Input/ Output	Pin Type	Pin Drive (mA)
-ADRLTH	1	O	TP	4
-ADRLTL	1	O	TP	4
-AOEIN	1	O	TP	4
DTFLOW	1	O	TP	4
DCLOCK	1	O	TP	4
-DRV BUS	1	O	TP	4
-HADENB	1	I	-	-
HDIR	1	O	TP	4
-HDOE(0-2)	3	O	TP	4
IA(1-9)	9	I	-	-
BLA(2-9)	8	I/O	TS	4
BLA(10,11,13-16)	6	I	-	-
LD(0-7)	8	I/O	TS	4
TOTAL PINS	42			

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Table 3.4 Power, Ground and No Connect Pins

Pin Names	Number of Signals	Input/ Output	Pin Type	Pin Drive (mA)
NC	12	-	-	-
VDD	10	I	-	-
VSS	13	I	-	-
TOTAL PINS	35			

Table 3.5 Host Interface- EISA Bus Pin Description

Symbol	Signal Name	I/O	Pin Number	Function
AENx	Address Enable	I	2	This active high slot specific input signal indicates (when deasserted) that the EISA 9010BV may respond to address and I/O commands.
BCLK	Bus Clock	I	3	This active high input is provided for synchronizing EISA bus events with the host system clock. BCLK operates at a frequency 8.333 MHz with a duty cycle of 50 percent.
-BE(3) -BE(2) -BE(1) -BE(0)	Byte Enables	I/O	7 6 5 4	These active low I/O signals are the byte enables that identify the specific bytes addressed in a double word. These signals and the address lines LA(2-23), are pipelined from one cycle to the next -BE(3) enables the high byte (byte 3) of a double word while -BE(0) enables the low byte. During slave cycles, BE(0-3) are used to generate address bits 0 and 1.
-CMD	Command Strobe	I	8	This active low input signal provides timing control within the EISA bus cycle. The system board asserts this signal on the rising edge of BCLK, simultaneous with the deassertion of the -START signal.
-EX16	16 Bit Slave	I/O	9	This active low I/O signal indicates an EISA memory or I/O slave is capable of transferring 16 bits of data. It is driven during slave accesses to SONIC or SONIC-T or SONIC-T registers. During 16 bit bus master transfers the EISA 9010BV samples -EX16 on the rising edge of BCLK after -START is asserted. If this signal is not asserted the EISA 9010BV floats the -BE(0-3) and -START lines to allow the system board to perform a size translation. Once completed the system board asserts this signal and the EISA 9010BV completes the cycle.

-EX32	32 Bit Slave	I/O	10	This active low I/O signal indicates an EISA memory or I/O slave is capable of transferring 32 bit double word size. During 32 bit bus master transfers the EISA 9010BV samples -EX32 on the rising edge of BCLK after -START is asserted. If this signal is not asserted the EISA 9010BV floats the -BE(0-3) and -START lines to allow the system board to perform a size translation. Once completed the system board asserts this signal and the EISA 9010BV completes the cycle.
EXRDY	EISA Channel Ready Input and Output	I/O	11	This active high open collector signal lengthens a bus cycle from its standard one BCLK time. It is asserted by a memory or I/O device when it can not respond quickly enough. When EXRDY is low the EISA 9010BV inserts wait cycles (one BCLK) until memory brings this signal high. The EISA 9010BV pulls EXRDY low during slave cycles.
IRQ(3) IRQ(2) IRQ(1) IRQ(0)	Interrupt Request	I/O	36 35 34 31	These signals are used to inform the system of the completion of a task. IRQ(0-3) selection is programmable in the configuration registers. They may be programmed to active high totem pole or active low open collector.
-MAKx	Master Acknowledge	I	37	This active low slot specific signal is asserted by the system board to grant access to the EISA bus. The signal is in response to the EISA 9010BV asserting the -MREQx signal. The EISA 9010BV must release the EISA bus within 7.68 usec after this signal is deasserted.
-MASTER16	16 Bit Bus Master	O	38	When this three-state output signal is asserted the EISA 9010BV is a 16 bit bus master. This pin is programmable in the configuration registers.
M-IO	Memory or I/O	I/O	39	This three-state signal distinguishes a memory cycle from an I/O cycle. When this signal is high a memory cycle is in progress. When M-IO is low an I/O cycle is in progress, M-IO is pipelined from one EISA bus cycle to the next.
-MREQx	Master Request	O	40	This active low totem pole, slot specific, output signal is asserted by the EISA 9010BV to request EISA bus access. The system board asserts -MAKx in response to this signal.
-MSBURST	Master Burst	O	42	The EISA 9010BV asserts this active low output signal to indicate to the slave that it is executing burst cycles. Burst transfers are programmable in the configuration registers.
-SLBURST	Slave Burst	I	43	This active low input informs the EISA 9010BV that the addressed slave supports burst cycles.

-START	Start Command	I/O	44	This active low three-state signal indicates the beginning of an EISA bus access. It is asserted for one BCLK period after the address is valid on the bus.
RES DRV	Bus Reset	I	45	This active high input signal provides a hard reset to the EISA 9010BV chip. Internal logic is initialized by this signal and any transfer operations are aborted.
W-R	Write/Read	I/O	46	This Three-state pin indicates whether to perform an EISA bus write or read operation. When this pin is high a write operation is requested and when low a read.

Table 3.6 Local Bus Pin Description

Symbol	Signal Name	I/O	Pin Number	Function
-ADS	Address Strobe	I	51	This active low input signal informs the EISA 9010BV that the DP83932/4 has placed a valid address on the bus.
BSCK	Bus Clock	O	53	This active high clock provides the timing for the DP83932/4 DMA logic.
CDEN	Card Enable	O	112	This totem pole output is asserted when the I/O board has been enabled through the EBC Register.
CRYIN	Crystal Input	I	116	This input pin provides the timing for all synchronous operations in the EISA 9010BV. It connects to either a TTL clock signal or directly to a crystal.
CRYOUT	Crystal Output	O	117	This output signal connects directly to crystal oscillator.It is a no connect pin when the the CRYIN pin connects to a TTL clock signal.
-CS	Chip Select	O	55	The EISA 9010BV asserts this active low signal when it has detected an access to the DP83932/4 's I/O registers. The DP83932/4 's ISA I/O address is programmable in Configuration Register 1, (0zC89h).
HLDA	Bus Hold Acknowledge	O	70	This active high totem pole output signal indicates the EISA 9010BV has successfully gained access to the host bus. When the DP83932/4 receives this signal it begins bus master operation.
HOLD	Bus Hold Request	I	69	This active high input indicates the DP83932/4 needs to gain access to the host bus.
LINT	DP83932/4 Local Interrupt	I	58	This active high input is active when the DP83932/4 has an interrupt pending. The EISA 9010BV asserts one of four host interrupts when this signal isactive.The host interrupt line that is asserted is programmable in Configuration Register 0, bits 1 and 2.

RA(3-5)	Register Address 3-5	O	73,74,75	These three-state active high pins contain the contents of the DP83932/4 Port Selector Register. They determine one of the eight ports to be selected in the DP83932/4 when using ISA addressing.
-LRESET	Reset	O	60	This active low output signal is asserted and de-asserted synchronous to BSCK. It provides a hardware reset to the DP83932/4 .
LMW-R	Memory Write or Read	I	66	This input signal is low when a bus master read operation is requested and high for a bus master write operation.
-EPROMCS	BIOS PROM Output Enable	O	113	This active low output pin connects to the output enable pin (-OE) of the BIOS Boot PROM. The EISA 9010BV gates the data from the PROM onto the system data bus. The system memory address of the BIOS PROM is programmable in Configuration Register 2.
-IDPROMCS	ID PROM Output Enable	O	114	This active low output pin connects to the output enable pin (-OE) of the Node ID PROM. The EISA 9010BV gates the data from the Node ID PROM onto the system data bus. The system I/O address of the ID PROM is programmable in Configuration Register 1.
-RDYi	Ready to DP83932/4	O	59	This active low output signal informs the DP83932/4 of the completion of a memory cycle. When it is high, the DP83932/4 inserts wait states. This signal is sampled by the DP83932/4 synchronously with BSCK.
-RDYo	Ready from DP83932/4	I	68	This active low input from the DP83932/4 is used during system slave accesses to the DP83932/4 's I/O registers. This signal is asserted when the DP83932/4 has completed the I/O cycle and is synchronous to BSCK clock.
S(0-2)	DP83932/4 Bus Status	I	61, 62, 63,	These status signals from the DP83932/4 are used by the EISA 9010BV to enable/disable BURST transfers. They indicate the current DP83932/4 bus operation.
-SAS	Slave Address Strobe	O	102	EISA 9010BV asserts this output signal to indicate to the DP83932/4 that valid address is on the bus during a register write operation or when the DP83932/4 can begin sourcing data during a register read operation.
SW-R	Slave Read or Write	O	67	The EISA 9010BV asserts this output signal to inform the DP83932/4 whether the current access is a read or write to DP83932/4 registers.
USER3 USER2 USER1 USER0	User Defined Pins	O	107, 106, 105, 104	These totem pole output pins are controlled from Configuration Register 1 for each host interface. They control logic on the I/O board.

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Table 3.7 Buffer Control, Address and Data Pins

Symbol	Signal Name	I/O	Pin Number	Function
-ADRLTH	Address Latch High Bytes	O	108	This active low totem pole output signal connects to 74F544's and 74F543's A to B latch enable inputs, (High Bytes). Connect to -LEAB input of latch.
-ADRLTL	Address Latch Low Byte	O	111	This active low totem pole output signals connects to 74F543's A to B latch enable input (Low Byte). Connect to -LEAB input of latch.
-AOEIN	Address Input Enable	O	101	This active low totem pole output signal connects to 74F543's B to A output enable input. Connect to -OEBA for lower three address drivers.
BLA(2-9) BLA(10,11) BLA(13-16)	Buffered Latched Address (Local Address)	I/O I I	14, 15, 16 17, 18, 19, 20, 21, 24, 25, 26, 27, 28, 29	These active high input signals are the host address lines needed for I/O and BIOS PROM space decode. BLA(2-9) are outputs during Bus Master transfers.
DTFLOW	Clocked/Trans-parent input	O	99	This signal is used as the Clocked/Transparent input to the 74F646 transceiver/registers. Connect to SBA input of transceiver. Clocked is for bus master and transparent is for slave mode.
DCLOCK	Clock Pulse Input	O	100	This signal is used as a clock pulse input for 74F646 Transceiver/registers. Connect to CAB input of transceiver.
-DRV BUS	Drive EISA Bus	O	123	This active low totem pole output signal connects the 74F543's and 74F544's A to B output enable inputs. Connect to -OEAB input of transceiver.
-HADENB	Host Address Enable	I	30	This signal provides for an external decode of Host Address bits (17-23). This pin is used for BIOS PROM decode only.
HDIR	Host Data Direction	O	122	This totem pole output signal connects to the DIR pin of the 74F646 which gates the data bus between the adapter board and the EISA bus. When this pin is low, the host data bus is gated to the adapter board. When this pin is high the data bus from the adapter board is gated to the host data bus.

-HDOE(2) -HDOE(1) -HDOE(0)	Host Data Output	O	126 125 124	These active low totem pole output signals connect to the -OE pin of the 74F646s which gate data between the adapter board and the host bus. These pins are connected as indicated below: Host byte -HDOE pin 0 -HDOE(0) 1 -HDOE(1) 2 -HDOE(2) 3 -HDOE(2)
IA(1-9)	DP83932/4 lower order address	I	76, 77, 78 79, 80, 81 82, 83, 84	These inputs are connected to the A1-9 signals of the DP83932/4 and are used to load the EISA 9010BV's address counter. This address counter generates the lower order address bits to the host bus during BURST transfer cycles. For non-BURST master cycles, A(2-9) pass through the EISA 9010BV without modification.
LD(0-7)	Host Data	I/O	87, 88, 89, 90, 91, 92, 93, 94	These three-state data signals program Configuration Registers in the EISA 9010BV. The host processor may also read back the registers.

Table 3.8 Power, Ground and No Connect Pin Description

NC	No Connect	-	41, 47, 48 52, 56, 57, 95, 98, 103, 120, 121,127	No Connect
VDD	Power	I	1, 12, 22 32, 50, 64 85, 96, 109, 119	Five Volt Power Supply Pins
VSS	Ground	I	13, 23, 33 49, 54, 65 71,72,86 97,110, 118,128	Ground Pins

SECTION 4 - BUS CYCLE DESCRIPTION

This section describes EISA 9010BV local and EISA bus functionality with the 83932/4.

SLAVE CYCLES

In the slave mode, the EISA 9010BV monitors the address lines BLA (11:2) and -BE (3:0) for general I/O address decoding, slot-specific address decoding, and configuration register accessing. During the slave mode, -AENx has to be asserted low.

The configuration registers can be accessed through 8-bit I/O read or write cycles. These cycles are 6 BCLK periods long.

83932/4 Register Access

The 83932/4 registers are accessed through EISA slave I/O cycles. The EISA 9010BV decodes the system address and drives -CS, -SAS, RA (3-5) and SW-R to the 83932/4. The EISA 9010BV also drives the data direction signal, HDIR, to the data buffers to indicate whether the cycle is a read or a write.

-CS is valid for addresses 0z000h-0z050h.

EISA ID, Node ID and BIOS PROM Access

The EISA ID and Ethernet ID use the same ID PROM. The EISAID and -IDPROMCS signals are accessed through 8-bit I/O slave cycles. The EISAID signal should connect to the on board PROM address A4. The EISA 9010BV decodes the system address and drives the -EPROMCS for BIOS PROM access.

EISA ID, Node ID and BIOSPROM accesses are executed by the EISA 9010BV as 8 bit EISA slave cycles. EXRDY is not deasserted. The -IDPROMCS is valid for addresses 0zC80h-0zC83h, and 0zC90h-0zC97h.

Interrupts

The EISA 9010BV provides four interrupt request lines, IRQ(3:0). LINT from the 83932/4 asserts the appropriate EISA interrupt request signals. If the EISA interrupt request line is programmed in the latched mode, reading bit 4 of register 0 will clear the interrupt request signal.

MASTER CYCLES

Bus Request

The 83932/4 initiates an EISA bus request by asserting HOLD to the EISA 9010BV. When the EISA 9010BV detects HOLD, it drives -MREQx to the EISA bus and waits to receive -MAKx from motherboard. After the EISA 9010BV detects -MAKx, it will assert HLDA to the 83932/4 and will assert -DRVBUS to turn on 74F543 and 74F544 latching buffers.

Bus Arbitration

The centralized arbitration controller arbitrates the request, -MREQx ,and the system board asserts a bus grant signal, -MAKx, when the bus is available. An EISA bus master may be preempted by another device that requests use of the bus. The EISA 9010BV allows the 83932/4 to hold the bus for 55 BCLKs or 23 BCLKs from the preemption after sampling its -MAKx signal negated. At this point, the EISA 9010BV removes HLDA to the 83932/4 which allows 9 BCLKs for the 83932/4 to release the bus.

Burst and Non-burst Modes of Operation

The EISA 9010BV can be programmed for burst or non-burst data transfer modes. To execute burst cycles, burst mode must be enabled from configuration register 3. To start a burst cycle, the address must be 4 byte aligned, and subsequent addresses must be contiguous.

If burst mode is enabled, the EISA 9010BV will monitor the -SLBURST signal at the beginning of the transfer to determine if the slave device that was addressed is capable of executing burst cycles. If the slave device does not respond with an active -SLBURST, the EISA 9010BV will not execute burst cycles. (The EISA 9010BV only supports 32 bit burst cycles.)

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For mismatched translation EISA cycles, the EISA 9010BV will monitor the -EX32 signal at the beginning of the transfer to determine if the system memory it addressed has the same bus width. If the -EX32 signal is not active, the EISA 9010BV will function in the non-burst mode and will "back-off" the bus by floating -START, -LBE(2:0), and disabling -HDOE(0:2) to allow the motherboard to take control of the transfer.

1K Byte Page Address Boundary

The EISA 9010BV will not start a burst cycle if the 83932/4 address is at the 1K byte page boundary address. During the burst cycle, the EISA 9010BV provides the support to detect the 1K byte page address boundary. At the 1K byte boundary, the EISA 9010BV will exit out of burst mode.

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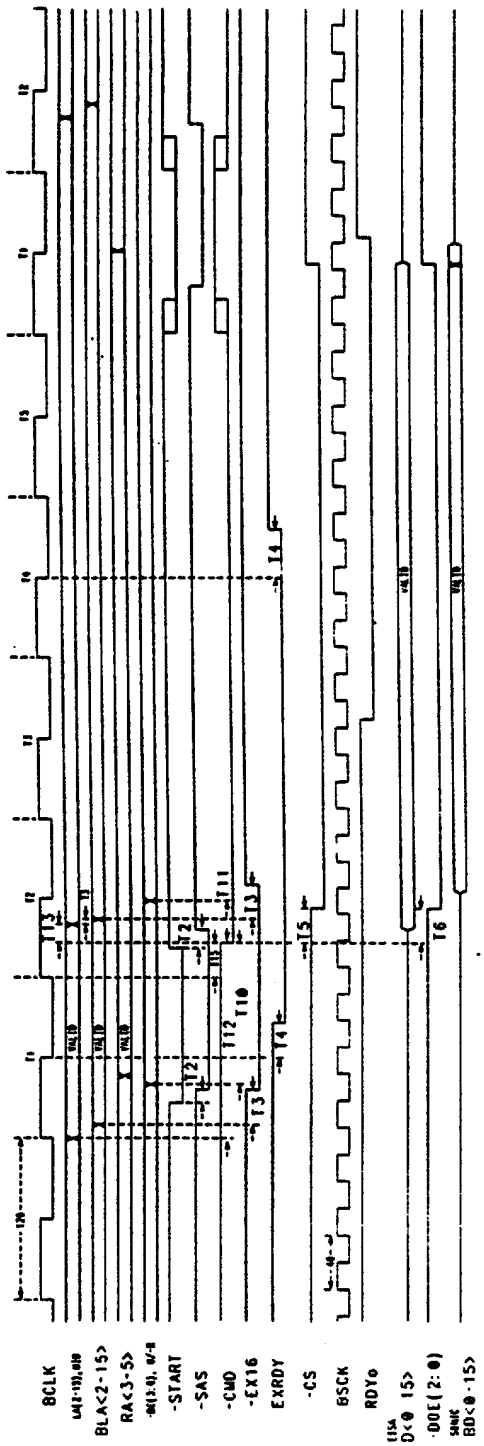
EISA 9010BV SLAVE WRITE TIMING



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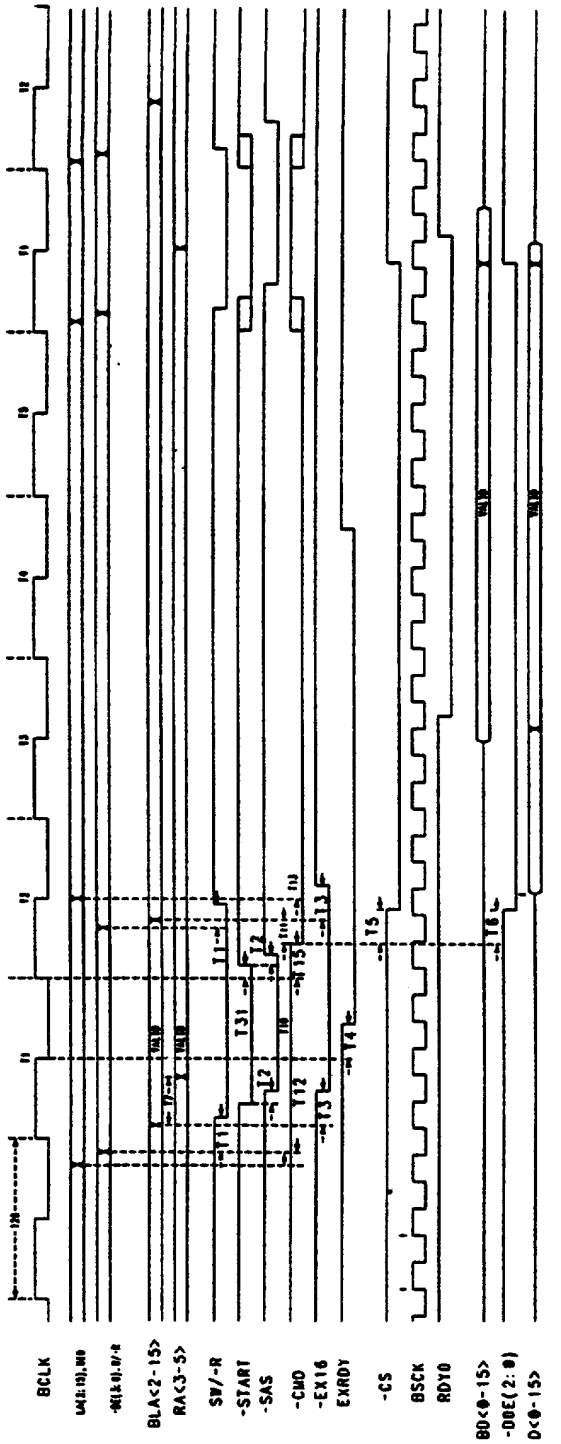
EISA 9010BV SLAVE READ TIMING



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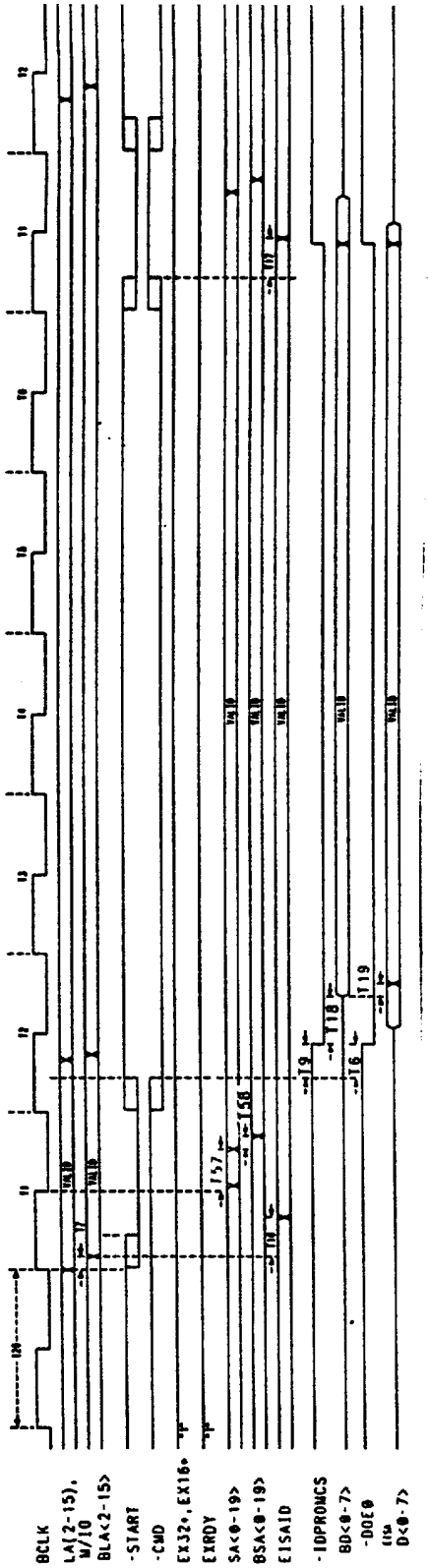
EISA 9010BV IDPROM READ TIMING



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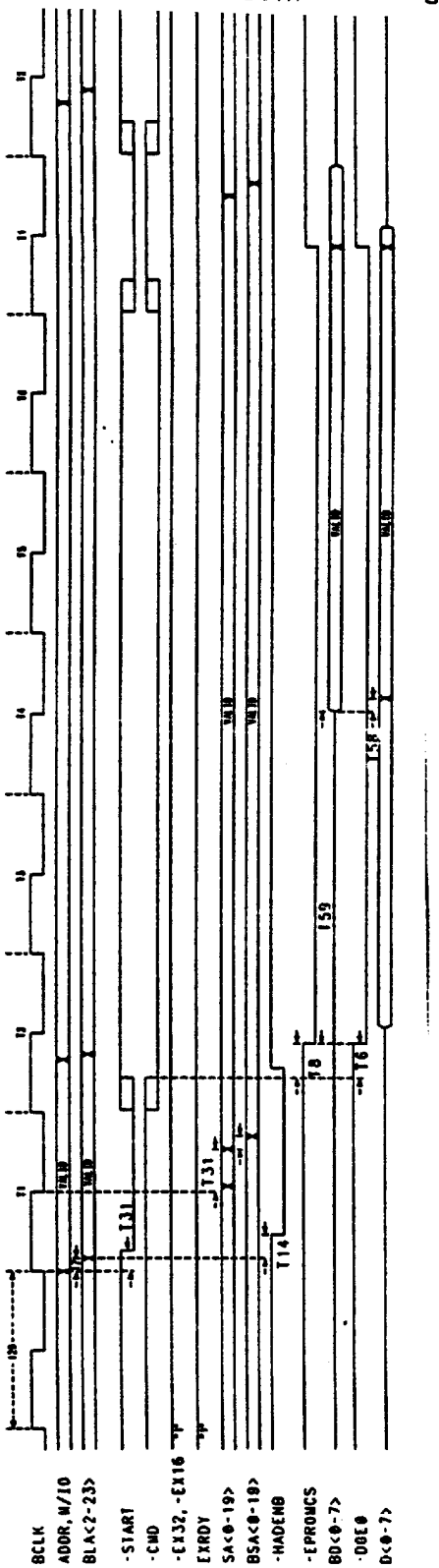
EISA 9010BV EPROM READ TIMING



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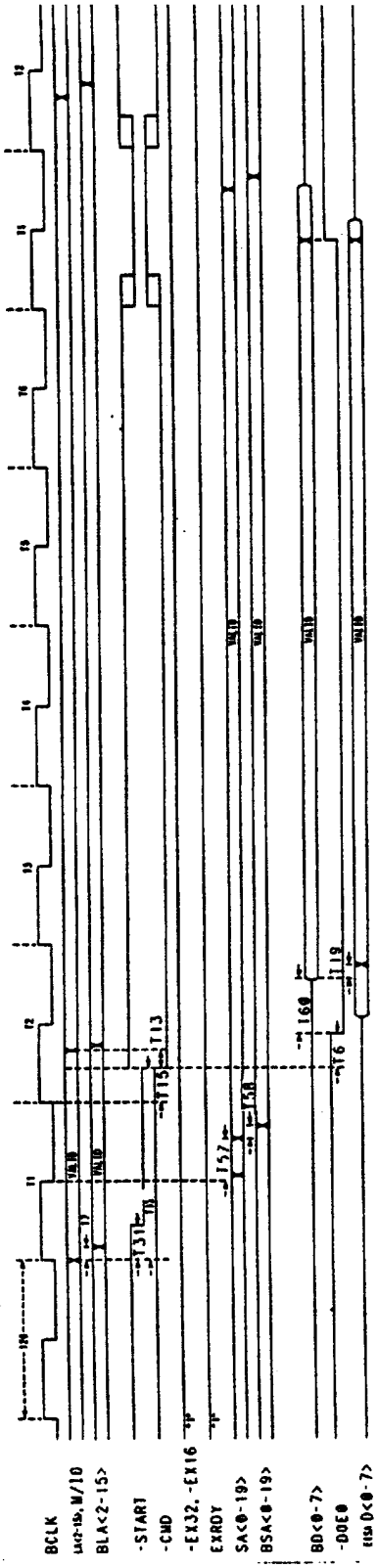
EISA 9010BV CONFIGURATION REGISTER READ TIMING



P L X TECHNOLOGY CORP 52E D 6855149 0000374 382 PLX

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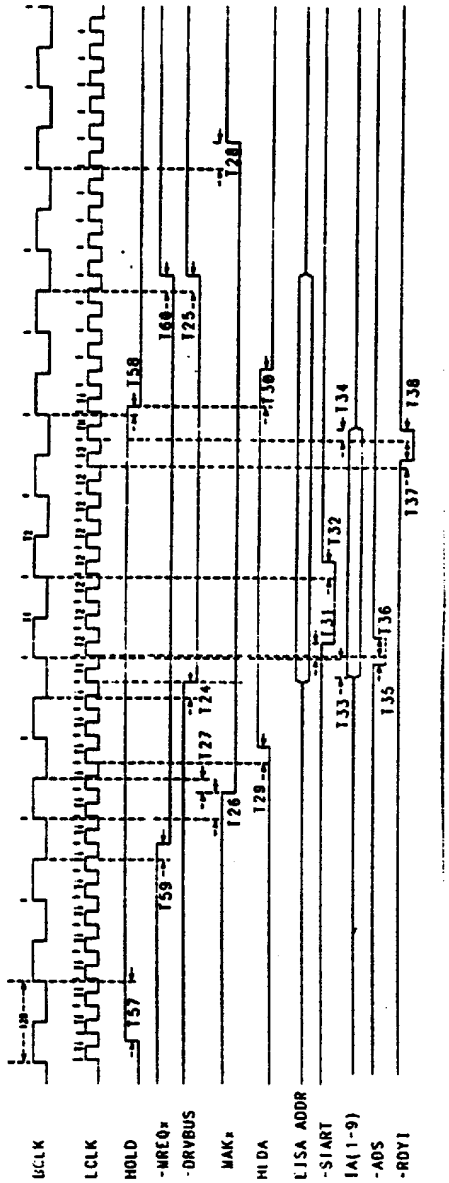
EISA 9010BV MASTER ARBITRATION



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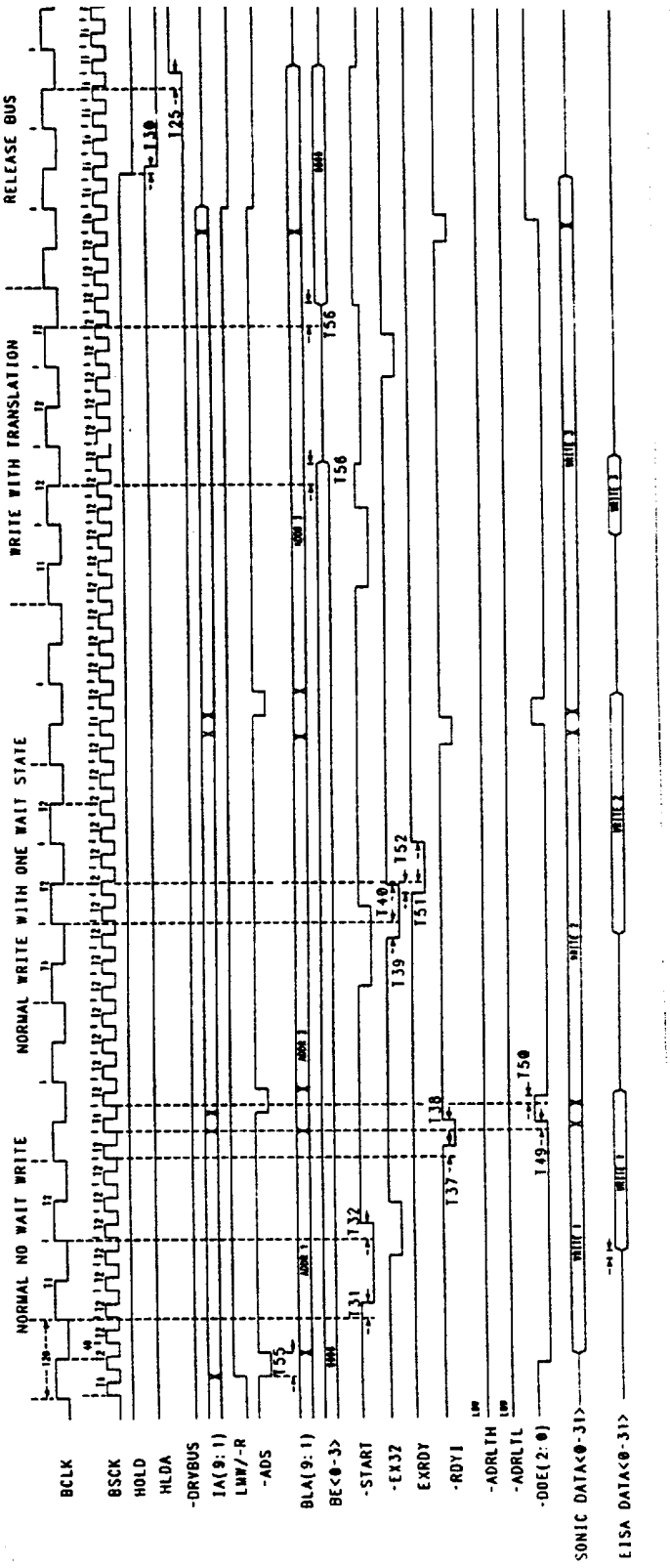
EISA 9010BV NON-BURST WRITE TIMING



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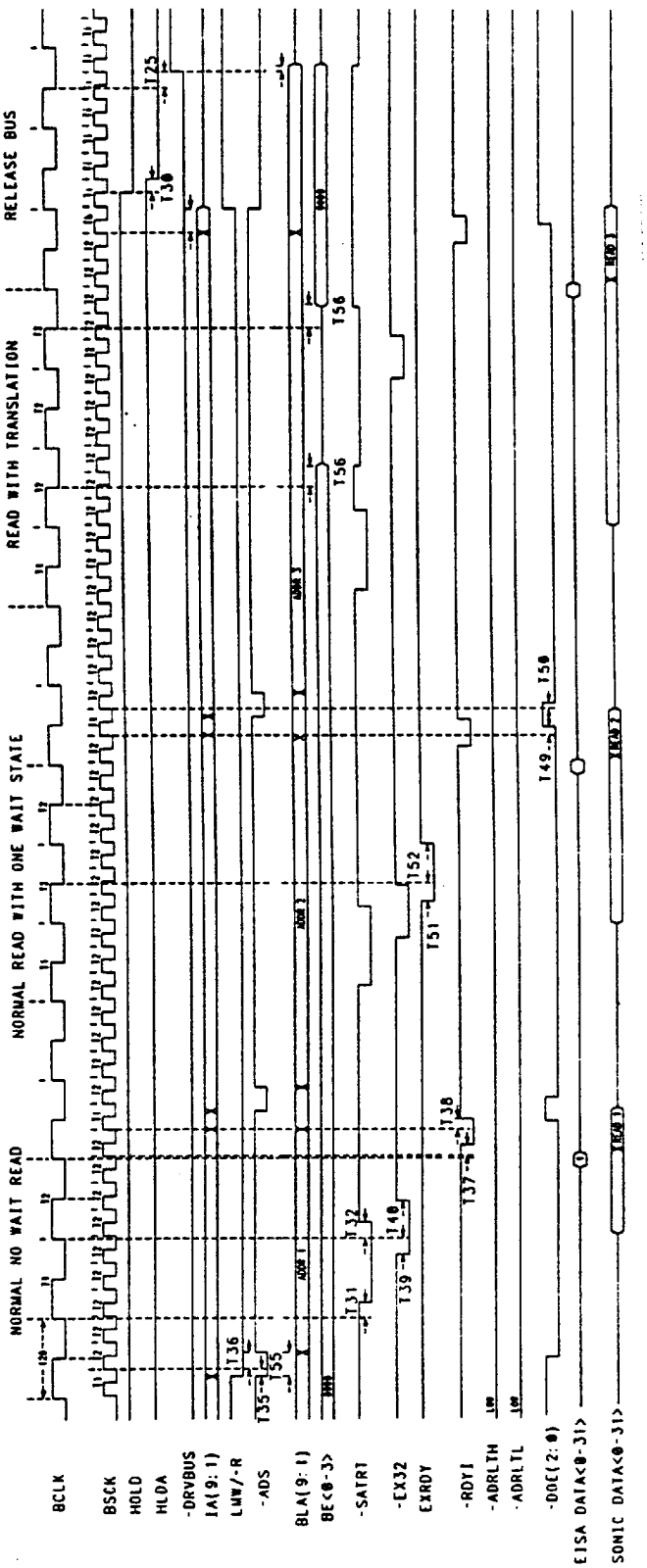
EISA 9010BV NON-BURST READ TIMING



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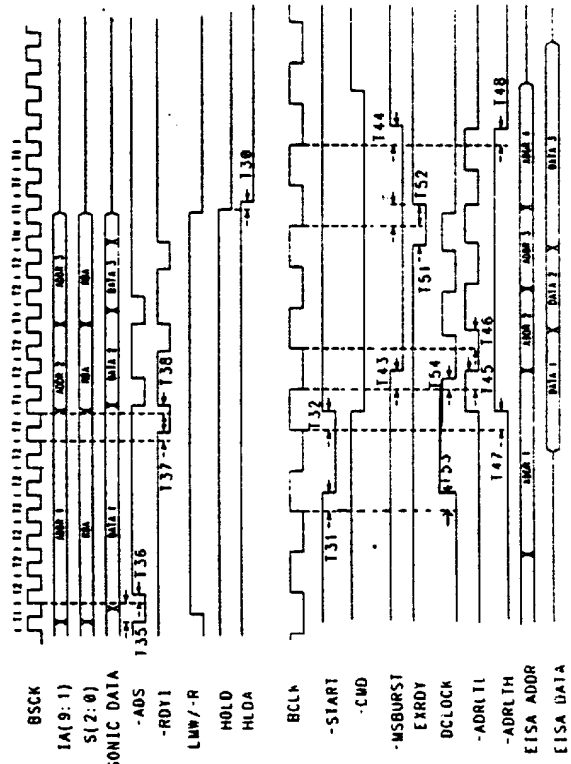
EISA 9010BV BURST W-W-W/WAIT



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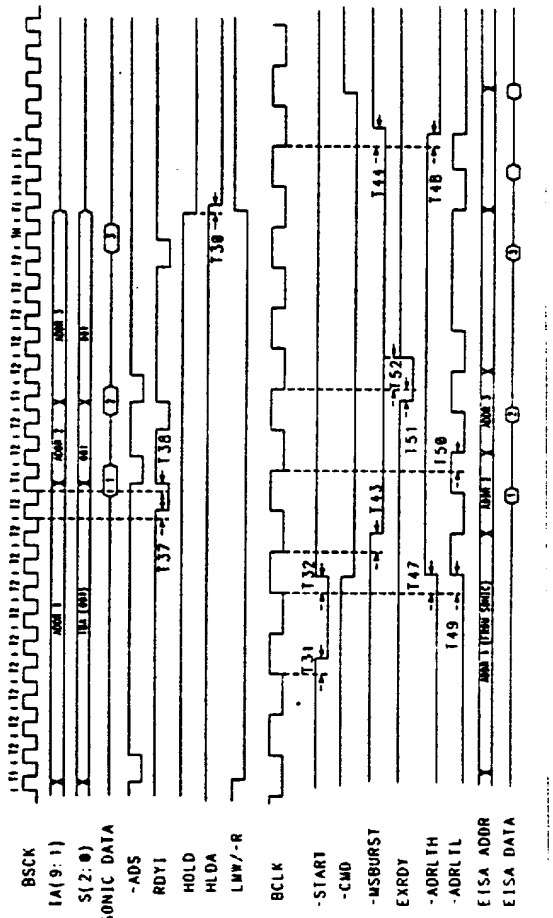
EISA 9010BV BURST R-R-R/WAIT



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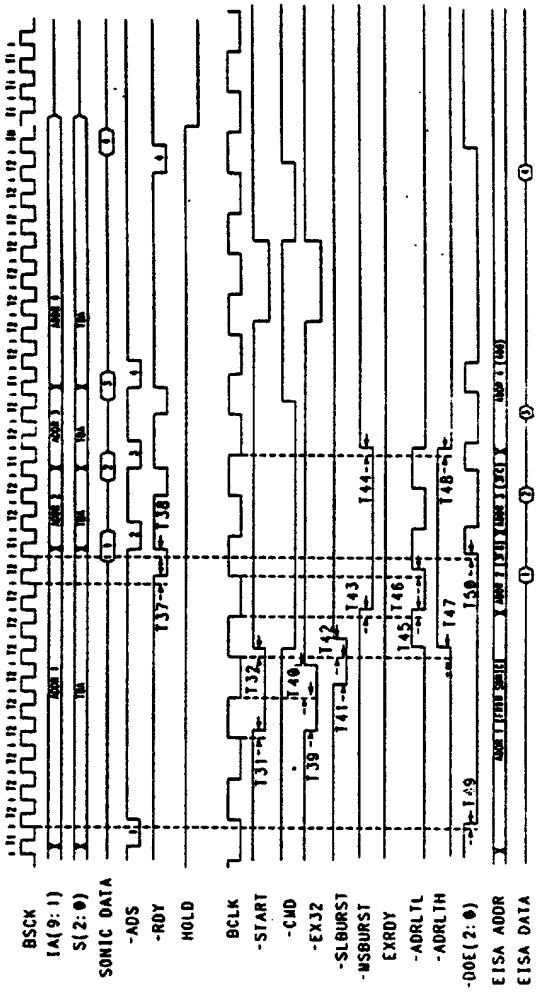
EISA 9010BV BURST R-R-R-R/PAGECROSS



P L X TECHNOLOGY CORP 52E D 6855149 0000380 686 PLX

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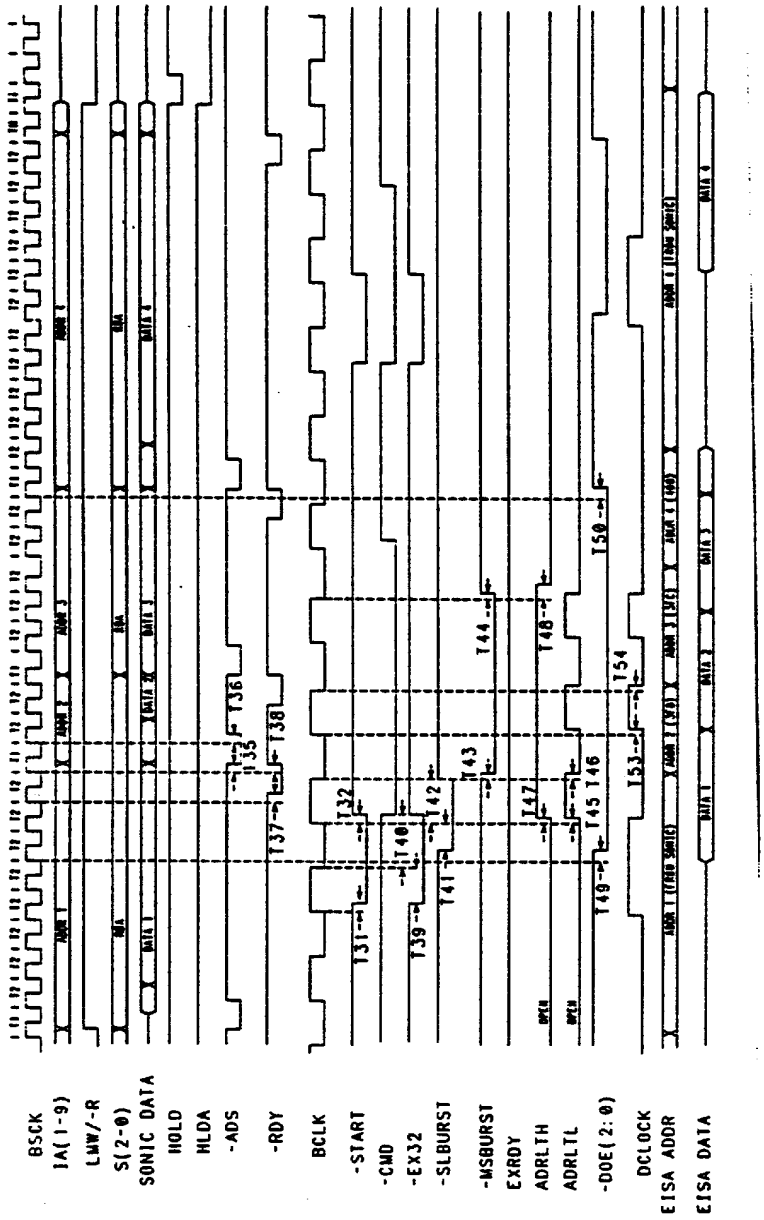
EISA 9010BV BURST W-W-W/PAGECROSS-W



EISA 9010BV TIMING

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Symbol	Description	Min	Max
T1	W/-R to SW/-R delay		25
T2	-START to -SAS delay		25
T3	BLA(2-15) to -EX16 delay		25
T4	BCLK falling to EXRDY delay		35
T5	-CMD to -CS delay		25
T6	-CMD to -DOE(2:0) delay		25
T7	BLA(2-15) to RA(3-5) valid delay		35
T8	-CMD to -EPROMCS delay		25
T9	-CMD to -IDPROMCS delay		25
T10	-BE(0:3) , W/-R setup to -CMD valid	80	
T11	-BE(0:3), W/-R hold from -CMD valid	25	
T12	LA(2-15), M/-IO setup to -CMD valid	120	
T13	LA(2-15), M/-IO hold from -CMD valid	25	
T14	BLA(2-23) to -HADENB valid delay		18
T15	BCLK rising to EISAID valid delay	2	25
T16	BLA(2-15) to EISAID valid delay		35
T17	BLA(2-15) to EISAID invalid delay		25
T18	-IDPROMCS to BD(0-7) valid delay		35
T19	BD(0-7) to EISA D(0-7) valid delay		10
T20	HOLD setup to BCLK rising	20	
T21	HOLD held to BCLK rising	10	
T22	BCLK falling to -MREQx valid		33
T23	BCLK falling to -MREQx invalid		33
T24	BCLK falling to -DRVBUS valid		25
T25	BCLK falling to-DRVBUS invalid		25
T26	BCLK rising to -MAKx valid		40
T27	-MAKx setup to BCLK falling	10	
T28	-MAKx held to BCLK falling	25	
T29	BSCK rising to HLDA valid		20
T30	HOLD falling to HLDA invalid		15
T31	BCLK rising to -START valid	2	25
T32	BCLK rising to -START invalid	2	25
T33	IA(9:1) setup to BCLK rising	15	
T34	IA(9:1) held to BCLK rising	10	
T35	-ADS setup to BSCK rising	10	
T36	-ADS held to BSCK rising	10	
T37	BSCK rising to -RDYi valid		15
T38	BSCK rising to -RDYi invalid		15
T39	-EX32 setup to BCLK falling	15	
T40	-EX32 held to BCLK falling	25	
T41	-SLBURST setup to BCLK rising	15	
T42	-SLBURST held to BCLK rising	25	
T43	BCLK falling to -MSBURST valid		25
T44	BCLK falling to -MSBURST invalid		25
T45	BCLK falling to -ADRLTL valid		20
T46	BCLK rising to -ADRLTL invalid		20
T47	BCLK rising to -ADRLTH invalid		20
T48	BCLK falling to -ADRLTH valid		20
T49	BSCK rising to -DOE(2:0) valid		20
T50	BSCK rising to -DOE(2:0) invalid		20
T51	EXRDY setup to BCLK falling	15	

T52	EXRDY held to BCLK falling	5	
T53	BCLK rising to DCLOCK valid		20
T54	BCLK rising to DCLOCK invalid		20
T55	IA(9:1) to BLA(9:1) delay		20
T56	-BE(3:0) to BCLK falling delay		30
T57	BCLK falling to SA(0-19) valid delay		30
T58	SA(0-19) to BSA (0-19) valid delay		10
T59	-EPROMCS to BD (0-7) valid delay		250
T60	-DOE0 to BD(0-7) valid delay		40

SECTION 6 - Electrical Specifications & Max Ratings

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Absolute Maximum Ratings

Storage Temperature	-65°C to +150°C
Ambient Temperature with Power Applied	-55°C to +125°C
Supply Voltage to Ground	-0.5V to +7.0V
Input Voltage (VIN)	VSS - 0.5V VDD + 0.5V
Output Voltage (VOUT)	VSS - 0.5V VDD + 0.5V

Operating Ranges

Ambient Temperature	Supply Voltage (VDD)	Input Voltage (VIN)
0°C to+70°C	5V +/- 5%	Min = VSS Max = VDD

Capacitance (sample tested only)

Parameter	Test Conditions	Pin Type	Typical Value	Units
CIN	VIN =2.0V f = 1 MHz	Input	5	pF
COUT	VOUT = 2.0V f = 1 MHz	Output	10	pF

Electrical Characteristics Tested Over Operating Range

Parameter	Description	Test Conditions		Min	Max	Units
VOH	Output High Voltage	VDD = Min, VIN=VIH or VIL	IOH = -4.0mA	2.4		V
VOL	Output Low Voltage		IOL per Tables 3.1-3.4		0.4	V
VIH	Input High Level			2.0		V
VIL	Input Low Level				0.8	V
ILI	Input Leakage Current	VSS <= VIN <=VDD VDD = Max		-10	+10	uA
IOZ	Tri-state Output Leakage Current	VDD= Max VSS <= VIN <=VDD		-10	+10	uA
ICC	Power Supply Current	VDD= Max (Typical = 40 mA)			80	mA

Section 7 - Package Mechanical Dimensions