EISA 9010

EISA Bus Master Interface Chip for National SONIC DP83932 LAN Controller

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Features

EISA bus master interface for National DP83932 Ethernet Controller

- Supports EISA Burst Mode Data rates to 33 MBytes/sec
- BIOS PROM and Node ID PROM support
- Clock to 25 MHz
- Direct connect to System Bus of all Host Interface Control Signals
- Low power CMOS in 128 Pin Plastic QFP Package

General Description

The EISA 9010 is designed to provide the most compact, inexpensive and highest performance EISA bus master interface for adapter boards that use the DP83932 LAN controller from National Semiconductor.

Use of the PLX Technology 9000 series of bus master chips minimizes hardware and software development costs and time because one basic adapter hardware and driver design can be used for EISA, AT or Micro Channel applications.

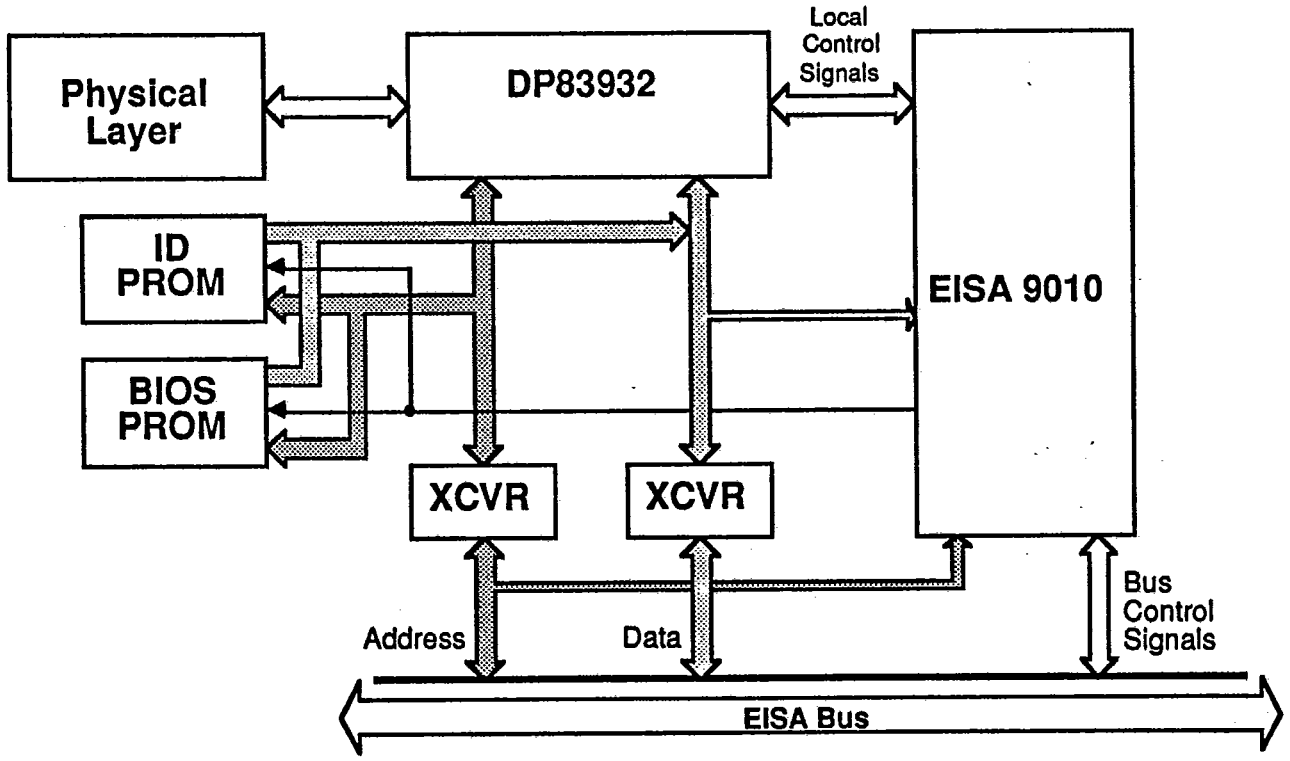

FIGURE 1. Typical Adapter Block Diagram

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EISA 9010 GENERAL DESCRIPTION

The EISA 9010 is designed to provide the most compact, inexpensive and highest performance EISA bus interface for the National SONIC DP83932.

EISA bus master adapters which use the DP83932 and the EISA 9010 offer substantial performance advantages over slave adapters. For example, a bus master can achieve up to eight times the system bus transfer rate of a typical sixteen bit AT slave implementation and at a competitive cost. LAN performance is also enhanced by the more efficient protocol processing of the intelligent controller. The bus master implementation frees the host processor from managing bus data transfer operations, which improves overall system performance.

Using the PLX Technology 9000 series of bus master chips also reduces total hardware and software development costs for LAN adapter manufacturers designing EISA, Micro Channel and AT compatible boards. In addition to the EISA 9010 interface chip, PLX technology provides the MC 9010 and AT 9010, which are Micro Channel and AT bus master chips respectively, that have local interfaces identical to the EISA 9010. Therefore, by using the 9000 series, similar hardware designs and software drivers can be used for all three buses, EISA, AT and Micro Channel.

Data Transfer Modes

The EISA 9010 supports both 16 and 32 bit Burst Data Transfers. In addition, the EISA 9010 supports slave mode for initialization of registers and access to other adapter board slave devices such as BIOS ROM, Node ID PROM or other memory and I/O devices.

Configuration Registers

The EISA 9010 contains five internal configuration registers and one Intelligent Peripheral Controller Port Selector Register. The configuration registers contain configuration data which is loaded from the host during I/O setup. Included in these registers are the interrupt request level, PREEMPT timer configuration, data size, I/O address decode bits, and PROM address decode bits. The EISA 9010 also provides four external user bits for application specific configuration information.

Specific EISA 9010 functions

EISA 9010 major functions include:

1. **Master Control Signal Protocol Converter.** The EISA 9010 converts all handshakes of the DP 83932 to EISA handshakes.
2. **Slave controller.** The EISA 9010 includes an EISA slave interface for control of adapter board slave devices.
3. **Address decoder.** The EISA 9010 decodes host address bits A16-A13, A11-A0 and contains an enable pin for an external A31-A17 or A24-A17 address decoder. The EISA 9010 decodes these addresses to generate chip selects.
4. **Interrupt generator.** The EISA 9010 can generate one of four host interrupts from one local interrupt, programmable through configuration registers.
5. **External Buffer Controller.** The EISA 9010 generates all buffer enable and direction signals for external address and data transceivers.
6. **Clock.** The EISA 9010 runs from an inexpensive crystal and generates a clock at25 MHz for external and internal use.
7. **User programmable configuration bits.** The EISA 9010 provides up to four external bits which can be configured through the configuration registers.
8. **Bus drivers.** All signals generated by the EISA 9010 drive the EISA bus directly, without requiring external drivers.
9. **Maximum bus hold time controller.** Through the configuration registers the user may program a maximum time which the adapter may hold the bus.
10. **Port selector register.** The EISA 9010 contains a register which latches Local Address 3-5 to provide port select information.
11. **Adapter ID mapping.** The adapter ID number is mapped into I/O space to allow the option to implement the adapter ID in an ID PROM.
12. **BURST Transfer Address Controller.** During EISA BURST transfers, the EISA 9020 generates A(2-9) to ensure proper timing between data and address signals.

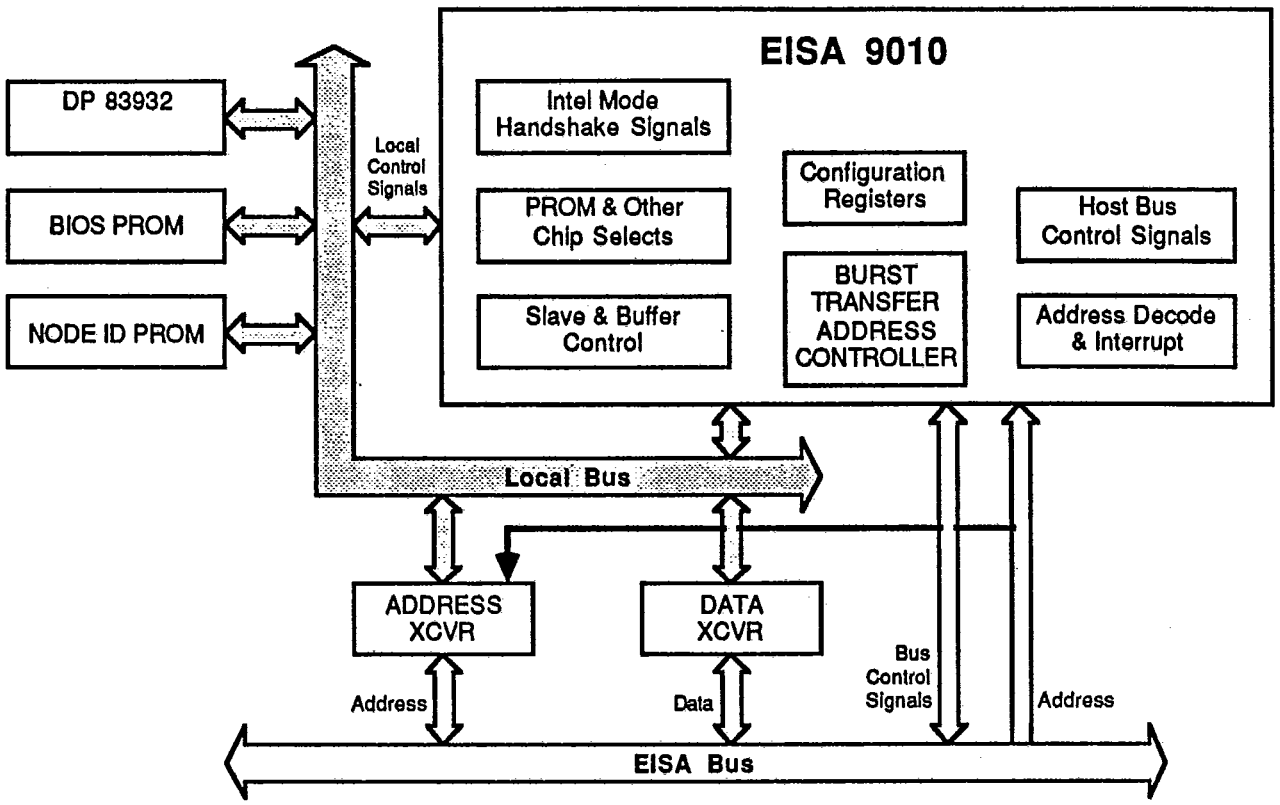

FIGURE 2. EISA 9010 Functional Block Diagram

Package Mechanical Dimensions