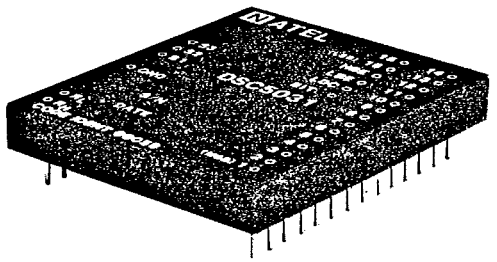
NATEL

DSC5031
DSC5032

Reference Powered, Low Profile (0.42")
1.3 Arc-minute Accuracy, 1.5 VA Output
16-bit Digital-to-Synchro Converter

Features

- ✓ **No DC Power Supplies Needed** (reference powered)
- ✓ **High Output Power in Small Package** (1.5 VA at 400 Hz)
- ✓ **1.3 Arc-Minute Accuracy**
- **Double-Buffered Digital Inputs**
- **Very Low Scale Factor Variation** (0.03% maximum)
- ✓ **Very Small Package Size** (3.1 X 2.6 X 0.42 inches)
- **Fully Protected Output** (current limiting) (short-circuit proof) (thermal cut-off)
- ✓ **Low Power Operation** (built-in dynamic supply)
- **Fully Isolated Operation** (inputs/outputs/reference)
- **Reference Input Protection**
- **Open Collector BIT Output**
- **TTL and CMOS Compatible**
- **Microprocessor Compatible** (8- and 16- bit)



Applications

Driving Control Transformers

Flight Instrumentation

Fire control systems

Servo Systems

Simulators

Positioning Control Systems

DSC5031
DSC5032

Description

Model 5031 is the first low-profile 16-bit Digital-to-Synchro converter that is reference powered; thereby eliminating the need for any external supplies. A single-point ground is all that is needed from the converter to the system's logic ground. The 1.5 VA output makes the 5031 an ideal choice when driving Control Transformers (CTs) or when testing Synchro-to-Digital (S-to-D) converters. In addition, the converter comes in the extremely small size of 3.1 X 2.6 X 0.42 inches. The converter is both 8- and 16- bit microprocessor compatible and includes a BIT output. The small size and excellent features have been made possible by the use of proven and reliable Natel hybrid microcircuits as an integral part of the 5031.

The reference-powered feature of the 5031 make it the converter of choice for use in systems that otherwise would need only a single 5-volt power supply. By using the 5031 in such systems, the overall system cost and complexity will be reduced substantially because ±15 volt power supplies will no longer be needed. In systems that still may need ±15 volt power, they will now have to supply less power. Other outstanding performance features include 1.3 arc-minute accuracy and 0.03% radius accuracy. In addition, the unique output stage of the 5031 uses a dynamic power supply to reduce the power dissipated in the output stage by a factor of two over conventional designs. The output stage is fully protected and includes fast-acting active current-limiting circuitry. A built-in-test circuit continuously monitors the output currents in all three output drivers along with other internal test points. An open collector logic output, referenced to the logic ground, immediately indicates if a fault condition is present.

The logic interface is easy, having the flexibility designed in to make interfacing possible with a minimum number of components. This includes the double-buffering of all input logic data bits. All data bits (1-16) are true binary coded and are actively pulled down to ground, so if the application requires less than 16-bits any unused bits may be left unconnected. Control bits LBE, HBE, and LDC control the operation of the data input buffers. All digital inputs are TTL and 5-V CMOS compatible, using internally derived logic thresholds that guarantee 0.8-V as a logic "0" and 2.4-V as a logic "1."

Theory of Operation

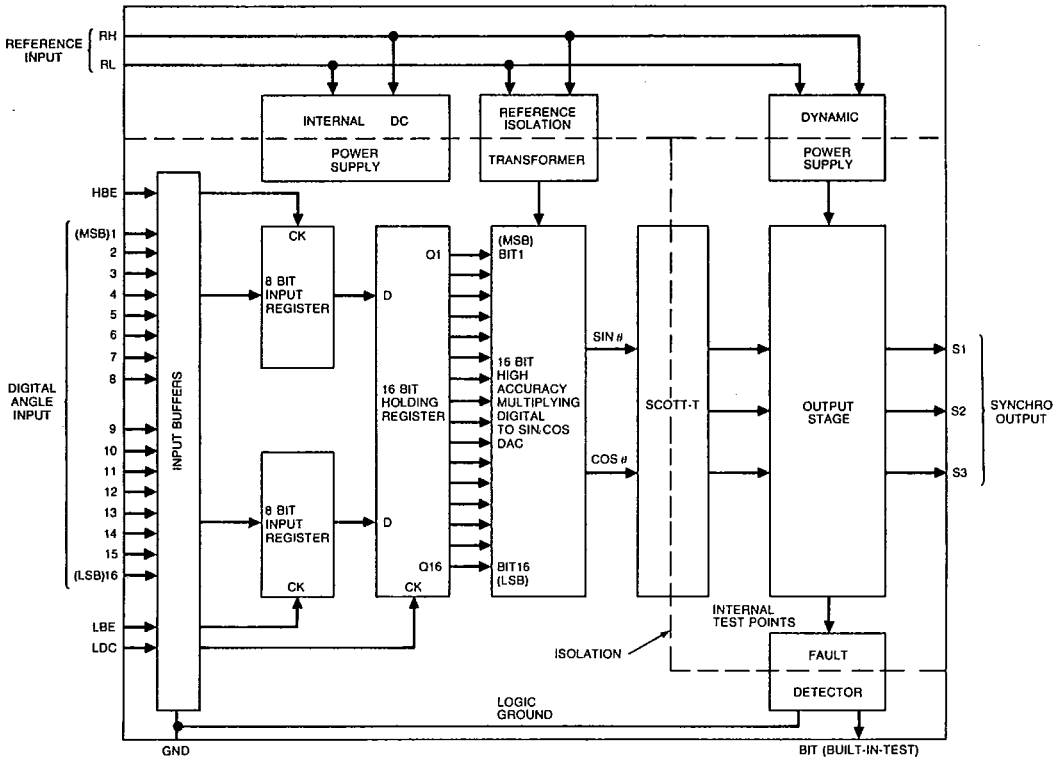


FIGURE 1 5031 Functional Block Diagram

The operation of Model 5031 is illustrated in the functional block diagram of Figure 1. The reference voltage (RH-RL) is received by both a power transformer and an isolation transformer. The power transformer has separate secondary windings. One set of windings provides bias and dynamic power supply voltages to the output stage; while another set provides power to the input circuitry, and is therefore referenced to the incoming "logic ground" line. The reference isolation transformer provides a scaled-down representation of the input reference to the multiplying digital-to-analog sine/cosine converter (DAC).

The digital word representing the input angle is applied to the input buffer registers, which are configured as two independently enabled bytes of 8 bits each. These bytes are controlled by the HBE (high byte enable) and LBE (low byte enable) input logic controls. When interfacing the 5031 to an 8-bit microprocessor, these registers are normally addressed sequentially over common data lines. When interfacing to a 16-bit data bus, both input registers are enabled simultaneously to accept a single 16-bit word. The second 16-bit "Holding Register" allows the upper and lower 8-bit bytes that are held in the input registers to be presented to the Sine/Cosine DAC simultaneously as a single 16-bit word. This holding register is controlled by the LDC (load converter) input. This double-buffering is especially important in 8-bit microcomputer-based systems where false codes and servo "hunting" would otherwise occur. The presence of these two registers in series allows the systems and circuit designers maximum flexibility in controlling the updating of the converter with digital data in systems with and without microprocessors. All three registers pass data from input to output whenever their respective enable signals are at logic "1," and latch data when the enable signals are at logic "0." The output of the holding register is applied to the digital input of the multiplying sine/cosine DAC. This DAC accepts the ac reference as a second input and multiplies the two together while following Sine and Cosine laws. The result are signals at the ac reference frequency and phase, which precisely reflect the sine and cosine of the input digital angle. The operation of the multiplying sine/cosine DAC is very similar to a pair of conventional four-quadrant multiplying DACs, with the exception that the transfer function is controlled by resistor ladders that follow sine and cosine laws instead of linear transfer functions. The format of these signals is changed from Sine/Cosine to Synchro format through an isolation scott-tee type transformer. The resultant 3 signals are then applied to the output stages.

The output stage consists of three precision power amplifiers in push-pull class AB configurations, powered from a dynamic power supply. This dynamic supply reduces the dissipation in the output section by allowing the output transistors to operate with less average voltage across them as compared to operation from a fixed dc power source. To assure stable operation over temperature and load variations, precision operational amplifiers are used as the primary amplifier gain elements. In addition to providing short circuit protection and current limiting, the power amplifiers are designed to shut down in a high impedance output state when the amplifier temperature reaches 125 degrees centigrade, thereby making them virtually indestructible.

The internal BIT circuit provides a fault indication if there is a loss of reference, output short circuit or overload, internal thermal shutdown, or internal circuit failure. The "open collector" logic output allows maximum flexibility in interfacing to system fault logic.

Specifications

PARAMETER	VALUE	REMARKS	TEST LEVEL
Digital Angular Resolution			
	16-bits (0.33 arc-minutes)		Note 2
Accuracy			
	± 4.0 arc-minutes (Option S) ± 2.0 arc-minutes (Option H) ± 1.3 arc-minutes (Option V)	Accuracy applies over the full operating temperature, frequency, power supply, and load ranges	Note 1
Reference/Power Input			
Voltage	115 V-rms, ±10% (option 9) 26 V-rms, ±10% (option 1)	For 90 V-rms output For 11.8 V-rms output	Note 2
Frequency	360 to 440 Hz		Note 3
Input Current 90 V-rms output (option 9)	17 mA-rms maximum 41 mA-rms maximum	V_{ref} = 115 V-rms, No Load V_{ref} = 115 V-rms, 1.5 VA load	Note 1
11.8 V-rms output (option 1)	77 mA-rms maximum 180 mA-rms maximum	V_{ref} = 26 V-rms, No Load V_{ref} = 26 V-rms, 1.5 VA load	Note 1
Breakdown Voltage	500 V-dc minimum	To logic ground or any output	Note 3
Harmonic Distortion	Up to 10 percent	Without degradation in accuracy	Note 3
Digital Inputs		Transient-protected CMOS	
Logic "0" level	-0.3 to 0.8 V-dc		Note 2
Logic "1" level	2.4 to 5.5 V-dc		Note 2
Input Current Data bits 1-16	15 μA typical (30 μA max.), active pull down to ground	Unused pins may be left unconnected	Note 3
Input Current HBE, LBE, LDC	-15 μA typical (-30 μA max.), active pull up to internal 5 V-dc	Unused pins may be left unconnected	Note 3
Data Bit Coding	Positive logic, natural binary angle	Bit 1 is MSB, Bit 16 is LSB	Note 3
Register Controls		Active-high transparent latches	
HBE	Logic "1" Logic "0"	Data bits 1-8 enter high-byte input register High-byte input register holds data	Note 1
LBE	Logic "1" Logic "0"	Data bits 9-16 enter low-byte input register Low-byte input register holds data	Note 1
LDC	Logic "1" Logic "0"	Data from input register enters holding register Holding register holds data	Note 1
Pulse Width HBE, LBE, and LDC	600 ns minimum	For guaranteed data transfer	Note 3
Data Set-up Time	200 ns minimum	Data stable before HBE or LBE low-to-high transition	Note 3
Data Hold Time	200 ns minimum	Data stable after HBE or LBE high-to-low transition	Note 3
BIT Output		Referenced to Digital Ground	
Output Current Sink Source (Leakage)	1 mA minimum @ 0.8 V-dc 10 nA typ. @ 25° C, (20 V-dc) 100 μA max. over temp.(20 V-dc)	Open collector output	Note 1
Logic "0"	-0.3 to +0.8 V-dc @ 1 mA load	For no fault detected	Note 1
Logic "1"	open collector, V max = 20 V-dc	Fault detected	Note 1

Specifications Continued

PARAMETER	VALUE	REMARKS	TEST LEVEL
Synchro Analog Outputs			
Voltages (Line-to-Line)	90 V-rms nominal (option 9) 11.8 V-rms nominal (option 1)	For nominal reference voltages.The outputs vary in direct proportion to the reference amplitude	
Gain	0.783 ±1% (option 9) 0.454 ±1% (option 1)	115 V-rms reference input/ 90 V-rms output 26 V-rms reference input/11.8 V-rms output	Note 1
Radius Accuracy	0.03% maximum	Scale factor variation with angle	Note 2
Drive Capability	1.5 VA minimum		Note 1
Output Current Drive	28 mA peak min. (option 9) 210 mA peak min. (option 1)	Between S1, S2, and S3 outputs	Note 3
Output Impedance (360 to 440 Hz)	less than 0.05 (2.5) ohms	For 11.8 (90) V-rms output Models	Note 3
Load Regulation	0.25% maximum	From no load to full load	Note 2
Synchro load impedance	$\|Z_{so}\| >$ 70 Ω (option 1) $\|Z_{so}\| >$ 4050 Ω (option 9)	1.5 VA limit	Note 1
Output Settling Time	250 μs maximum	To specified converter accuracy (179° step)	Note 2
Phase Shift	less than 1 degree	Reference input to synchro outputs	Note 3
Quadrature Output	0.15% maximum		Note 2
Output dc Offset (Line-to-Line)	± 10 mV typical, ±50 mV max. ± 1.5 mV typical, ± 8 mV max.	For 90 V-rms L-L Models (option 9) For 11.8 V-rms L-L Models (option 1)	Note 2
Thermal Cut-off	85° C case temperature min.		Note 1
Short Circuit Duration	Indefinite	All outputs together simultaneously	Note 3
Power Dissipation		Internal	
No Load 1.5 VA Load	2.0 watts maximum 3.2 watts maximum	For resistive loads. Does not include power dissipated in the load	Note 3
Thermal Resistance		Based on internal module dissipation	
Case to Ambient	10 degrees C per watt typical	Actual value depends upon cooling configuration	Note 3
Junction to Case	10 degrees C per watt max.	For the worst case device junction	Note 3
Physical Characteristics			
Size	3.12 X 2.62 X 0.42 inches (80 X 67 X 11 mm)		Note 3
Weight	6 oz. (170 g) maximum		Note 3

NOTE 1. Compliance of each component to this specification is 100% guaranteed by Natel. To assure compliance, this key parameter is 100% tested.

NOTE 2. Compliance of each component to this specification is 100% guaranteed by Natel. To assure compliance, AQL levels are verified using a lot sample level in the range of one to five percent.

NOTE 3. Compliance of each component to this specification is 100% guaranteed by Natel. To assure compliance, AQL levels are verified using a lot sample level of less than one percent. Note 3 parameters are maximum design limits.

If your application requires 100% testing of any additional parameters of this specification or requires non-standard input or output characteristics, please contact a Natel Applications Engineer or the Sales Department.

Absolute Maximum Ratings

Reference Input (option 9). . . . . 138 V-rms
Reference Input (option 1). . . . . 35 V-rms
Digital Inputs . . . . . - 0.3 to +6.5 V-dc
Storage Temperature . . . . . - 65° C to +135° C

Although the digital inputs have integral transient protection, this protection is not a substitute for proper electrostatic handling procedures. This part is ELECTROSTATIC SENSITIVE and must be treated as such.

Pin Designations

GND — Digital Ground - To be connected to the input logic ground. This is also the ground reference for the BIT output.

1-16 — Parallel Input Data Bits - 1 is MSB. Bit weight = 180 degrees. 16 is LSB. Bit weight = 0.0055 degrees.

For Model 5032, 14 is the LSB with a bit weight of 0.022 degrees. Pins 15 and 16 are not brought out on Model 5032.

RH, RL — Input Reference Voltage - RH stands for reference high. RL stands for reference low.

S1, S2, S3 — Analog Synchro Output Signals - These outputs are the synchro equivalent of the digital input angle. They are isolated from both the reference input and the logic input ground.

HBE* — High Byte Enable - Data bits 1-8 enter the input buffer register when HBE is set to a logic "1." When HBE is at logic "0," input data bits 1-8 are ignored.

LBE* — Low Byte Enable - Data bits 9-16 enter the input buffer register when LBE is set to a logic "1." When LBE is at logic "0," the input data bits are ignored.

LDC* — Load Converter - When LDC is set to logic "1," the contents of the two input buffer registers are transferred to the input holding register. When LDC is set to logic "0," data is held in the holding register.

BIT* — Built in Test - Open collector logic output signal referenced to the logic ground. Logic "0" = no fault condition present. Logic "1" (open circuit) = fault condition.

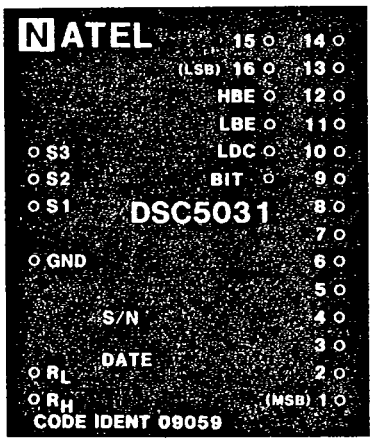


FIGURE 2 DSC5031 Pin Assignments

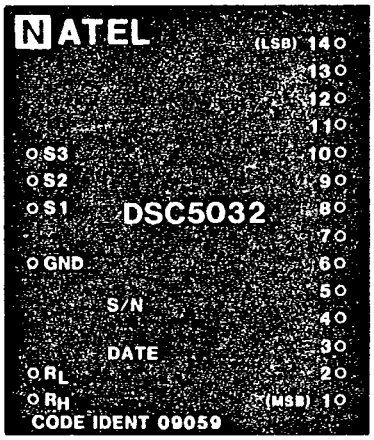
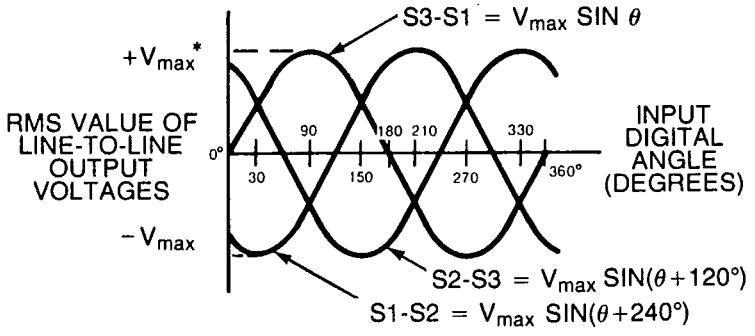


FIGURE 3 DSC5032 Pin Assignments

*NOTE These pins are not brought out for the Model 5032

Analog Output Signals

The Synchro output signals S1, S2, and S3 are all in phase (± 180°) with the incoming reference signal and have amplitudes which vary in direct proportion to the reference. The transfer function of this scaling is dependent upon the reference input voltage option (115 V-rms or 26 V-rms) and upon the input digital angle. Since the 5031 has Synchro-format outputs which drive the load in essentially a three-wire "delta" configuration, the output voltages are specified as "line-to-line." See figure 4. The output amplitudes of interest are the differential amplitudes between the S1, S2, and S3 outputs when taken in pairs (S3-S1, S1-S2, S2-S3). For option 9 of the 5031, where the reference input is 115 V-rms, the maximum line-to-line output voltage is 90 V-rms. This would occur, for example, between the S1 and S3 outputs when the digital input angle is 90°. For option 1 of the 5031, where the reference input is 26 V-rms, the corresponding maximum line-to-line output voltage is 11.8 V-rms.
In Figure 4, $V_{max} = V_{reference} \times$ Converter Gain.



*In phase with RH-RL

FIGURE 4 Output Voltage Phasing

Digital Interface

The double-buffered input registers of the DSC5031 offer the user an easily implemented interface with 8- or 16-bit microprocessor data buses. For applications not involving a microprocessor, independently controlled 8-bit latching registers give the user the flexibility of designing a customized interface system. Provision has also been made for asynchronous data inputs through the use of the LDC control function. Asynchronous data inputs up to 16 bits can be accommodated.

Continuous Operation

Asynchronous converter operation, without timing controls, is shown in figure 5. Digital control signals LBE, HBE, and LDC have internal pull-up circuitry, permitting these pins to be left open. The parallel information at the data inputs 1-16 is continuously converted to 3-wire Synchro format at the analog outputs. For applications requiring less than 16-bit resolution unused pins can be left open. Internal pull-down circuitry applies a logic "0" to unconnected data inputs.

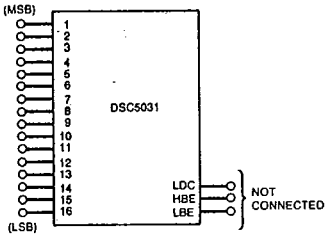


FIGURE 5 Digital Connection for Continuous Operation

Two-Byte Loading

The circuit configuration for two-byte loading of angular data from a data bus is shown in figure 6. As shown in the the timing diagram of figure 7, the 8 LSBs (9-16) are transferred to the low-byte input register when LBE is at logic "1." LBE can be at logic "1" when data bits are changing, but must remain at logic "1" for a minimum of 600 ns after the data is stable. Data should be held for 200 ns (data hold time) after LBE goes to logic "0." Bits 1-8 are transferred to the high-byte input register when HBE is at logic "1." The timing requirements are the same as those for LBE. Data is transferred from the two input registers to the holding register when LDC (load converter) is at a logic "1." If LDC is at logic "0," the contents of the holding register are latched and remain at their previous values unaffected by changes at the data inputs or input registers. Please note that LBE, HBE, and LDC are level-actuated functions.

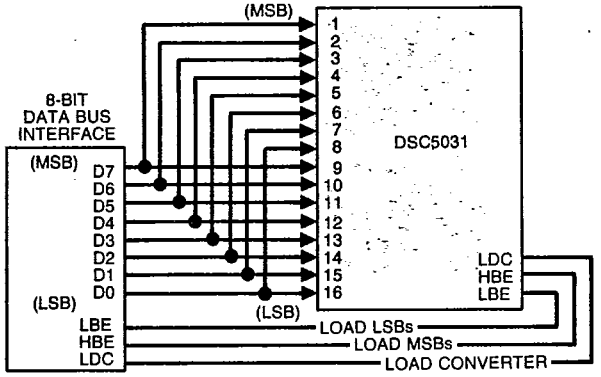


FIGURE 6 Digital Connections for Two-Byte Loading

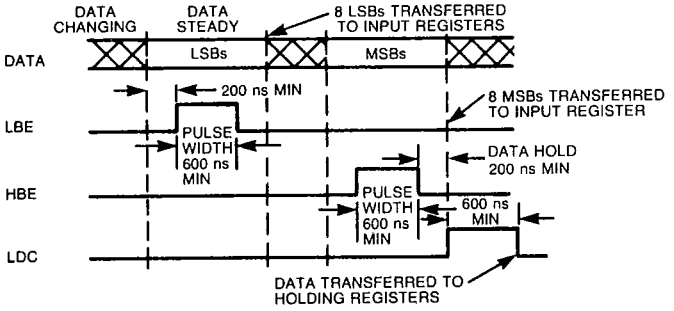


FIGURE 7 Timing For Two-Byte Loading

Edge-Triggered (Master-Slave) Loading

For single-byte loading, the 5031 can be configured to operate with edge-triggered loading by using a single external inverter gate. This is shown in figure 8. In this configuration, the input buffer registers are acting as the "master" registers ; and the holding register is acting as the "slave" register. When the clock signal is at logic "0" data is accepted into the "master" register and data is held in the "slave" register. At the low-to-high transition of the clock, the data is transferred from the master to the slave. The timing diagram for this method of operation is shown in figure 9. For proper operation, the LDC transition should always occur before the HBE/LBE transition.

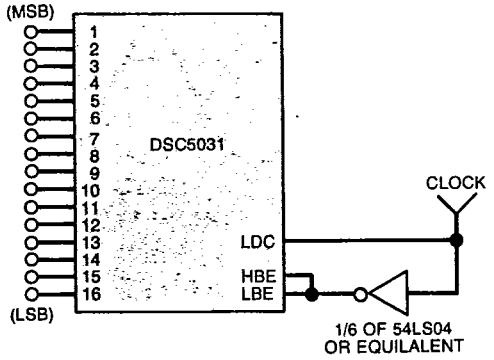


FIGURE 8 Digital Connections for Edge-Triggered Loading

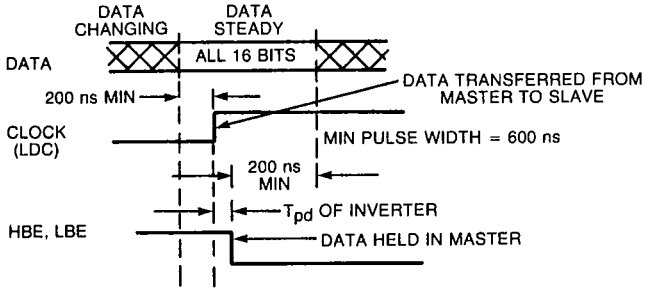


FIGURE 9 Timing for Edge-Triggered Loading

BIT Output

Another outstanding feature of the 5031 is the BIT output signal. This logic signal is continuous, and therefore it can be relied upon to be either at logic "0" or logic "1" with no awkward "pulse output" states to try to interpret. If everything is OK, the signal is at a logic "0" continuously. If a fault is detected, the BIT output will go to a logic "1" open collector output state. The open collector output is capable of holding off 20 volts in the high state, which simplifies the interfacing of this signal. The fact that a "no fault" condition results in a logic "0" output is significant because it eliminates the fault detection ambiguity that would otherwise exist if power were lost to the converter. The conditions that give rise to a logic "1" on the BIT output are as follows:

1. Loss of reference power.
2. Output short circuit or overload.
3. Internal thermal shutdown.
4. Internal circuit failure resulting in output imbalance or overload.

Driving Synchro-to-Digital Converters

A useful application of the 5031 is in testing Synchro-to-Digital Converters. This application can be for both laboratory test equipment and for real-time BIT and fault isolation testing of systems and PC boards, which have one or more S-to-D converters. The 5031 is ideally suited for these applications due to the following features:

1. The high accuracy (1.3 arc-minutes) of the 5031 allows for precision testing.
2. The 90 V-rms output version can easily test 90-V converters without using external transformers.
3. Multiple S-to-D loads can be driven from a single 5031. With only a 0.42 inch height, it can easily fit on low-profile logic boards.

Driving Control Transformers

Control Transformers (CTs) are electromechanical Synchro devices that provide a null voltage output from the rotor windings whenever the actual shaft angle of the CT matches the angle sent to the CT from the S1, S2, and S3 outputs of the 5031. The actual transfer function of a CT is as follows:

$$V_{rotor}(rms) = K \times V_{L\text{-}L} \times \sin(\theta - \phi)$$

where:

K = Gain of the CT
$V_{L\text{-}L}$ = L-L voltage from 5031
θ = the angle represented by the 5031 output
ϕ = the CT shaft angle

In systems that utilize CTs, they are used as position sensing elements rather than as torque or motor elements. The force that is used to position the shaft generally is provided by a motor coupled to the common shaft. CT impedances, therefore are relatively high. Table 1 shows typical impedances for various sizes of CTs. It is clear from table 1 that the Natel DSC5031 is capable of easily driving common CTs. Of course, the VA rating of the load should always be verified to be sure that the 5031 has sufficient drive capacity.

TABLE 1. Typical Control Transformer Parameters

CT Size	Frequency	Voltage	Z_{so}	$\lvert Z_{so} \rvert$	Required VA
08	400	11.8 V-rms	64+j332	338	0.31
11	400	11.8 V-rms	20+j128	129	0.81
18	400	90 V-rms	1360+j12600	12700	0.48

Output Protection

The Model 5031 incorporates several protection methods including:

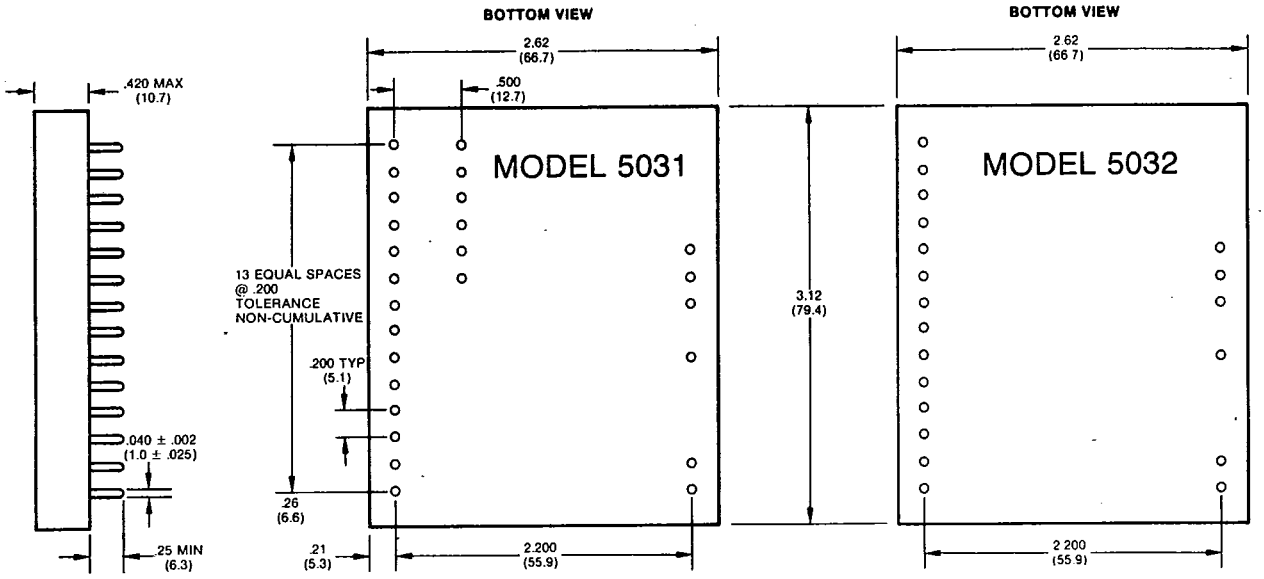
1. Active current limiting
2. Thermal cut-off
3. Overvoltage transient protection

The active current-limiting circuitry in the 5031 continuously monitors the instantaneous current in each of the three output driver stages and compares this current to a preset level. When an overcurrent or output short circuit condition exists, the peak current that can be supplied to the load is instantly limited to a value that is safe for the components used within the 5031.

The thermal cut-off circuit of the 5031 uses a solid-state temperature sensing element mounted on a common surface with all of the components of the three power amplifiers. A high-gain amplifier senses the voltage from this temperature sensor and provides an indication when the power amplifier's temperature reaches 125 degrees centigrade. If this occurs, a disable signal is applied to each of the output power amplifiers, which removes all output current drive capability. The result is that the outputs go into a high-impedance state and are no longer capable of driving load current, even into a dead-short circuit. When the internal temperature drops to a safe level, the output stages are automatically restored to their normal state.

The 5031 incorporates overvoltage transient protection on the reference input . This transient protection utilizes a rugged transient suppression diode that automatically conducts to suppress transient energy whenever the applied voltage reaches a dangerous level. The reference-protection diode is connected internally across RH-RL and may begin to conduct if the reference input (RH-RL) reaches 190 volts peak (42 volts peak for option 1).

For added protection, it is recommended that external output-protection diodes be connected in a "delta" configuration, with one diode between each of the S1-S2, S2-S3, and S1-S3 output pairs. This extra external protection is necessary at the output of the 5031 due to the fact that synchros are by nature inductive loads and can produce voltage transients many times their nominal voltage due to inductive "kick." For the 90 V-rms model (option 9), these diodes can be part number 1N6072. For the 11.8 V-rms model (option 1), the diodes can be part number 1N6048.



NOTES:
1. DIMENSIONS SHOWN IN INCHES AND (mm)
2. PINS ARE GOLD PLATED (50μINCH MIN)
3. CASE MATERIAL IS GLASS FILLED DIALLYL PHTHALATE.

TOLERANCES:
.XX = ±.020 (±.51)
.XXX = ±.010 (±.25)

MECHANICAL OUTLINE

Ordering Information

DSC5031 - T R A M

Temperature Range

1 = 0° C to +70° C
2 = -55° C to +85° C

Reference/Output Voltage

1 = 26 V-rms reference/ 11.8 V-rms output
9 = 115 V-rms reference/ 90 V-rms output

Accuracy

S = ± 4 arc-minutes
H = ± 2 arc-minutes
V = ± 1.3 arc-minutes

Mil Specification

S = Standard
B = MIL-STD-883, rev. B

SPECIFY DSC5032 FOR 14-BIT INDUSTRY STANDARD PIN-OUT

Other products available from NATEL

- Hybrid (36-pin DDIP size) Synchro (Resolver)-to-Digital converters with 10- to 16-bit resolutions (1000 series)
- Second generation Four Quadrant Multiplying Sin/Cos DAC (HDSC2026)
- Low cost Digital-to-Sin/Cos converter in a ceramic package (HDSC2306)
- 2-channel Digital-to-Sin/Cos converter in a single 36-pin hybrid (HDSC2036)
- 2 VA output, Digital to Resolver Converter in a 32-pin package (HDR2116)
- Resolver Control Differential Transmitter in a single 36-pin package (HCDX3106)
- 22-bit Binary-to-BCD and BCD-to-Binary converters (SBD227 and SDB724)

A wide range of applications assistance is available from Natel. Application notes can be requested when available... and Natel's applications engineers are at your disposal for solving specific problems.

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