CYPRESS SEMICONDUCTOR

ADVANCED INFORMATION

CY7C1331
CY7C1332

64K x 18 Synchronous Cache 3.3V RAM

Features

- **Supports 50-MHz Pentium™ processor cache systems with zero wait states**
- **64K by 18 common I/O**
- **Fast clock-to-output times**
  - **— 12.5 ns with 0-pF load**
  - **— 14 ns with 85-pF load**
- **Two-bit wraparound counter supporting the Pentium and 486 burst sequence (7C1331)**
- **Two-bit wraparound counter supporting linear burst sequence (7C1332)**
- **Separate processor and controller address strobes**
- **Synchronous self-timed write**
- **Direct interface with the processor and external cache controller**
- **Asynchronous output enable**
- **JEDEC-standard pinout**
- **52-pin PLCC and PQFP packaging**

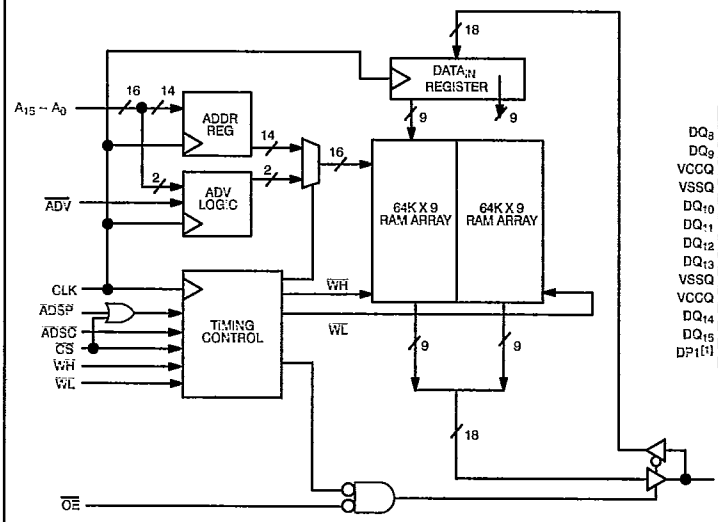
Functional Description

The CY7C1331 and CY7C1332 are 3.3V 64K by 18 synchronous cache RAMs designed to interface with high-speed microprocessors with minimum glue logic. Maximum access delay from clock rise is 12.5 ns. A 2-bit on-chip counter captures the first address in a burst and increments the address automatically for the rest of the burst access.

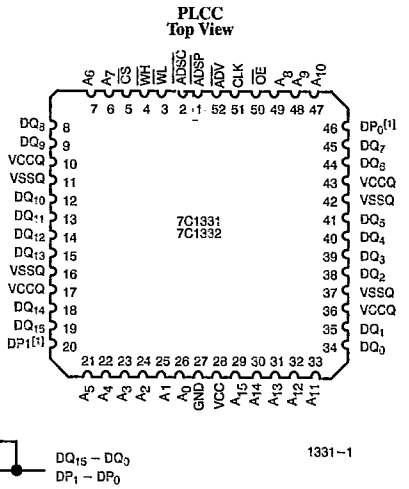
The CY7C1331 is designed for Intel Pentium and i486 CPU–based systems; its counter follows the burst sequence of the Pentium and the i486 processors. The CY7C1332 is architected for processors with linear burst sequences. Burst accesses can be initiated with the processor address strobe ($\overline{ADSP}$) or the cache controller address strobe ($\overline{ADSC}$) inputs. Address advancement is controlled by the address advancement ($\overline{ADV}$) input.

A synchronous self-timed write mechanism is provided to simplify the write interface. A synchronous chip select input and an asynchronous output enable input provide easy control for bank selection and output three-state control.

Logic Block Diagram



Pin Configuration



Selection Guide

		7C1331–12 7C1332–12	7C1331–16 7C1332–16	7C1331–19 7C1332–19
Maximum Access Time (ns) (0-pF load)		12.5	16.5	19.5
Maximum Operating Current (mA)	Commercial	180	160	150
	Military			170

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Note:
1. DP_0 and DP_1 are functionally equivalent to DQ_X.

Functional Description (continued)

Single Write Accesses Initiated by $\overline{ADSP}$

This access is initiated when the following conditions are satisfied at clock rise: (1) $\overline{CS}$ is LOW and (2) $\overline{ADSP}$ is LOW. $\overline{ADSP}$-triggered write cycles are completed in two clock periods. The address at A_0 through A_{15} is loaded into the address register and address advancement logic and delivered to the RAM core. The write signal is ignored in this cycle because the cache tag or other external logic uses this clock period to perform address comparisons or protection checks. If the write is allowed to proceed, the write input to the CY7C1331 and CY7C1332 will be pulled LOW before the next clock rise. $\overline{ADSP}$ is ignored if $\overline{CS}$ is HIGH.

If $\overline{WH}$, $\overline{WL}$, or both are LOW at the next clock rise, information presented at $DQ_0 - DQ_{15}$ and $DP_0 - DP_1$ will be written into the location specified by the address advancement logic. $\overline{WL}$ controls the writing of $DQ_0 - DQ_7$ and DP_0 while $\overline{WH}$ controls the writing of $DQ_8 - DQ_{15}$ and DP_1. Because the CY7C1331 and CY7C1332 are common-I/O devices, the output enable signal ($\overline{OE}$) must be deasserted before data from the CPU is delivered to $DQ_0 - DQ_{15}$ and $DP_0 - DP_1$. As a safety precaution, the appropriate data lines are three-stated in the cycle where $\overline{WH}$, $\overline{WL}$, or both are sampled LOW, regardless of the state of the $\overline{OE}$ input.

Single Write Accesses Initiated by $\overline{ADSC}$

This write access is initiated when the following conditions are satisfied at rising edge of the clock: (1) $\overline{CS}$ is LOW, (2) $\overline{ADSC}$ is LOW, and (3) $\overline{WH}$ or $\overline{WL}$ are LOW. $\overline{ADSC}$ triggered accesses are completed in a single clock cycle.

The address at A_0 through A_{15} is loaded into the address register and address advancement logic and delivered to the RAM core. Information presented at $DQ_0 - DQ_{15}$ and $DP_0 - DP_1$ will be written into the location specified by the address advancement logic. $\overline{WL}$ controls the writing of $DQ_0 - DQ_7$ and DP_0 while $\overline{WH}$ controls the writing of $DQ_8 - DQ_{15}$ and DP_1. Since the CY7C1331 and the CY7C1332 are common-I/O devices, the output enable signal ($\overline{OE}$) must be deasserted before data from the cache controller is delivered to the data lines. As a safety precaution, the appropriate data lines are three-stated in the cycle where $\overline{WH}$, $\overline{WL}$, or both are sampled LOW, regardless of the state of the $\overline{OE}$ input.

Single Read Accesses

A single read access is initiated when the following conditions are satisfied at clock rise: (1) $\overline{CS}$ is LOW, (2) $\overline{ADSP}$ or $\overline{ADSC}$ is LOW, and (3) $\overline{WH}$ and $\overline{WL}$ are HIGH. The address at A_0 through A_{15} is stored into the address advancement logic and delivered to the RAM core. If the output enable ($\overline{OE}$) signal is asserted (LOW), data will be available at the data outputs a maximum of 12.5 ns after clock rise.

Burst Sequences

The CY7C1331 provides a 2-bit wraparound counter, fed by pins $A_0 - A_1$, that implements the Intel 80486 and Pentium processor address burst sequence (see *Table 1*). Note that the burst sequence depends on the first burst address.

Table 1. Counter Implementation for the Intel Pentium/80486 Processor's Sequence

First Address	Second Address	Third Address	Fourth Address
$A_X + 1, A_X$	$A_X + 1, A_X$	$A_X + 1, A_X$	$A_X + 1, A_X$
00	01	10	11
01	00	11	10
10	11	00	01
11	10	01	00

The CY7C1332 provides a two-bit wraparound counter, fed by pins $A_0 - A_1$, that implements a linear address burst sequence (see *Table 2*).

Table 2. Counter Implementation for a Linear Sequence

First Address	Second Address	Third Address	Fourth Address
$A_X + 1, A_X$	$A_X + 1, A_X$	$A_X + 1, A_X$	$A_X + 1, A_X$
00	01	10	11
01	10	11	00
10	11	00	01
11	00	01	10

Application Example

Figure1 shows a 512-Kbyte secondary cache for a hypothetical 3.3V, 50-MHz Pentium or i486 processor using four CY7C1331 cache RAMs.

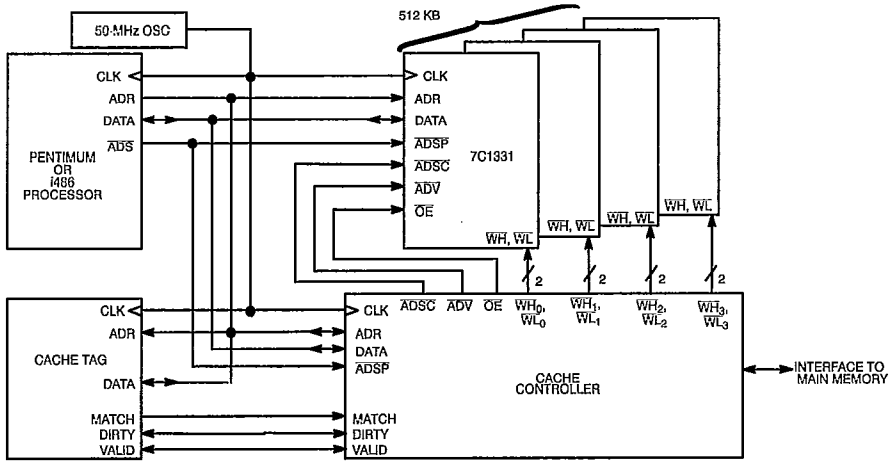

Figure 1. Cache Using Four CY7C1331s

Pin Definitions

Signal Name	Type	# of Pins	Description
VCC	Input	1	+3.3V Power
VCCQ	Input	4	+3.3V (Outputs)
GND	Input	1	Ground
VSSQ	Input	4	Ground (Outputs)
CLK	Input	1	Clock
$A_{15} - A_0$	Input	16	Address
$\overline{ADSP}$	Input	1	Address Strobe from Processor
$\overline{ADSC}$	Input	1	Address Strobe from Cache Controller
$\overline{WH}$	Input	1	Write Enable – High Byte
$\overline{WL}$	Input	1	Write Enable – Low Byte
$\overline{ADV}$	Input	1	Advance
$\overline{OE}$	Input	1	Output Enable
$\overline{CS}$	Input	1	Chip Select
$DQ_{15}-DQ_0$	Input/Output	16	Regular Data
DP_1-DP_0	Input/Output	2	Parity Data

Pin Descriptions

Signal Name	I/O	Description
Input Signals		
CLK	I	Clock signal. It is used to capture the address, the data to be written, and the following control signals: $\overline{ADSP}$, $\overline{ADSC}$, $\overline{WH}$, $\overline{WL}$, $\overline{CS}$, and $\overline{ADV}$. It is also used to advance the on-chip auto-address-increment logic (when the appropriate control signals have been set).
A15 -A0	I	Sixteen address lines used to select one of 64K locations. They are captured in an on-chip register on the rising edge of CLK if $\overline{ADSP}$ or $\overline{ADSC}$ is LOW. The rising edge of the clock also loads the lower two address lines, $A_1 - A_0$, into the on-chip auto-address-increment logic if $\overline{ADSP}$ or $\overline{ADSC}$ is LOW.
$\overline{ADSP}$	I	Address strobe from processor. This signal is sampled at the rising edge of CLK. When this input and/or $\overline{ADSC}$ is asserted, A_0–A_{15} will be captured in the on-chip address register. It also allows the lower two address bits to be loaded into the on-chip auto-address-increment logic. If both $\overline{ADSP}$ and $\overline{ADSC}$ are asserted at the rising edge of CLK, only $\overline{ADSP}$ will be recognized. The $\overline{ADSP}$ input should be connected to the $\overline{ADS}$ output of the processor. $\overline{ADSP}$ is ignored when $\overline{CS}$ is HIGH.
$\overline{ADSC}$	I	Address strobe from cache controller. This signal is sampled at the rising edge of CLK. When this input and/or $\overline{ADSP}$ is asserted, A_0–A_{15} will be captured in the on-chip address register. It also allows the lower two address bits to be loaded into the on-chip auto-address-increment logic. The $\overline{ADSC}$ input should *not* be connected to the $\overline{ADS}$ output of the processor.
$\overline{WH}$	I	Write signal for the high-order half of the RAM array. This signal is sampled by the rising edge of CLK. If $\overline{WH}$ is sampled as LOW, i.e., asserted, the control logic will perform a self-timed write of $DQ_{15} - DQ_8$ and DP_1 from the on-chip data register into the selected RAM location. There is one exception to this. If $\overline{ADSP}$, $\overline{WH}$, and $\overline{CS}$ are asserted (LOW) at the rising edge of CLK, the write signal, $\overline{WH}$, is ignored. Note that $\overline{ADSP}$ has no effect on $\overline{WH}$ if $\overline{CS}$ is HIGH.
$\overline{WL}$	I	Write signal for the low-order half of the RAM array. This signal is sampled by the rising edge of CLK. If $\overline{WL}$ is sampled as LOW, i.e., asserted, the control logic will perform a self-timed write of $DQ_7 - DQ_0$ and DP_0 from the on-chip data register into the selected RAM location. There is one exception to this. If $\overline{ADSP}$,$\overline{WL}$, and $\overline{CS}$ are asserted (LOW) at the rising edge of CLK, the write signal, $\overline{WL}$, is ignored. Note that $\overline{ADSP}$ has no effect on $\overline{WL}$ if $\overline{CS}$ is HIGH.
$\overline{ADV}$	I	Advance. This signal is sampled by the rising edge of CLK. When it is asserted, it automatically increments the two-bit on-chip auto-address-increment counter. In the CY7C1332, the address will be incremented linearly. In the CY7C1331, the address will be incremented according to the Pentium/486 burst sequence. This signal is ignored if $\overline{ADSP}$ or $\overline{ADSC}$ is asserted concurrently with $\overline{CS}$. Note that $\overline{ADSP}$ has no effect on $\overline{ADV}$ if $\overline{CS}$ is HIGH.
$\overline{CS}$	I	Chip select. This signal is sampled by the rising edge of CLK. If $\overline{CS}$ is HIGH and $\overline{ADSC}$ is LOW, the SRAM is deselected. If $\overline{CS}$ is LOW and $\overline{ADSC}$ or $\overline{ADSP}$ is LOW, a new address is captured by the address register. If $\overline{CS}$ is HIGH, $\overline{ADSP}$ is ignored.

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Pin Descriptions (continued)

Signal Name	I/O	Description
$\overline{OE}$	I	Output enable. This signal is an asynchronous input that controls the direction of the data I/O pins. If $\overline{OE}$ is asserted (LOW), the data pins are outputs, and the SRAM can be read (as long as $\overline{CS}$ was asserted when it was sampled at the beginning of the cycle). If $\overline{OE}$ is deasserted (HIGH), the data I/O pins will be three–stated, functioning as inputs, and the SRAM can be written.
Bidirectional Signals		
DQ15-DQ0	I/O	Sixteen bidirectional data I/O lines. $DQ_{15} - DQ_8$ are inputs to and outputs from the high-order half of the RAM array, while $DQ_7 - DQ_0$ are inputs to and outputs from the low-order half of the RAM array. As inputs, they feed into an on-chip data register that is triggered by the rising edge of CLK. As outputs, they carry the data read from the selected location in the RAM array. The direction of the data pins is controlled by $\overline{OE}$: when $\overline{OE}$ is high, the data pins are three-stated and can be used as inputs; when $\overline{OE}$ is low, the data pins are driven by the output buffers and are outputs. $DQ_{15} - DQ_8$ and $DQ_7 - DQ_0$ are also three-stated when $\overline{WH}$ and $\overline{WL}$, respectively, are sampled LOW at clock rise.
DP1–DP0	I/O	Two bidirectional data I/O lines. These operate in exactly the same manner as $DQ_{15} - DQ_0$, but are named differently because their primary purpose is to store parity bits, while the DQs' primary purpose is to store ordinary data bits. DP_1 is an input to and an output from the high-order half of the RAM array, while DP_0 is an input to and an output from the lower-order half of the RAM array.

Maximum Ratings

(Above which the useful life may be impaired. For user guidelines, not tested.)

Storage Temperature ..... – 65°C to +150°C
Ambient Temperature with
Power Applied ..... – 55°C to +125°C
Supply Voltage on V_{CC} Relative to GND ... – 0.5V to +3.6V
DC Voltage Applied to Outputs
in High Z State[2] ..... – 0.5V to V_{CC} + 0.3V
DC Input Voltage[2] ..... – 0.5V to V_{CC} + 0.3V
Current into Outputs (LOW) ..... 20 mA
Static Discharge Voltage ..... >2001V
(per MIL-STD-883, Method 3015)
Latch-Up Current ..... >200 mA

Operating Range

Range	Ambient Temperature[3]	V_{CC}, V_{CCQ}
Com'l	0°C to +70°C	3.3V ± 0.3V
Mil	– 55°C to +125°C	3.3V ± 0.3V

Electrical Characteristics Over the Operating Range[4]

Parameter	Description	Test Conditions		7C1331–12 7C1332–12 Min.	7C1331–12 7C1332–12 Max.	7C1331–16 7C1332–16 Min.	7C1331–16 7C1332–16 Max.	7C1331–19 7C1332–19 Min.	7C1331–19 7C1332–19 Min.	Unit
V_{OH}	Output HIGH Voltage	V_{CC} = Min., I_{OH} = –2.0 mA		2.4		2.4		2.4		V
V_{OL}	Output LOW Voltage	V_{CC} = Min, I_{OL} = 2.0 mA			0.4		0.4		0.4	V
V_{IH}	Input HIGH Voltage			2.0	V_{CC} +0.3V	2.0	V_{CC} +0.3V	2.0	V_{CC} +0.3V	V
V_{IL}	Input LOW Voltage[2]			–0.3	0.8	–0.3	0.8	–0.3	0.8	V
I_X	Input Load Current	$GND \leq V_I \leq V_{CC}$		–1	+1	–1	+1	–1	+1	µA
I_{OZ}	Output Leakage Current	$GND \leq V_I \leq V_{CC}$, Output Disabled		–5	+5	–5	+5	–5	+5	µA
I_{OS}	Output Short Ciruit Current[5]	V_{CC} = Max., V_{OUT} = GND			–300		–300		–300	mA
I_{CC}	V_{CC} Operating Supply Current	V_{CC}=Max., Iout=0mA, $f=f_{MAX}=1/t_{RC}$	Com'l		180		160		150	mA
			Mil						170	

Notes:
2. Minimum voltage equals – 2.0V for pulse durations of less than 20 ns.
3. T_A is the "instant on" case temperature.
4. See the last page of this specification for Group A subgroup testing information.
5. Not more than one output should be shorted at one time. Duration of the short circuit should not exceed 30 seconds.

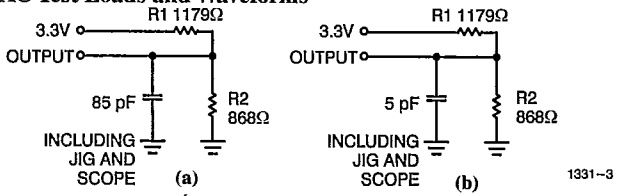
Electrical Charaierictics (continued)

Parameter	Description	Test Conditions		7C1331–12 7C1332–12 Min.	7C1331–12 7C1332–12 Max.	7C1331–16 7C1332–16 Min.	7C1331–16 7C1332–16 Max.	7C1331–19 7C1332–19 Min.	7C1331–19 7C1332–19 Min.	Unit
I_{SB1}	Automatic CE Power-Down Current – TTL Inputs	Max. V_{CC}, $\overline{CS} \geq V_{IH}$, $V_{IN} \geq V_{IH}$ or $V_{IN} \leq V_{IL}$, f=f_{MAX}	Com'l		30		30		30	mA
			Mil						30	
I_{SB2}	Automatic CE Power-Down Current –CMOS Inputs	Max. V_{CC}, $\overline{CS} \geq V_{CC}$ –0.3V, $V_{IN} \geq V_{CC}$ –0.3V or $V_{IN} \leq$ 0.3V, f=0 [6]	Com'l		10		10		10	mA
			Mil						10	

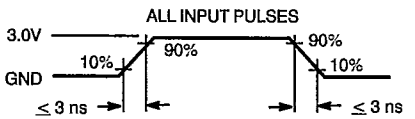
Capacitance[7]

Parameter	Description	Test Conditions		Max.	Unit
C_{IN}: Addresses	Input Capacitance	T_A = 25°C, f = 1 MHz, V_{CC} = 3.3V	Com'l	4	pF
			Mil	6	
C_{IN}: Other Inputs	Input Capacitance		Com'l	6	pF
			Mil	8	
C_{OUT}	Output Capacitance		Com'l	6	pF
			Mil	8	

AC Test Loads and Waveforms

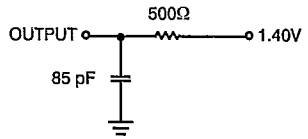


1331–3



1331–4

Equivalent to: THÉVENIN EQUIVALENT



Notes:

6. Clock signal allowed to run at speed.
7. Tested initially and after any design or process changes that may affect these parameters.

Switching Characteristics Over the Operating Range[8]

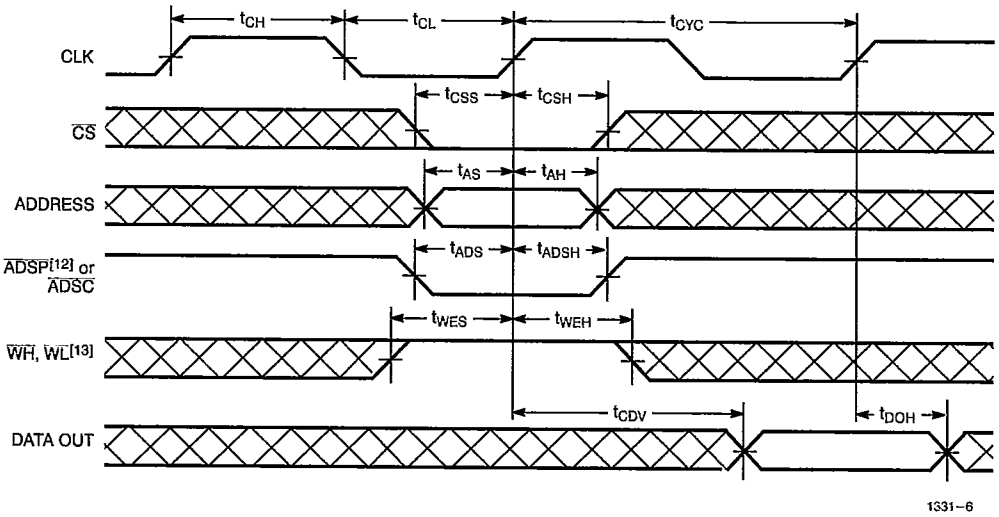
Parameter	Description	7C1331–12 7C1331–12		7C1331–16 7C1331–16		7C1331–19 7C1332–19		Unit
		Min.	Max.	Min.	Max.	Min.	Max.	
t_{CYC}	Clock Cycle Time	20		25		30		ns
t_{CH}	Clock HIGH	8		9		12		ns
t_{CL}	Clock LOW	8		9		12		ns
t_{AS}	Address Set-Up Before CLK Rise	3		4		5		ns
t_{AH}	Address Hold After CLK Rise	1		2		3		ns
t_{CDV1}	Data Output Valid After CLK Rise, 0-pF Load		12.5		16.5		19.5	
t_{CDV2}	Data Output Valid After CLK Rise		14		18		21	ns
t_{DOH}	Data Output Hold After CLK Rise	3		3		3		ns
t_{ADS}	$\overline{ADSP}$, $\overline{ADSC}$ Set-Up Before CLK Rise	3		4		5		ns
t_{ADSH}	$\overline{ADSP}$, $\overline{ADSC}$ Hold After CLK Rise	1		2		3		ns
t_{WES}	$\overline{WH}$, $\overline{WL}$ Set-Up Before CLK Rise	3		4		5		ns
t_{WEH}	$\overline{WH}$, $\overline{WL}$ Hold After CLK Rise	1		2		3		ns
t_{ADVS}	$\overline{ADV}$ Set-Up Before CLK Rise	3		4		5		ns
t_{ADVH}	$\overline{ADV}$ Hold After CLK Rise	1		2		3		ns
t_{DS}	Data Input Set-Up Before CLK Rise	3		4		5		ns
t_{DH}	Data Input Hold After CLK Rise	1		2		3		ns
t_{CSS}	Chip Select Set-Up	3		4		5		ns
t_{CSH}	Chip Select Hold After CLK Rise	1		2		3		ns
t_{CSOZ}	Chip Select Sampled to Output High Z[9]	2	7	2	8	2	11	ns
t_{EOZ}	$\overline{OE}$ HIGH to Output High Z[9]	2	7	2	8	2	11	ns
t_{EOV}	$\overline{OE}$ LOW to Output Valid		6		7		8	ns
t_{WEOZ}	$\overline{WH}$ or $\overline{WL}$ Sampled LOW to Output High Z[9,10]		7		8		11	ns
t_{WEOV}	$\overline{WH}$ or $\overline{WL}$ Sampled HIGH to Output Valid[10]		14		18		21	ns

Notes:

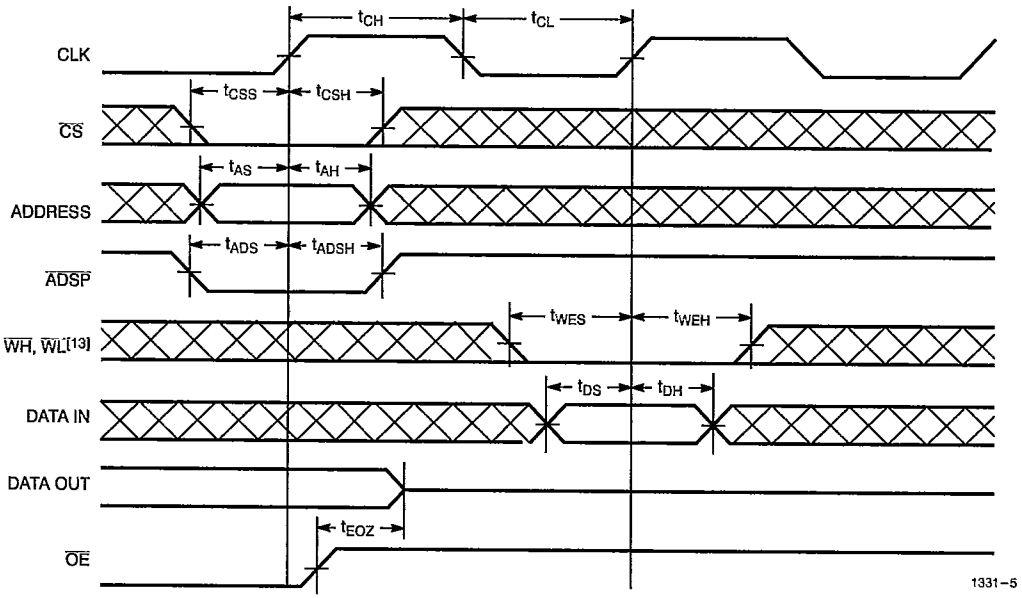
8. Unless otherwise noted, test conditions assume signal transition time of 3 ns or less, timing reference levels of 1.5V, input pulse levels of 0 to 3.0V, and output loading of the specified I_{OL}/I_{OH} and 85-pF load capacitance.
9. t_{CSOZ}, t_{EOZ}, and t_{WEOZ} are specified with a load capacitance of 5 pF as in part (b) of AC Test Loads. Transition is measured ± 500 mV from steady-state voltage.
10. At any given voltage and temperature, t_{WEOZ} min. is less than t_{WEOV} min.

Switching Waveforms

Single Read[11]



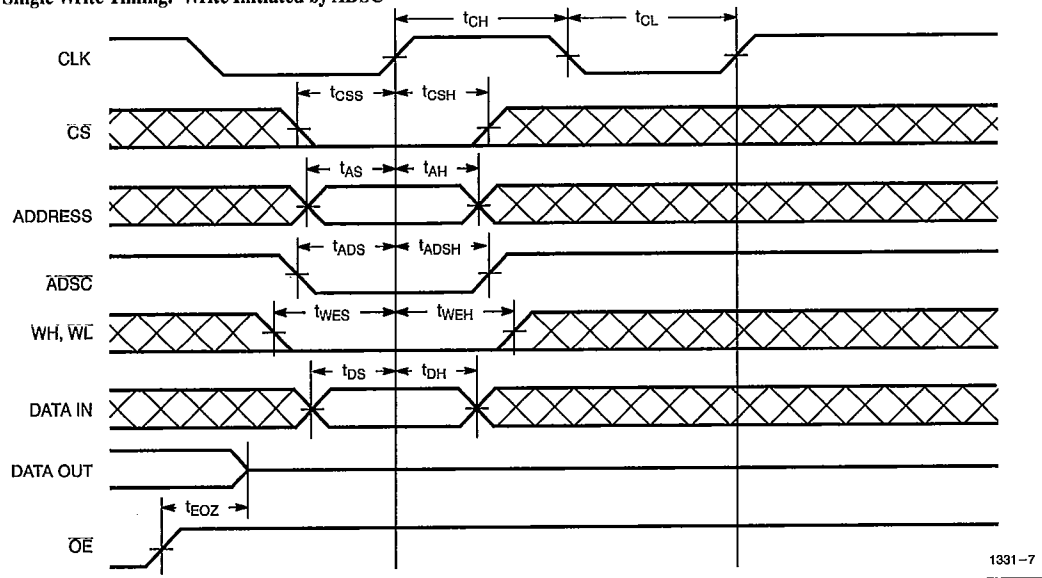
Single Write Timing: Write Initiated by $\overline{ADSP}$



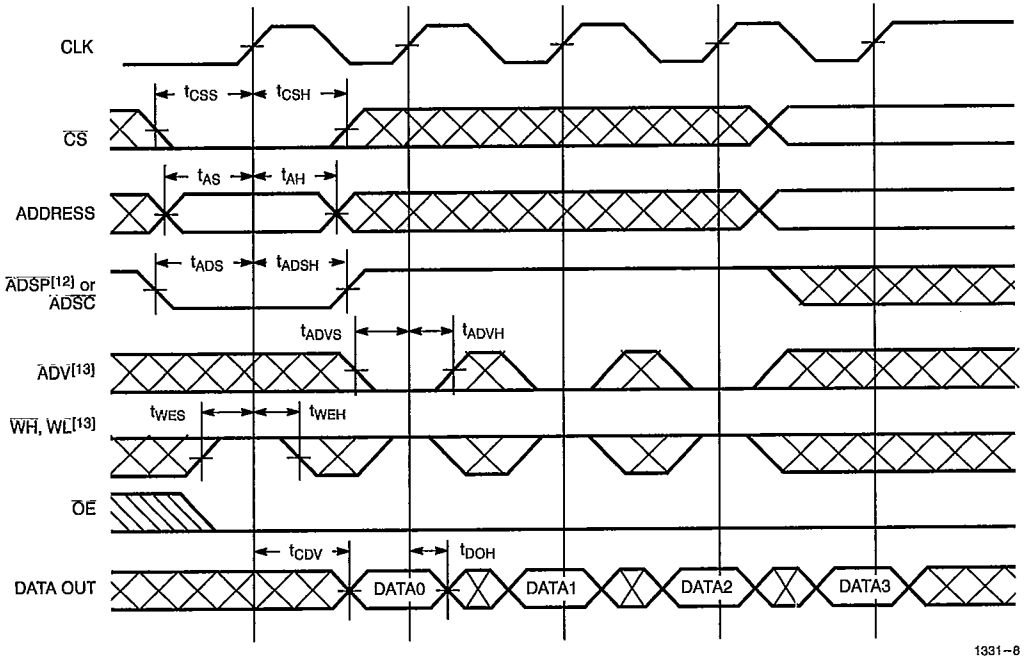
Notes:
11. $\overline{OE}$ is LOW throughout.
12. If $\overline{ADSP}$ is asserted while $\overline{CS}$ is HIGH, $\overline{ADSP}$ will be ignored.
13. $\overline{ADSP}$ has no effect on $\overline{ADV}$, $\overline{WH}$, and $\overline{WL}$ if $\overline{CS}$ is HIGH.

Switching Waveforms (continued)

Single Write Timing: Write Initiated by $\overline{ADSC}$

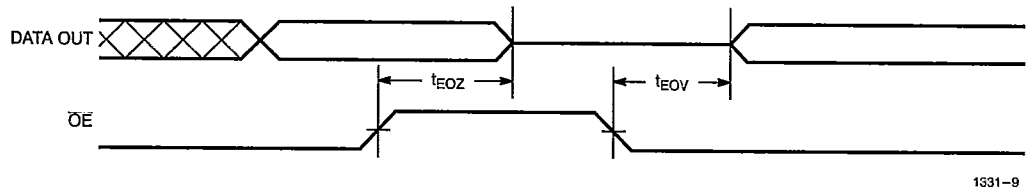


Burst Read Sequence with Four Accesses



Switching Waveforms (continued)

Output (Controlled by $\overline{OE}$)



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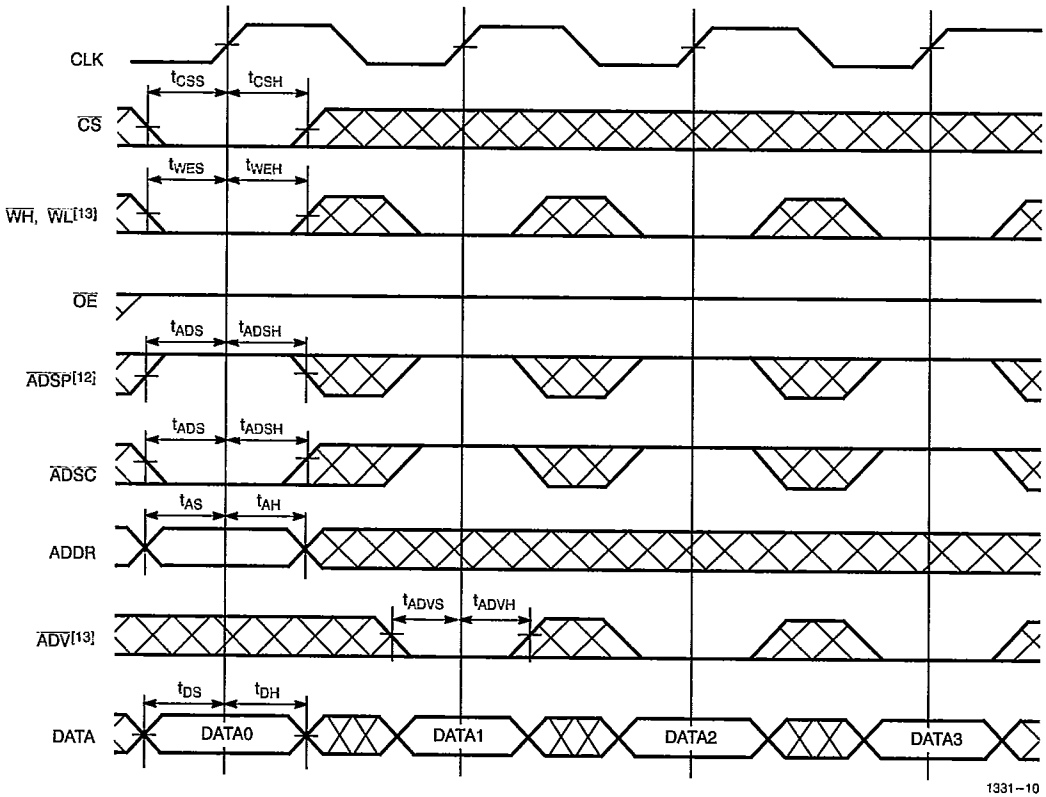
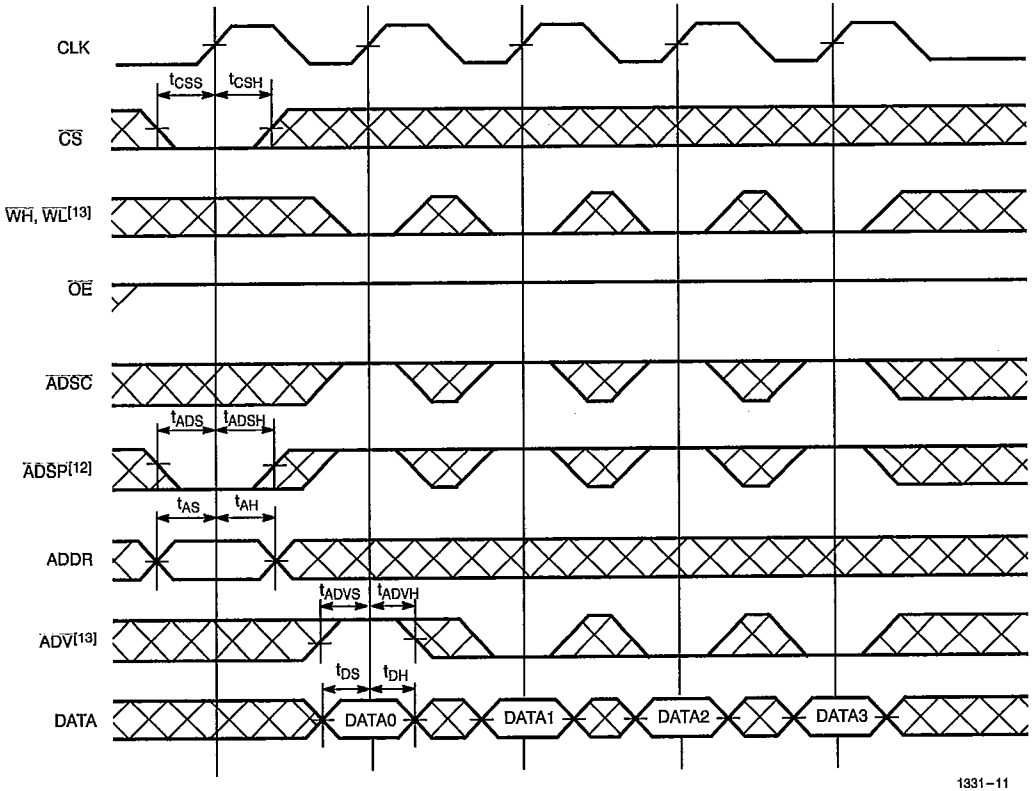
Write Burst Timing: Write Initiated by $\overline{ADSC}$



1331–10

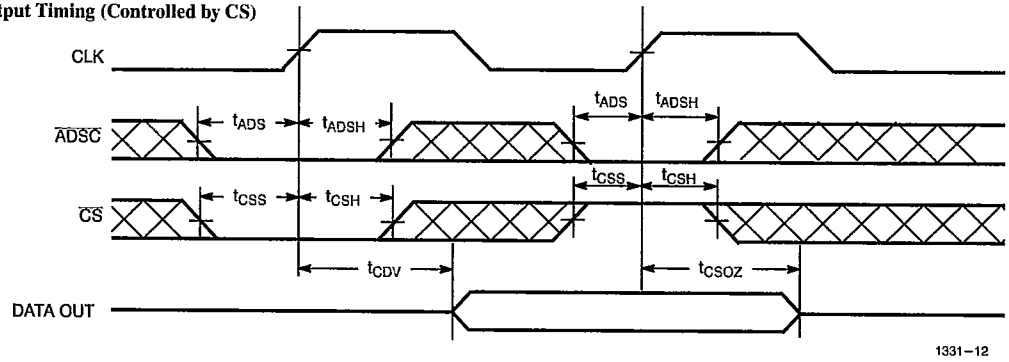
Switching Waveforms (continued)

Write Burst Timing: Write Initiated by $\overline{ADSP}$

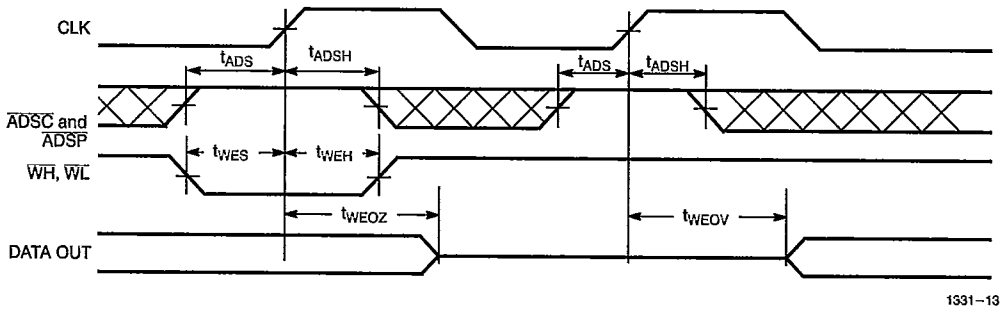


Switching Waveforms (continued)

Output Timing (Controlled by CS)



Output Timing (Controlled by $\overline{WH}/\overline{WL}$)



Truth Table

Inputs						Address	Operation
$\overline{CS}$	$\overline{ADSP}$	$\overline{ADSC}$	$\overline{ADV}$	$\overline{WH}$ or $\overline{WL}$	CLK		
H	X	L	X	X	L→H	N/A	Chip deselected
H	L	H	H	H	L→H	Same address as previous cycle	Read cycle ($\overline{ADSP}$ ignored)
H	L	H	L	H	L→H	Incremented burst address	Read cycle, in burst sequence ($\overline{ADSP}$ ignored)
H	L	H	H	L	L→H	Same address as previous cycle	Write cycle ($\overline{ADSP}$ ignored)
H	L	H	L	L	L→H	Incremented burst address	Write cycle, in burst sequence ($\overline{ADSP}$ ignored)
L	L	X	X	X	L→H	External	Read cycle, begin burst
L	H	L	X	H	L→H	External	Read cycle, begin burst
L	H	L	X	L	L→H	External	Write cycle, begin burst
X	H	H	L	L	L→H	Incremented burst address	Write cycle, begin burst
X	H	H	L	H	L→H	Incremented burst address	Read cycle, begin burst
X	H	H	H	L	L→H	Same address as previous cycle	Write cycle
X	H	H	H	H	L→H	Same address as previous cycle	Read cycle

Ordering Information

Speed (ns)	Ordering Code	Package Name	Package Type	Operating Range
12	CY7C1331–12JC	J69	52-Lead Plastic Leaded Chip Carrier	Commercial
	CY7C1331–12NC	TBD	52-Lead Plastic Quad Flatpack	
16	CY7C1331–16JC	J69	52-Lead Plastic Leaded Chip Carrier	Commercial
	CY7C1331–16NC	TBD	52-Lead Plastic Quad Flatpack	
19	CY7C1331–19JC	J69	52-Lead Plastic Leaded Chip Carrier	Commercial
	CY7C1331–16NC	TBD	52-Lead Plastic Quad Flatpack	

Speed (ns)	Ordering Code	Package Name	Package Type	Operating Range
12	CY7C1332–12JC	J69	52-Lead Plastic Leaded Chip Carrier	Commercial
	CY7C1332–12NC	TBD	52-Lead Plastic Quad Flatpack	
16	CY7C1332–16JC	J69	52-Lead Plastic Leaded Chip Carrier	Commercial
	CY7C1332–16NC	TBD	52-Lead Plastic Quad Flatpack	
19	CY7C1332–19JC	J69	52-Lead Plastic Leaded Chip Carrier	Commercial
	CY7C1332–19NC	TBD	52-Lead Plastic Quad Flatpack	

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CYPRESS SEMICONDUCTOR

PLCC and CLCC Packaging for High-Speed Parts

The semiconductor industry is constantly searching for package options that enhance the capabilities of high-performance devices. For fast device performance with minimal ground bounce, electrical characteristics must include low inductance and capacitance from external pin to die bond-wire pad. A package should also furnish good thermal characteristics for reliability over extended temperature ranges.

Other major properties sought after are low cost, as well as standardized outline/pin configurations for compatibility, ease of manufacturing, and handling throughput. The package must also work with surface mount technology and have a small footprint to save board space.

The package that best meets all these requirements is the PLCC (plastic leaded chip carrier). In the past, utilization of PLCCs was not practical for high-power, bipolar devices. However, the advent of low-power bipolar and BiCMOS ECL-compatible SRAMs and PLDs now provides the opportunity for high-volume usage. As manufacturers switch from bipolar to BiCMOS, the lower power dissipation of high-density ECL SRAMs and complex PLDs promise to give PLCC packages a bright future. For military applications and extended temperature environments or for devices with higher power dissipation, you can substitute the CLCC (ceramic leaded chip carrier).

The PLCC has many desirable qualities:

- Suitable for surface mounting with J-type leads
- Small footprint to save board space
- Low inductance and capacitance for high speed with little ground-bounce
- Good thermal characteristics for reliability over temperature range
- Ease of manufacturing and handling for production throughput
- Low cost compared to CERDIP, flatpack, LCC
- Standard package outline and pin-configuration compatibility

The PLCC's J-type surface-mount leads have the advantage over gull-wing leads, which are susceptible to fatigue. J leads also enhance handling ease in test and burn-in fixtures. The PLCC's 1-pF capacitance compares favorably with the 3 and 6 pF for plastic DIPs and CERDIPs, and inductance is equally impressive: 2 nH versus 6 and 11 nH for plastic DIP and CERDIP. Unlike flatpacks, PLCCs are available in standard tooling. PLCCs come in a variety of pin configurations, from 18 to over 200 pins, versus a maximum of 40 pins for plastic DIPs.

The Ceramic Leaded Chip Carrier

For high-temperature environments and high-power devices, you can make use of the ceramic leaded chip carrier (CLCC, Y package), which can also be surface mounted. The Y package has the same footprint and J leads as the PLCC (*Figure 1*) and works well for the faster PLDs and SRAMs.

If you do not know system temperature in the early stages of a design, you can substitute the Y package for the PLCC and vice versa, so long as the device's die junction temperature does not exceed 150°C. The Y package is slightly more expensive than the PLCC, but with a thermal resistance from junction to ambient (Θ_{JA}) of 35°C/W at 500 LFPM, the Y package can dissipate heat more efficiently.

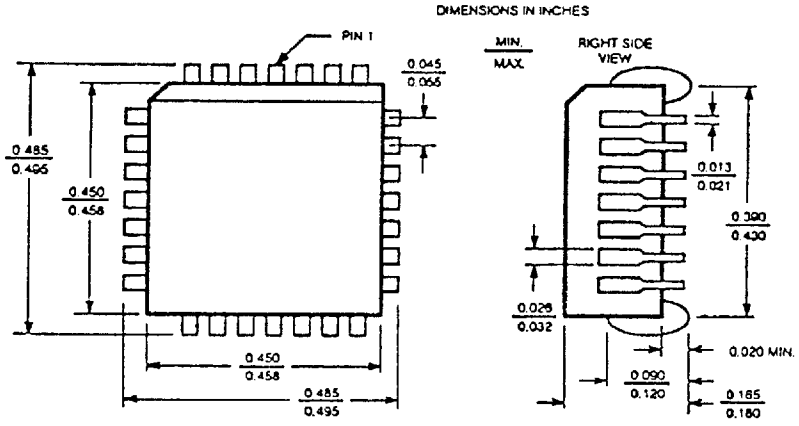
Reliability

Cypress's bipolar and BiCMOS products in PLCC and CLCC packages go through extensive burn-in and testing at elevated temperature to guarantee package integrity. Cypress strongly recommends 500-LFPM system forced air flow but guarantees reliability in systems with or without the flow if the ambient air does not cause the junction temperature (T_J) to exceed 150°C.

The PLCC's Θ_{JA} is approximately 45°C/W. The SRAMs have power dissipation that ranges from 780 mW max for the CY100E422L-5 up to 1097 mW max for the CY10E474L-5. This dissipation results in junction temperature rises from 35 to 49°C. The 16P4-type PLD (CY100E302L-6) has a temperature rise of 39°C, and the

T-90-20

28-Lead Plastic Leaded Chip Carrier J64



28-Pin Ceramic Leaded Chip Carrier Y64

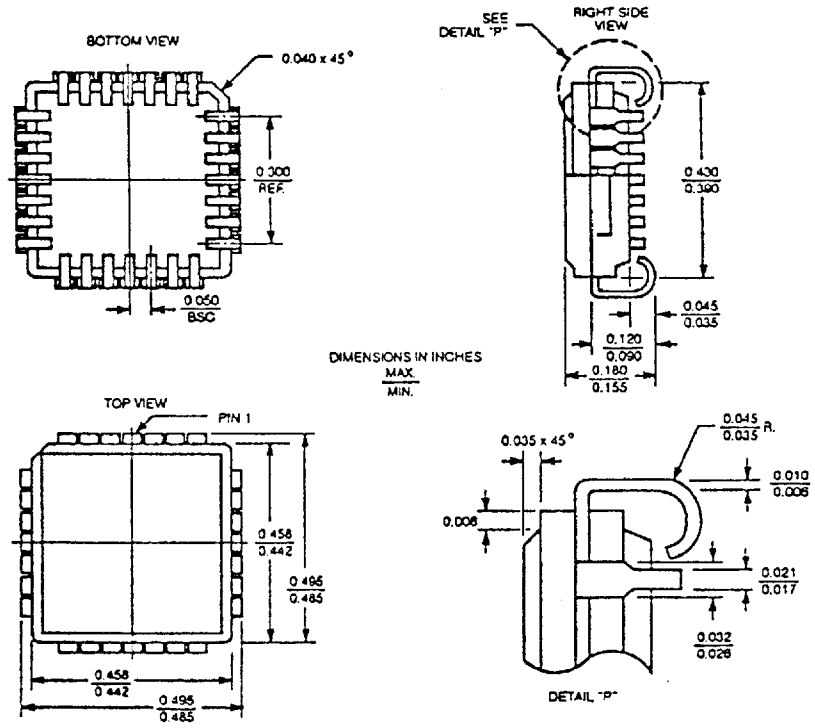


Figure 1. Diagrams of 28-Lead Chip Carriers

16P8-type PLD (CY10E301L-6) has a temperature rise of 47°C. The CLCC package's Θ_{JA} equals 35°C/W for temperature rises of up to 55°C (CY10E474-3).

Finding Chip-Level Junction Temperature

The following relationship determines chip-level junction temperature for the PLCC package:

$T_J = \Delta T + T_A$

where

$\Delta T = P_D \times \Theta_{JA}$

and

$\Theta_{JA} = \Theta_{JC} + \Theta_{CS} + \Theta_{SA}$

To calculate worst case junction temperature (T_J) use maximum supply V_{EE} and I_{EE} for power dissipation and maximum T_A for the temperature range of interest. For the 10K/10KH CY10E301L in a PLCC, for example, device I_{EE} = 170 mA max and V_{EE} = 5.46V max for P_D = 928 mW. Add 15 mW per output for a total output P_D = 120 mW. Therefore, the total P_D = 1048 mW.

For a PLCC, Θ_{JA} = 45°C/W at 500 LFPM, and Θ_{JA} = 64°C/W for still air.

For a CLCC, Θ_{JA} = 35°C/W at 500 LFPM, and Θ_{JA} = 54°C/W for still air.

Because

T_J = total $P_D \times \Theta_{JA} + T_A$

and

T_A = 75°C worst-case commercial temperature range, for the PLCC:

$T_J = (1.048\ W)(45°C/W) + 75°C = 122°C$ at 500 LFPM

$T_J = (1.048\ W)(64°C/W) + 75°C = 142°C$ in still air

This calculation is for absolute worst-case data sheet conditions. The burn-in temperature used by Cypress (T_J) is much higher than the device will ever see in a system. Note that *most systems will not run at worst case due to guard-banding*. For this reason, use V_{EENOM} = 5.2V or 4.5V and $I_{EENOM} = (I_{EEMAX})(85\%)$ for nominal-condition calculations.

Real-World Values

Obviously, most systems do not operate at the worst-case conditions. Therefore, *Figures 2* through *5* show graphs over different operating conditions to determine failures in time (FITs) and mean time between failure (MTBF) for a typical system or in a worst-case scenario.

The graphs are based on a linear method of interpreting the failures observed at burn-in and indicate the long-term reliability of Cypress devices. You can use the graphs to determine MTBF and FITs for any Cypress device in any package after calculating the appropriate ΔT.

The X-axis on the graphs indicates junction temperature. These values are determined by adding the ΔT to ambient temperature, as described earlier. As an example, *Figures 2* and *3* note the following critical points for a CY10E301L ECL PLD under three different operating conditions:

- Point A — 10K/10KH typical data sheet conditions: 25°C ambient, nominal V_{EE} and I_{EE}, 50Ω loads, 500 LFPM air flow, T_J = 64°C, FITs = 7, MTBF = 18,000 yrs.
- Point B — 10K/10KH typical operating conditions: 55°C ambient, nominal V_{EE} and I_{EE}, 50Ω loads, 500 LFPM air flow, T_J = 94°C, FITs = 45, MTBF = 2800 yrs.
- Point C — 10K/KH absolute worst-case conditions: 75°C ambient, 5.46 V max and 170 mA max, 50Ω loads, 500 LFPM air flow, T_J = 122°C, FITs = 225, MTBF = 525 yrs.

The activation energy used for the MTBF and FITs information is 0.7 eV. This is an average number for die-surface-related defects, such as metal and oxide pinholes, etc., but is very conservative for silicon defects or mechanical interfaces to packages. The number is usually 1.0 eV. A small change here results in a significant change in MTBF or FITs. A change to 0.8 eV equates to a 33% reduction in FITs rate or a 50% increase in MTBF.

The Packages of Choice

The PLCC and CLCC are accepted as the packages of choice by many manufacturers of high-speed devices. Motorola Semiconductor uses the PLCC as the only package for the company's very high speed ECL$_{INPS}$ ECL logic family, which stands for "ECL in picoseconds" and is pronounced "eclipse." This family has set-up times and propagation delays in the sub-nanosecond range, with power dissipation of over 1W. Fully compatible with Cypress SRAMs and PLDs, the ECL$_{INPS}$ family includes many 10K, 10KH, and 100K standard logic gates, building blocks, and transceivers.

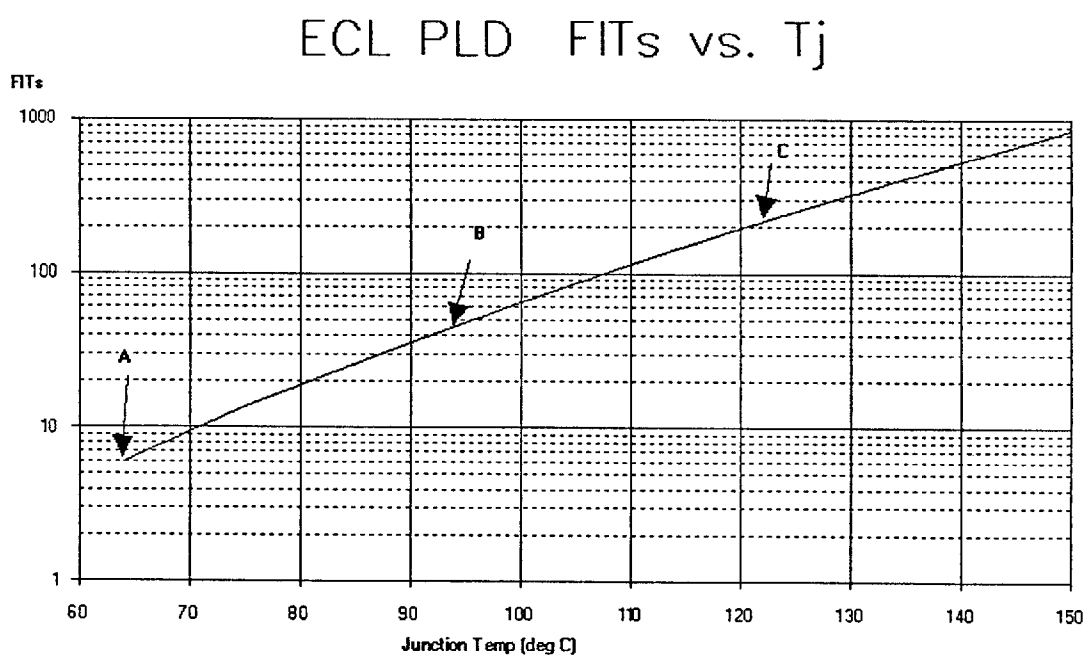


Figure 2. Failures in Time vs Junction Temperature

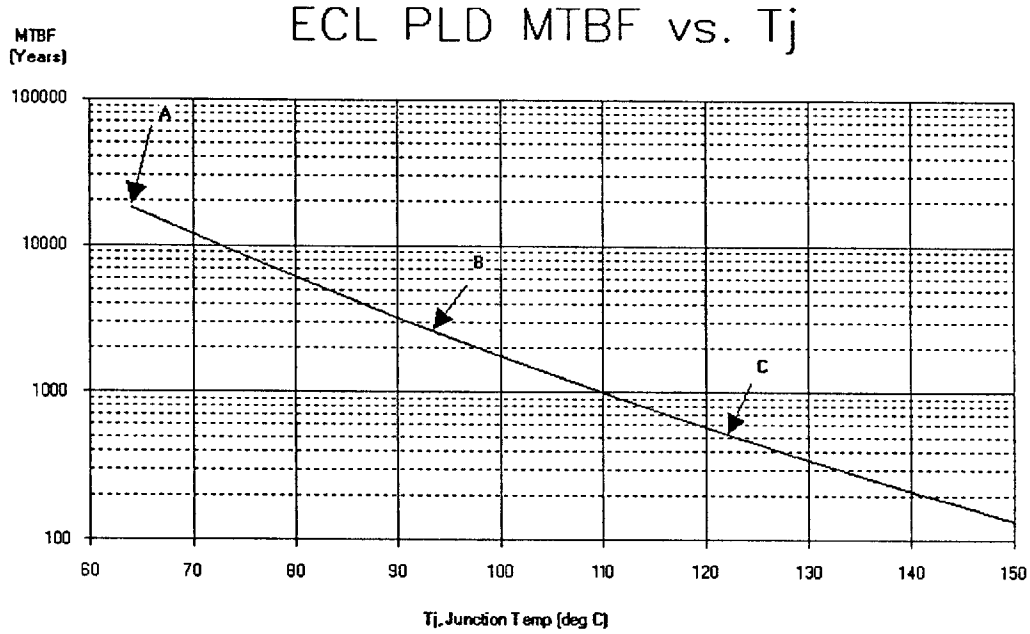


Figure 3. Mean Time Between Failures vs Junction Temp.

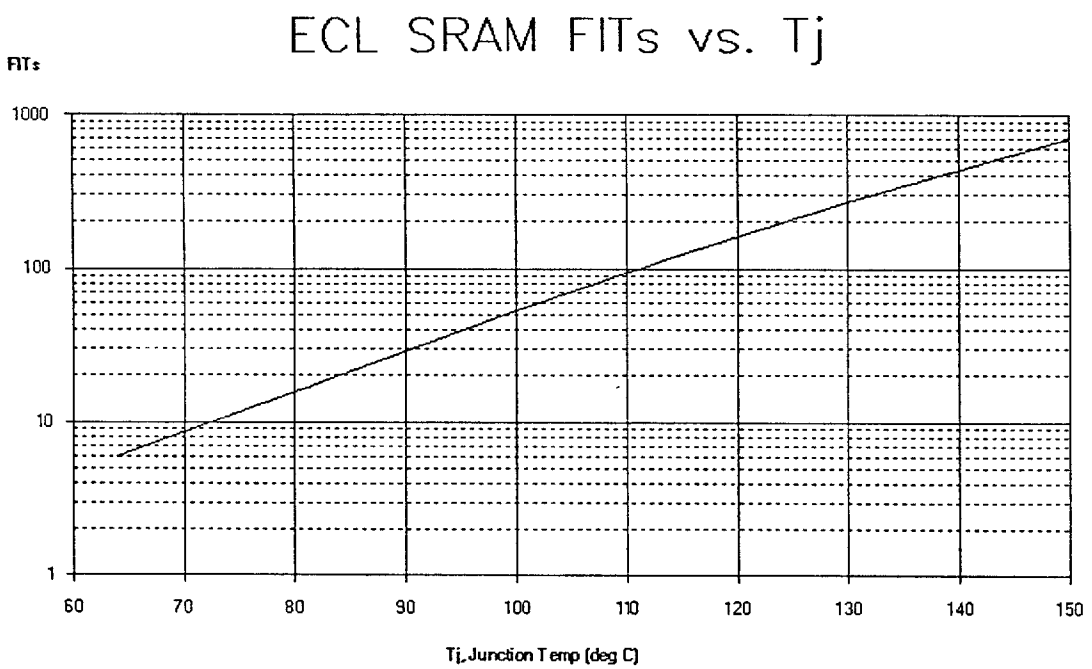


Figure 4. Failures in Time vs Junction Temperature

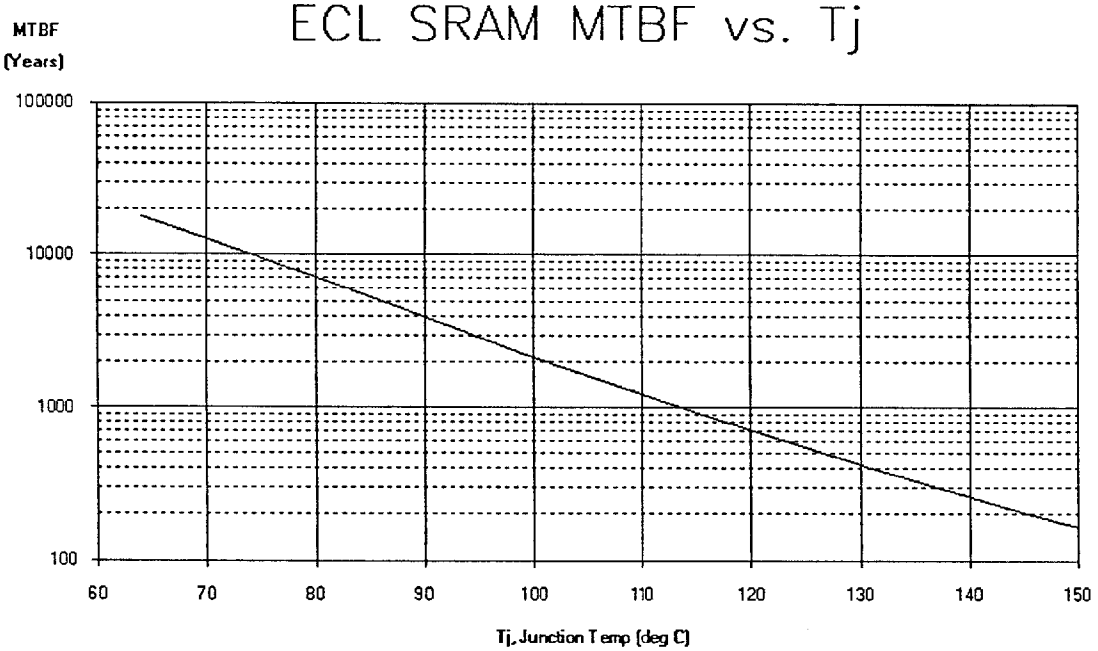


Figure 5. Mean Time Between Failure vs Junction Temp.