# Stratum 3+ Simplified Control Timing Modules STM-S3+

CONNOR WINFIELD

2111 Comprehensive Drive
Aurora, Illinois 60505
Phone: 630-851-4722
Fax: 630-851-5040
**www.conwin.com**


## Application

The Connor-Winfield Stratum 3+ Simplified Control Timing Module can be used as a complete system clock module for any Stratum 3 timing application in which the design requires the added capabilities of a Stratum 3E level Hold Over within 5°C variation in accordance with GR-1244-CORE-1995.

Connor-Winfield's Stratum 3+ Timing module helps reduce the cost of your design by minimizing your development time and maximizing your control of the system clock with our simplified design.

## Features

- 4 Operational Modes
- Stratum 3 Clocking System
- Stratum 3E Hold Over Accuracy ±5°
- Hitless Reference Switching
- 5 Active Alarms
- Guaranteed Free Run
- Lock Time of 100 Secs
- TVL Alarm

US Headquarters:
630-851-4722
European Headquarters:
+353-62-472221

## General Description

The Connor-Winfield Stratum 3+ Simplified Control Timing Module (STM-3+) meets every Stratum 3 requirement of GR-1244-CORE-1995. In addition, it also provides the enhanced Hold Over accuracy of Statum 3E specifications over ±5° C range. Control loop filters effectively attenuate any reference jitter and smooth out phase transients.

The STM-3+ is designed to be controlled externally. Full external control input allows the user to select and monitor any of the four possible operating modes:

- Free Run Mode (A=0, B=0 =>Free Run=1)
- Normal Mode #1 (A=1, B=0 => Ref 1=1)
- Normal Mode #2 (A=0, B=1 =>Ref 2=1)
- Hold Over Mode (A=1, B=1 =>Hold Over=1)

Table 4 illustrates the control signal inputs (A,B) and the corresponding operational modes. Real-time indication of the operational mode is indicated by unique operating mode outputs on pins 1-4. In addition, all outputs can be placed into a high impedence state when a high signal is placed on the Tri-State control pin

Normal Mode #1 results in an output signal that is phase locked to the External Reference Input #1. Normal Mode #2 results in an output signal that is phase locked to External Reference Input #2. Hold Over mode results in an output signal at or near the frequency as determined by a past historical value and the holdover performance of the STM. The historical value is updated every 40 secs. In the absence of External Control Inputs, the STM enters the default Free Run mode and signals an external alarm. Free Run mode is a guaranteed ±4.6 ppm of the nominal frequency.

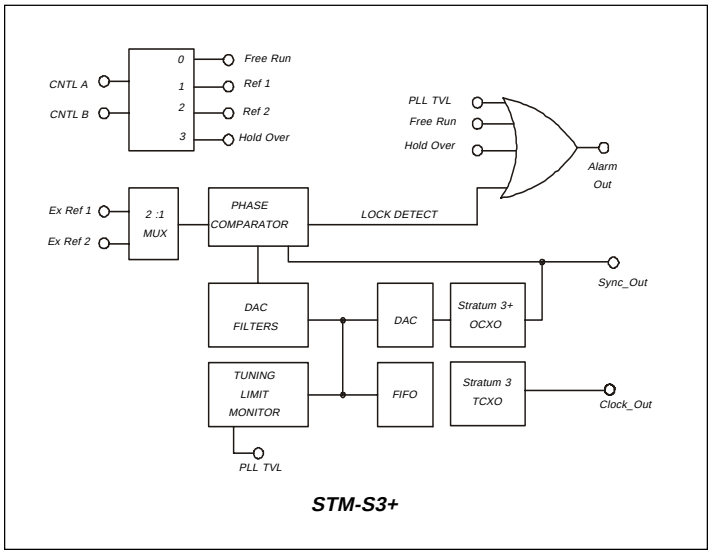
The STM-S3+ provides an alarm pin that goes high during an alarm condition. Alarm signals are generated at the Alarm Out pin during the following conditions:

- Holdover
- Free Run
- Loss of Lock (LOL)
- Loss of Reference (LOR)
- Tune-Limit (PLL_TVL)

A Tune-Limit (PLL_TVL) alarm signal indicates that the Voltage Controlled OCXO tuning voltage is approaching within the 10% limit of its lock capability and LOL may soon occur.

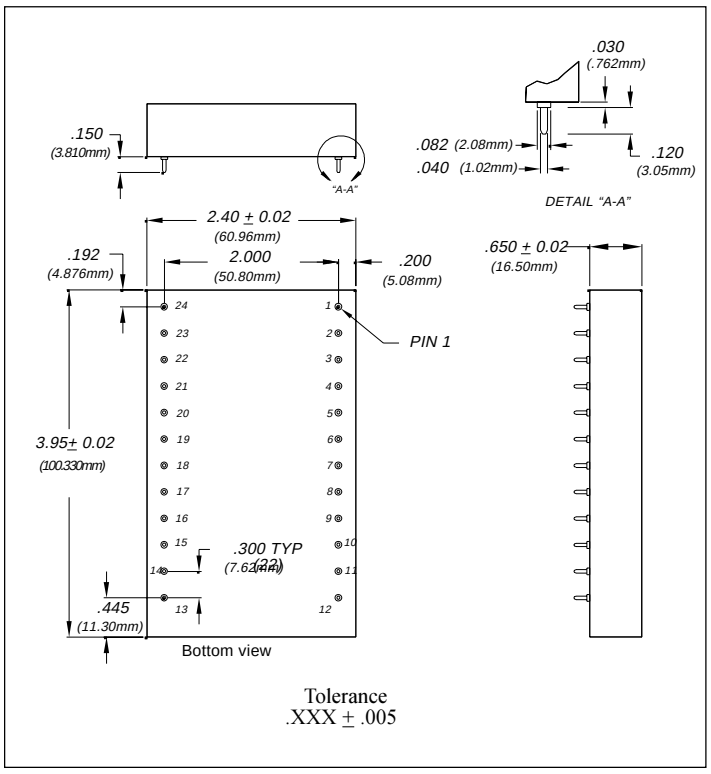
## Functional Block Diagram

Figure 1




## Package Layout

Figure 2



## Absolute Maximum Rating

Table 1 STM-S3+

| Symbol | Parameter | Minimum | Nominal | Maximum | Units | Notes |
|---|---|---|---|---|---|---|
| $V_{CC}$ | Power Supply Voltage (Vcc to GND) | -0.5 | - | +7.0 | Volts | 1.0 |
| $V_{IN}$ | Input Voltage | -0.5 | - | +5.5 | Volts | 1.0 |
| $T_{STG}$ | Storage Temperature | -40.0 | - | +90 | deg. C | 1.0 |

## Recommended Operating Conditions

Table 2 STM-S3+

| Symbol | Parameter | Minimum | Nominal | Maximum | Units | Notes |
|---|---|---|---|---|---|---|
| $V_{CC}$ | Power Supply Voltage (vcc to GND) | 4.75 | 5.0 | 5.25 | V | |
| $V_{POR}$ | Power-on Reset Voltage Level | 4.25 | | 4.5 | V | 2.0 |
| $V_{IH}$ | High Level Input Voltage (TTL Compatible) | 2.0 | | 5.25 | V | |
| $V_{IL}$ | Low Level Input Voltage (TTL Compatible) | 0.0 | | 0.8 | V | |
| $T_{IN}$ | Input Signal Transition Time | | | 250.0 | nS | |
| $C_{IN}$ | Input Capacitance | | | 15.0 | pF | |
| $V_{OH}$ | High Level Output Voltage @IOH=8.0 mA, Vcc minimum | 2.4 | | | V | 3.0 |
| $V_{OL}$ | Low Level Output Voltage @IOH=8.0 mA, Vcc maximum | | | 0.4 | V | |
| $T_{HL}$ | Clock out transition time high-to-low, no load | | 4.0 | | nS | |
| $T_{LH}$ | Clock out transition time low-to-high, no load | | 4.0 | | nS | |
| $T_{RIP}$ | Input 8 kHz reference signal positive pulse width | 30.0 | | | nS | |
| $T_{RIN}$ | Input 8 kHz reference signal Negative pulse width | 30.0 | | | nS | |
| $T_{AB}$ | Mode Select Response | | 2 | | mS | |
| $T_{OP}$ | Standard Opearting temperature | 0.0 | | 70.0 | deg. C | |

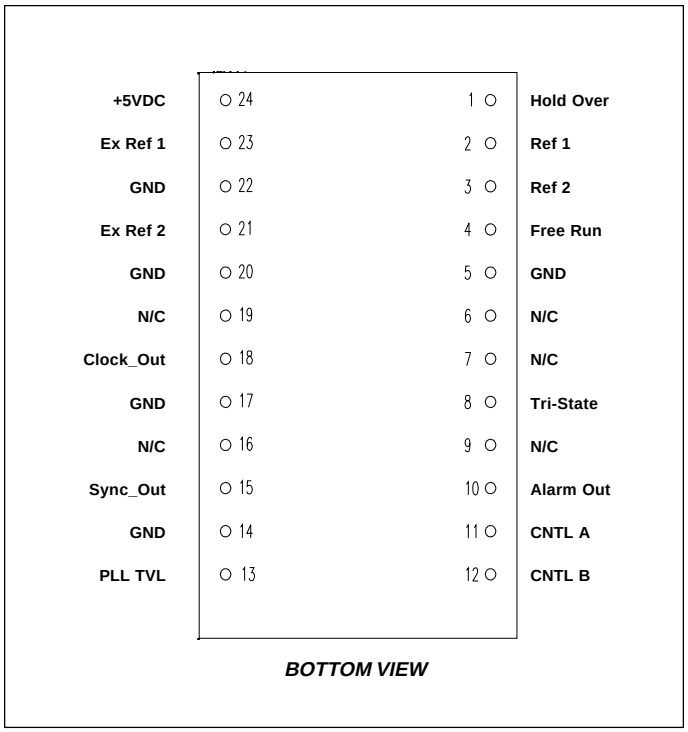
## Operating Specifications

Table 3 STM-S3+

| Parameter | Specifications | | Notes |
|---|---|---|---|
| Frequency Range | 16.384 MHz, 19.44 MHz, 38.88 MHz | | |
| Supply Current | 350 mA Typical, 550 mA during warmup | | |
| Timing Reference Inputs | GR-1244-CORE 3.2.1, R3-1 | | |
| Jitter, Phase Transient and Wander Tolerances | GR-1244-CORE 4.2-4.4 | | |
| Wander Genration | GR-1244-CORE 4.2-4.4 | | |
| Free Run Accuracy | ±4.6 ppm | | |
| Holdover Stability | (0° - 70°) ±0.039 ppm | (±5°C) ±0.012 ppm | 4.0 |
| Initial Offset | ±0.001 ppm | ±0.001 ppm | |
| Temperature | ±0.035 ppm | ±0.010 ppm | |
| Drift | ±0.003 ppm | ±0.001 ppm | |
| Holdover History | 40 sec | | |
| Pull-in / Hold-in Range | ±4.6 ppm | | 5.0 |
| Lock Time | < 100 sec | | |
| Lock Accuracy | 0.001 ppm | | 6.0 |
| PLL-TVL Alarm Limits | Within 10% of Tuning Range Limit, See Fig 8 | | |

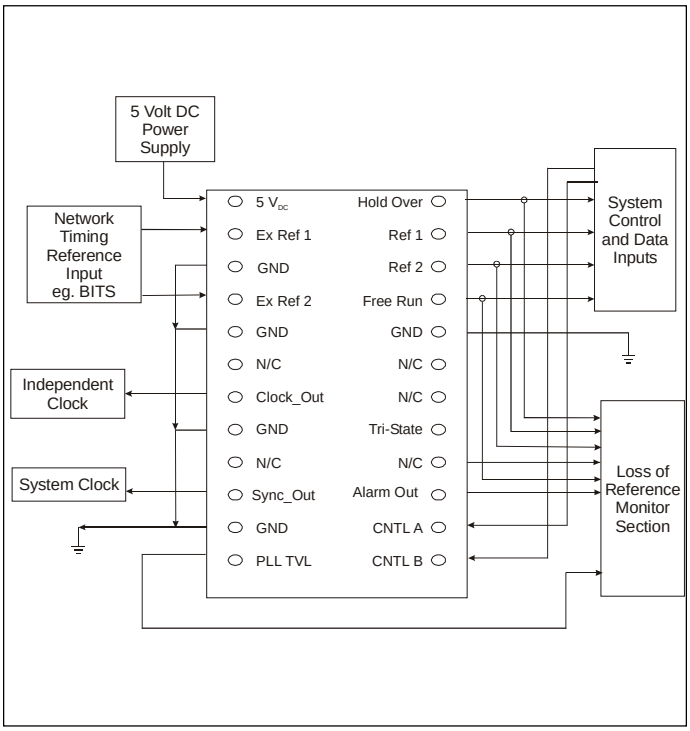
## Pin Assignment

Figure 3




## Typical Application

Figure 4




## Operational Modes

Table 4

| Control Input Pins | | | Operational Mode | | Output Indicator Pins | | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|---|
| Tri-State | A | B | | | Ref 1 | Ref 2 | Hold Over | Free Run | PLL_TVL | Alarm Out | *Clock-Out Sync Out |
| 0 | 0 | 0 | Free Run (default) | | 0 | 0 | 0 | 1 | 0 | 2 | Per Spec |
| 0 | 1 | 0 | Mode #1 | Normal | 1 | 0 | 0 | 0 | 0 | 0 | Per Spec |
| | | | | Tune Limit | 1 | 0 | 0 | 0 | 1 | 1 | Per Spec |
| | | | | LOR + LOL | 1 | 0 | 0 | 0 | 0 | 1 | Per Spec |
| 0 | 0 | 1 | Mode #2 | Normal | 0 | 1 | 0 | 0 | 0 | 0 | Per Spec |
| | | | | Tune Limit | 0 | 1 | 0 | 0 | 1 | 1 | Per Spec |
| | | | | LOR + LOL | 0 | 1 | 0 | 0 | 0 | 1 | Per Spec |
| 0 | 1 | 1 | Hold Over Mode | | 0 | 0 | 1 | 0 | 0 or 1 | 1 | Per Spec |
| 1 | X | X | Tri-State Mode | | High Impedence | | | | | | |

** See GR-1244-CORE, Issue 3 for Clock Out and Sync Out*

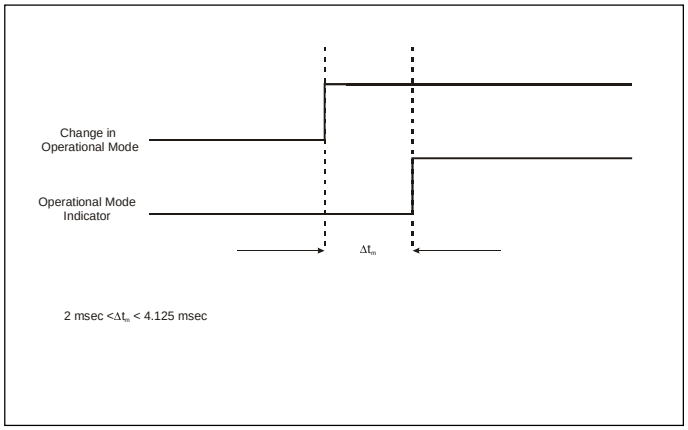
## Pin Description

Table 5

| Pin # | Pin Name | Pin Information |
|---|---|---|
| 1 | Hold Over | Mode indicator. When the STM is in holdover mode, Hold Over will be a logic high output. |
| 2 | Ref 1 | Mode indicator. When the STM is using External Reference #1, Ref 1 will be a logic high output. |
| 3 | Ref 2 | Mode indicator. When the STM is using External Reference #2, Ref 2 will be a logic high output. |
| 4 | Free Run | Mode indicator. When the STM is in free run mode, Free Run will be a logic high output. |
| 5 | GND | Ground. |
| 6 | N/C | No connection required |
| 7 | N/C | No connection required |
| 8 | Tri-State | Tri-State control for all outputs. 1=Hi-Z, 0=normal. |
| 9 | N/C | No connection required |
| 10 | Alarm Out | Alarm indicator output. |
| 11 | CNTL A | Mode control input. |
| 12 | CNTL B | Mode control input. |
| 13 | PLL TVL | Tuning Voltage Alarm. |
| 14 | GND | Ground. |
| 15 | Sync_Out | System clock output. |
| 16 | N/C | No connection required |
| 17 | GND | Ground. |
| 18 | Clock_Out | An independent Stratum 3 clock output with the required ±4.6 ppm. Can be used for general purpose clocking needs. |
| 19 | N/C | No connection required |
| 20 | GND | Ground. |
| 21 | Ex Ref 2 | External Reference #2 Input. |
| 22 | GND | Ground. |
| 23 | Ex Ref 1 | External Reference #1 Input. |
| 24 | +5 V DC | +5 Volt DC supply. (Vcc) |

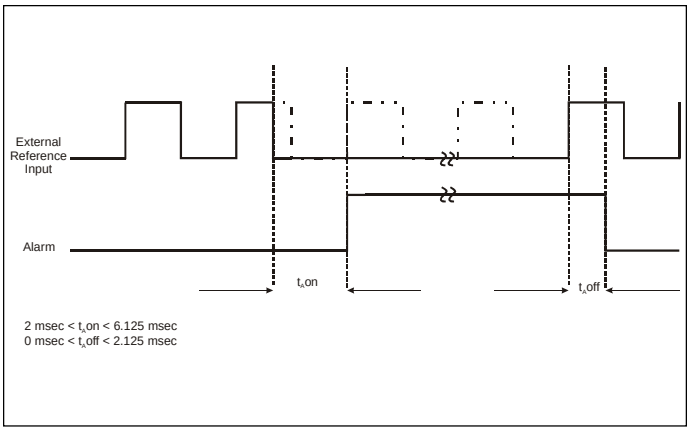
## Operational Mode Change Timing Diagram

Figure 5



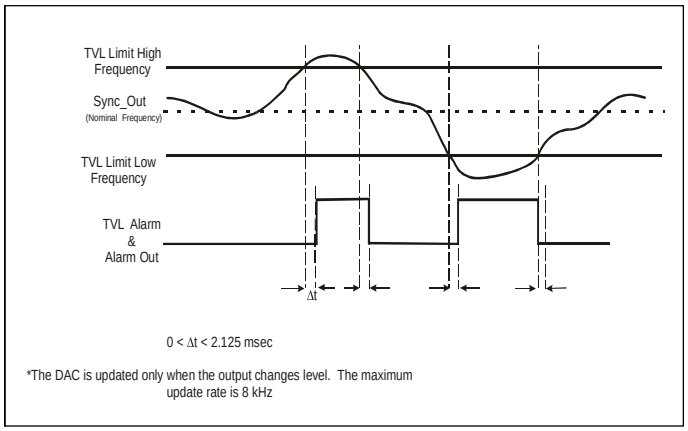

## Loss of Reference Timing Diagram

Figure 6



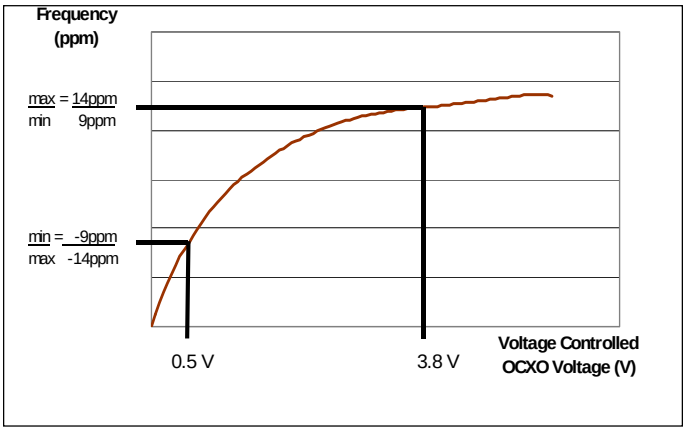

## TVL Alarm Timing Diagram

Figure 7



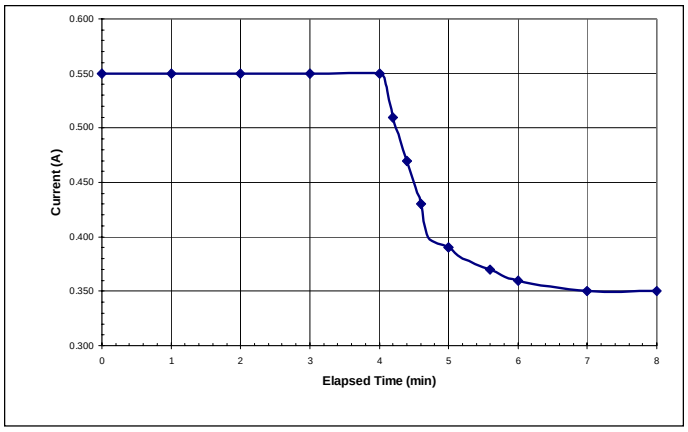

## TVL Alarm Range

Figure 8



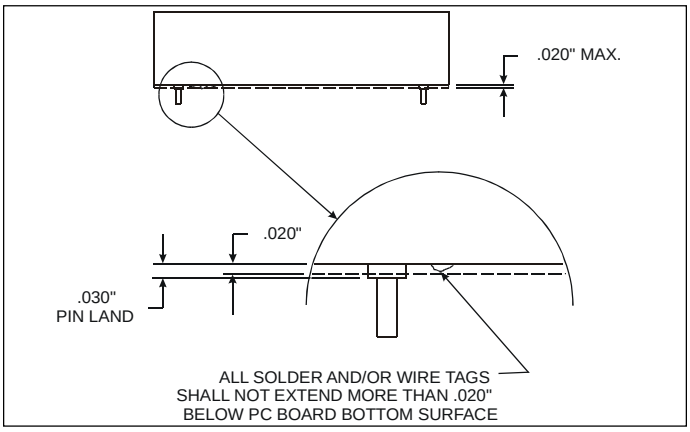

## Maximum Current Draw

Figure 9



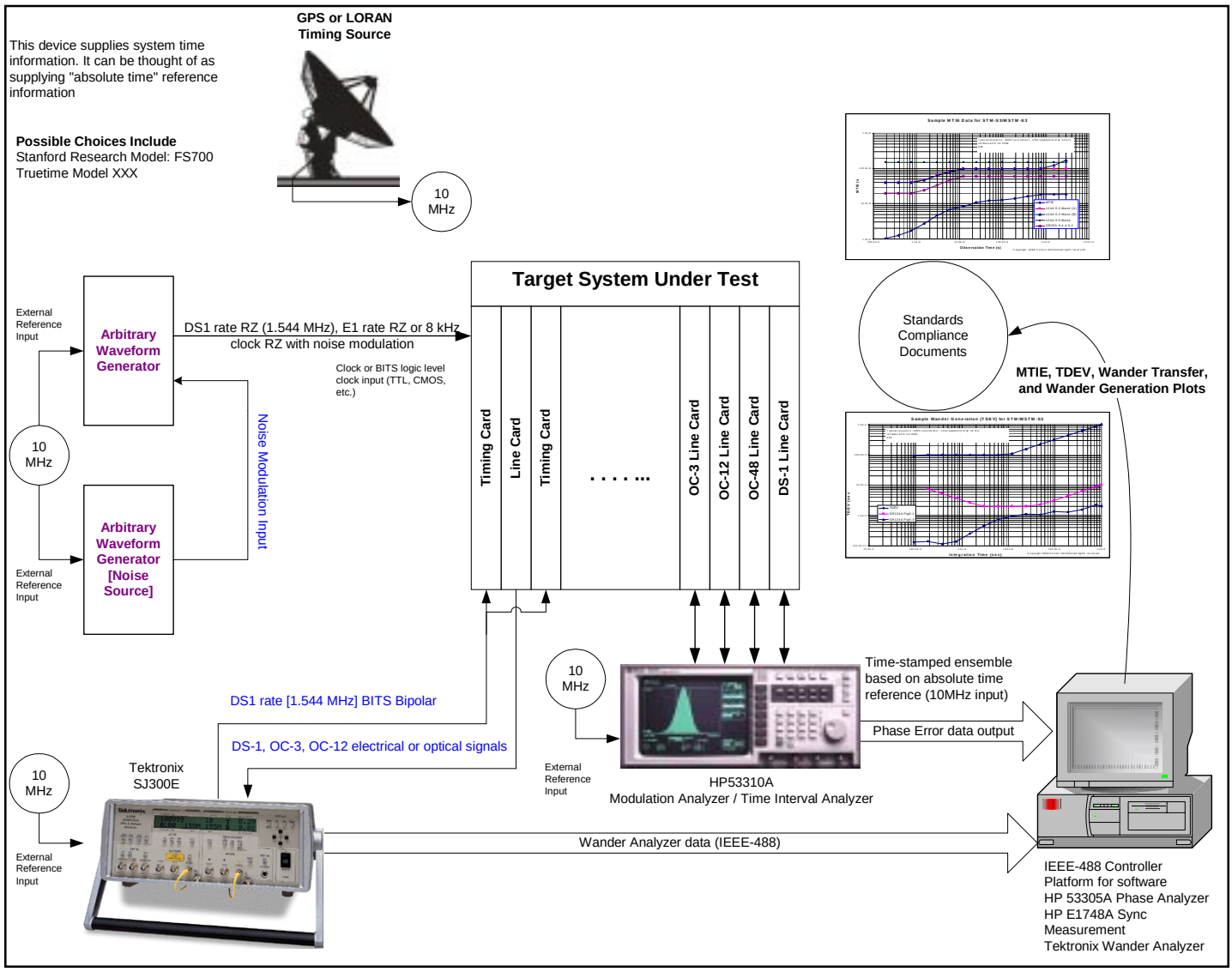

## Mounting Clearances

Figure 10



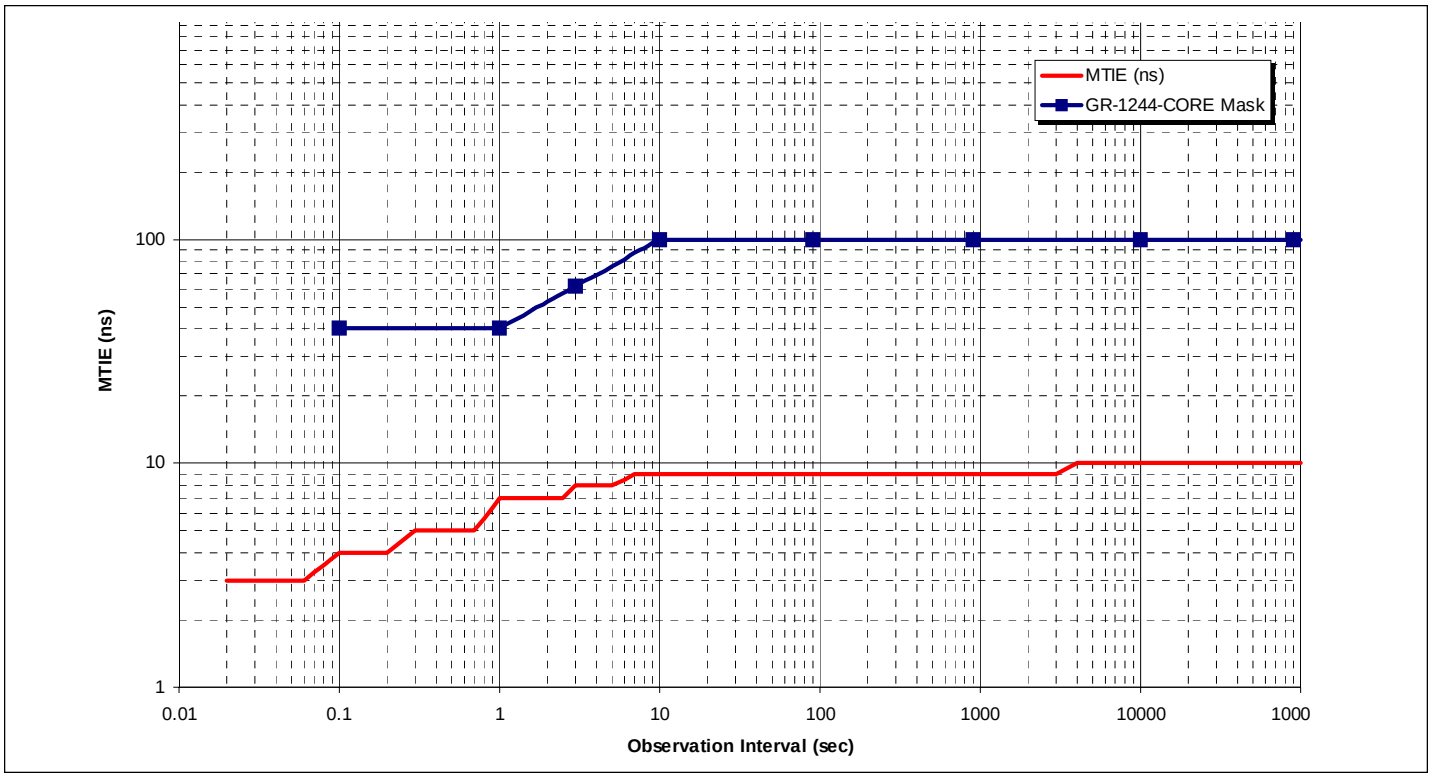
## Typical System Test Set-up

Figure 11



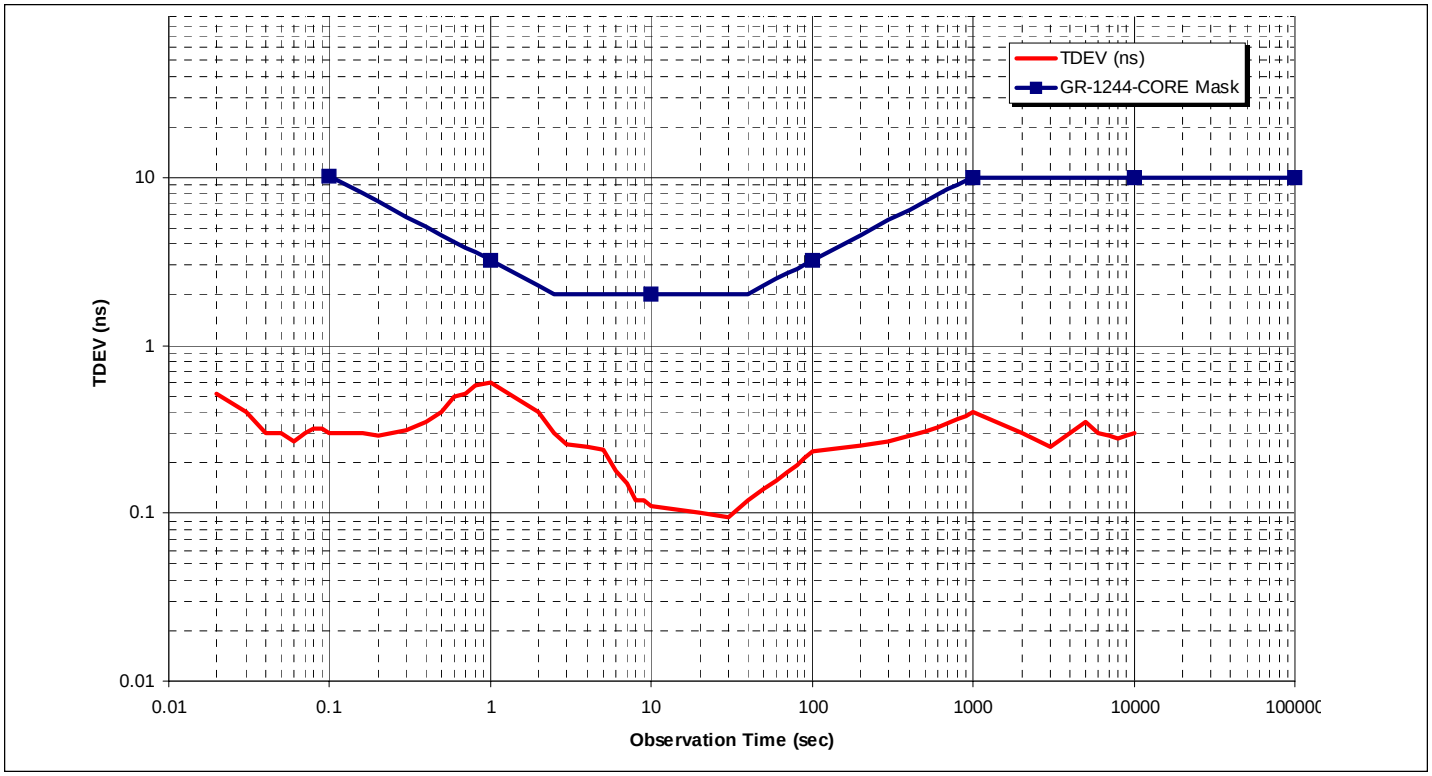
## Typical MTIE - Over Temperature with Noise

Figure 12



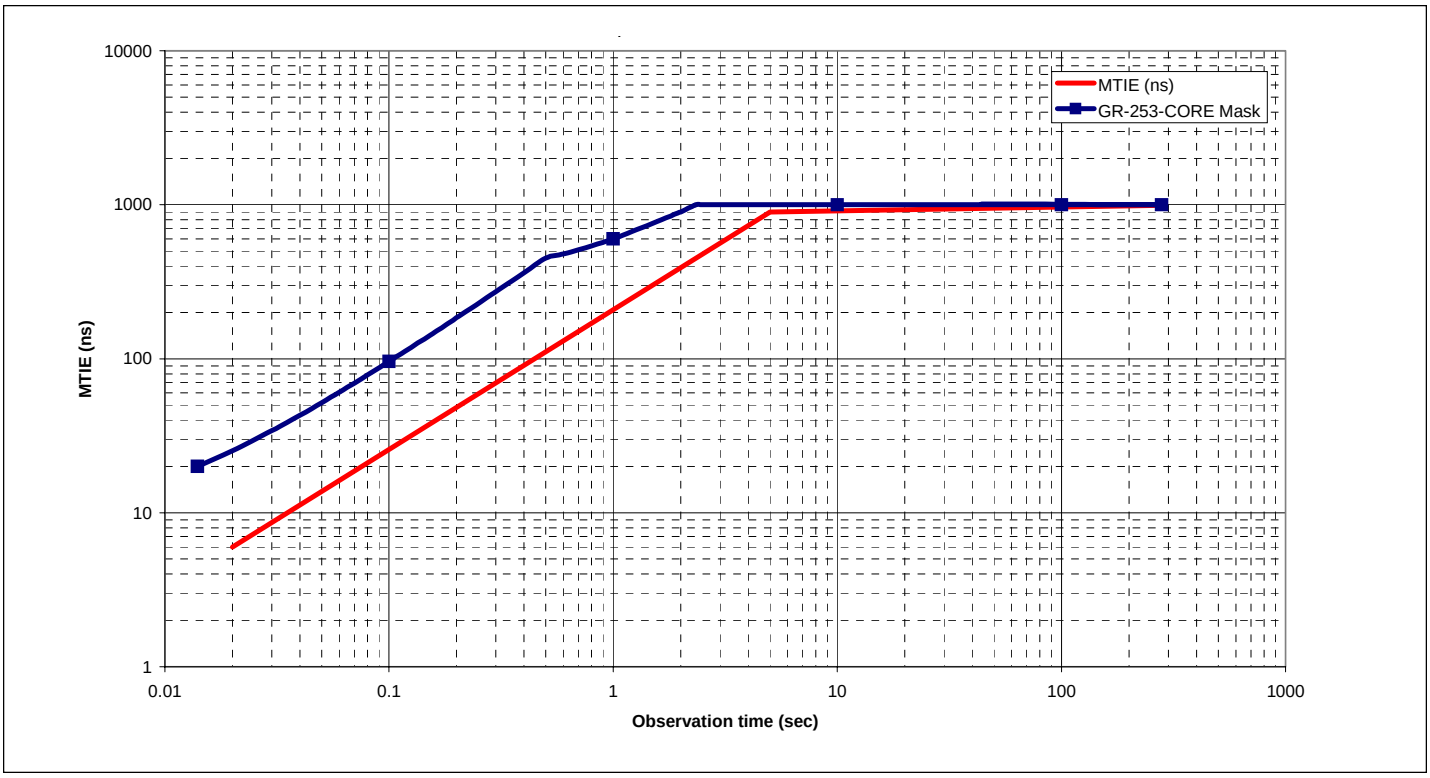

## Typical TDEV - Over Temperature with Noise

Figure 13



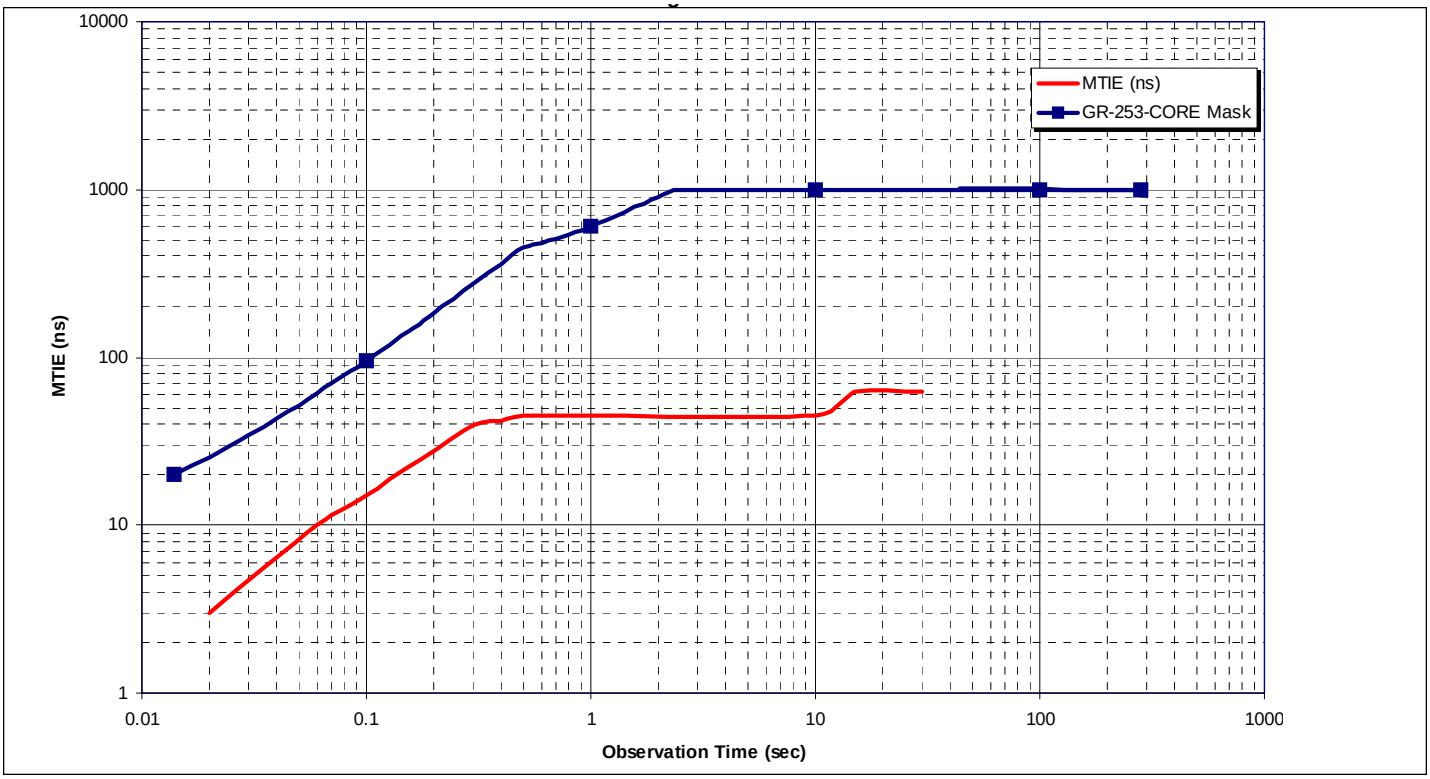
## 1 µs Phase Transient

Figure 14



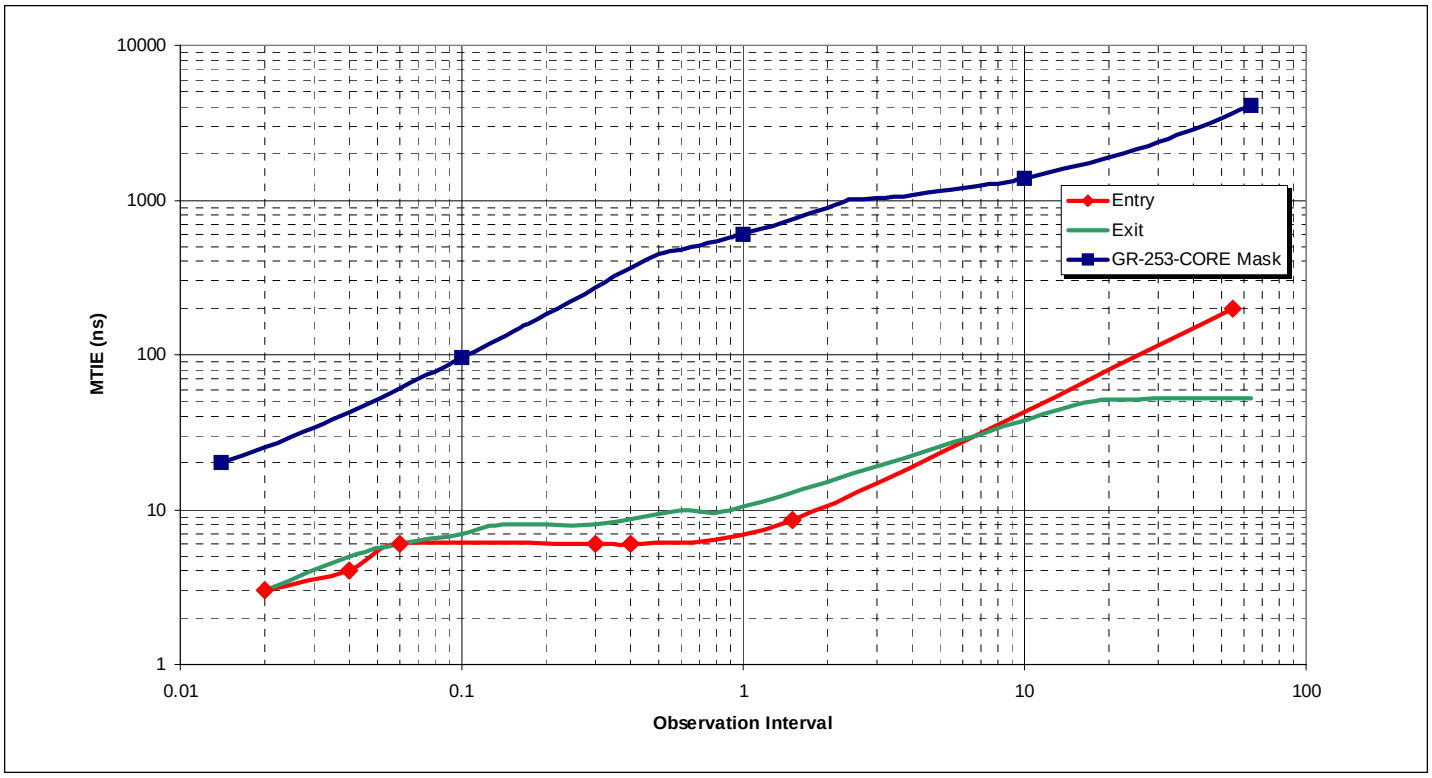

## Reference Switching Phase Transient

Figure 15



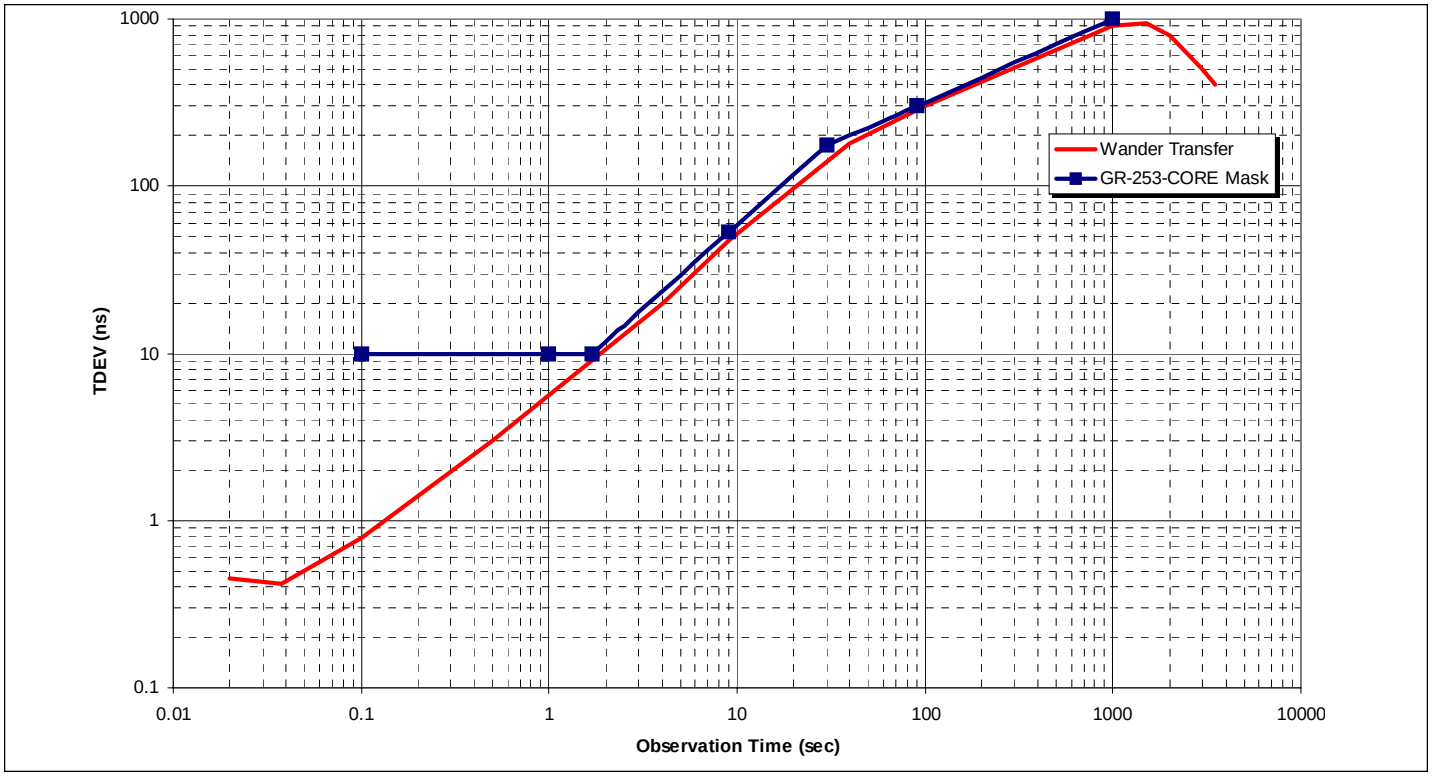
## Hold Over Entry and Exit with Same Reference

Figure 1




## Wander Transfer

Figure 17



NOTES:

1.0 Stresses beyond those listed under Absolute Maximum Rating may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those listed under Recommended Operating Conditions is not implied. Exposure ot Absolute Maximum Ratings conditions for extended periods of time may affect device reliability.

2.0 Power-on reset will be acivated within this level.

3.0 Nominal signal into a CMOS load is usually 3V or greater.

4.0 Hold Over stability is the cumulative fractional frequency offset containing Initial Offset, Temperature, and Drift components as described by Bellcore GR-1244-CORE 5.2.

5.0 Pull-in range is the maximum frequency deviation on the reference inputs to the timing module that can be overcome to pull itself into synchronization with the reference.

6.0 After 100 seconds at stable room temperature.

## Ordering Information:

STM-S3+ – 16.384 MHz

STM-S3+ – 19.44 MHz

STM-S3+ – 38.88 MHz

| REVISION | REVISION DATE | NOTE |
|---|---|---|
| P00 | 6/29/00 | Preliminary informational release |
| P01 | 2/05/00 | Changed Format |
| P02 | 2/27/01 | Minor Corrections |
| P03 | 6/27/01 | Reformatted Layout |