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SSI 32R1560R/61R
+5, -3V, 10-Channel MR Read/Write/Servo Write
Advance Information

October 1995

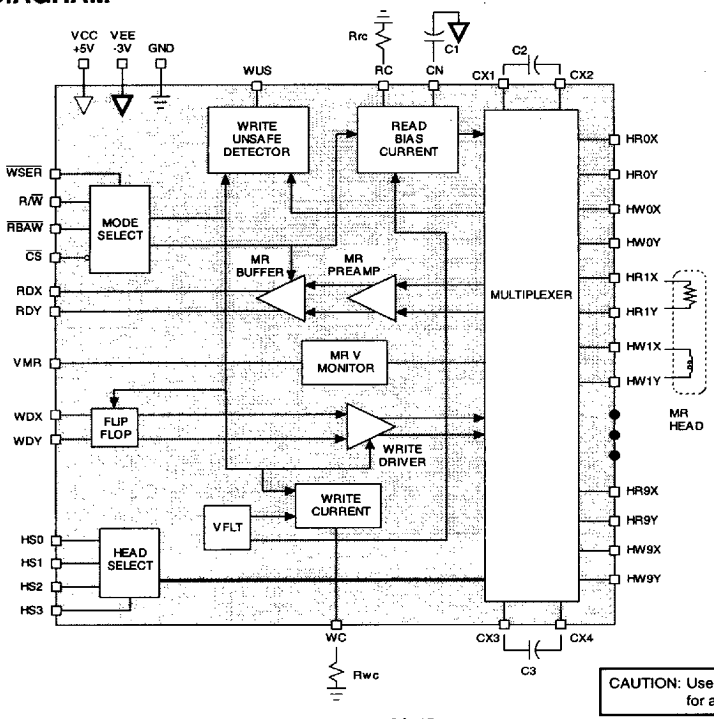
DESCRIPTION

The SSI 32R1560R/61R is a BiCMOS monolithic integrated circuit designed for use with four-terminal, Magneto-Resistive recording heads. It provides a write driver, MR read bias current, low noise read amplifier and fault detection circuitry for up to ten channels. In a write servo mode two banks of 5 write heads each can be separately selected. The device requires +5V and -3V power supplies, and comes in a 64-lead TQFP package.

FEATURES

- **+5V, -3V ±10% supply**
- **Designed for four-terminal MR heads with minimum external components**
- **Write unsafe detection**
- **Truly differential current bias/voltage sense MR read amp**
- **MR head bias current range = 6 to 16 mA**
- **MR read gain = 150 V/V**
- **MR read input noise = 0.75 nV/√Hz (Nom)**
- **MR read input resistance = 900Ω (Min)**
- **MR read input capacitance = 12 pF (Nom)**
- **No flip-flop bond option, 32R1561R**
- **Head voltage swing = 10 Vp-p (Nom)**
  Write current range = 10 to 40 mA
- **Max write current rise/fall time = 5 ns (Typ. head)**
- **Enhanced system write to read and read to write recovery time**
- **Power supply fault protection**
- **Servo write feature**

BLOCK DIAGRAM



CAUTION: Use handling procedures necessary for a static sensitive component.

FUNCTIONAL DESCRIPTION

CIRCUIT OPERATION

The SSI 32R1560R/61R addresses up to 10 four terminal MR heads providing write drive or read bias and amplification. The mode control and head selection are accomplished with TTL pins $\overline{CS}$, R/W, $\overline{RBAW}$, $\overline{WSER}$ and Hsn as shown in Tables 1, 2 and 3. All the TTL inputs have internal pull-up resistor so that when left opened, it will default to the TTL High state. Exception to this rule are head select inputs Hsn which have internal pull-down resistors and, consequently, will default to the TTL Low state.

TABLE 1: Head Selection

HS3	HS2	HS1	HS0	HEAD SELECTED
0	0	0	0	0
0	0	0	1	1
0	0	1	0	2
0	0	1	1	3
0	1	0	0	4
0	1	0	1	5
0	1	1	0	6
0	1	1	1	7
1	0	0	0	8
1	0	0	1	9

TABLE 2: Mode Selection

$\overline{CS}$	R/W	$\overline{WSER}$	$\overline{RBAW}$	DESCRIPTION
0	1	X	X	read mode only
0	0	1	1	write mode, MR bias current off
0	0	1	0	write mode, MR bias current on
0	0	0	1	Servo bank write
1	X	X	X	idle mode

TABLE 3: Servo Mode Head Selection

$\overline{CS}$	R/W	$\overline{WSER}$	HS0	DESCRIPTION
0	0	0	0	Heads 0, 1, 2, 3 and 4 are turned on for servo bank write
0	0	0	1	Heads 5, 6, 7, 8 and 9 are turned on for servo bank write

WRITE MODE

Taking both $\overline{CS}$ and R/W low selects write mode which configures the SSI 32R1560R/61R as a current switch and activates the Write Unsafe (WUS) detect circuitry. Head current is toggled between the X (HWnX) and Y (HWnY) side of the selected head on each Low to High transition of the differential PECL signal WDX-WDY. Changing from read or Idle mode to write mode initializes the write Data Flip-Flop to pass write current into the "X" pin, i. e., the Y side of the head will be higher potential then X side. For no flip-flop option (32R1561R) WDX > WDY will cause Iw to flow from Y to X. The write current is externally programmed either by a resistor Rwc connected from pin WC to GND or by a current sink from pin WC. The magnitude of the current (0-pk) is given by:

$$Iw = \frac{Aw \cdot Vwc}{Rwc} = \frac{Kwc}{Rwc}$$

where Aw is 20 mA/mA and Vwc is 2V.

Note that the actual head current Ix,y is given by:

$$I_{x,y} = \frac{Iw}{1 + Rh/Rd}$$

where Rh is the head DC resistance and Rd is the damping resistance.

SERVO WRITE MODE

Taking $\overline{CS}$, RW and $\overline{WSER}$ low enables write servo mode. In this mode five write heads comprising one servo bank are simultaneously activated. Write servo banks are selected by HS0 line according to Table 3.

WRITE UNSAFE

Any of the following conditions will be indicated as a high level on the Write Unsafe (WUS) open collector output:

- WDX/WDY frequency too low
- Device in read mode
- No head current
- Head open

Upon entering write mode, WUS is valid after two Low to High transitions of WDX - WDY following the required Read-Write transition time (0.5 µs max).

READ MODE

Taking $\overline{CS}$ low and R/W high selects read mode which activates the MR bias current generator and low noise differential amplifier. The outputs of the read amplifier RDX and RDY are emitter followers and are in phase with the resistivity change at the selected input ports HRnX and HRnY where the respective MR head is attached. The DC current necessary for biasing the MR sensor is externally programmed either by a resistor Rrc connected from pin RC to GND or by a current sink. The magnitude of the bias current is given by:

$$Ir = \frac{Ar \cdot Vrc}{Rrc} = \frac{Krc}{Rrc}$$

where Ar is 20 mA/mA and Vrc is 2.0V.

An external capacitor connected from pin CN to VEE is used for reducing the noise from MR bias current source. A low inductance capacitor with a value of 0.1 µF is recommended. Two external floating capacitors C2 and C3 connected between pins CX1/CX2 and CX3/CX4 respectively are required for DC blocking. For the application that uses up to five MR heads, i. e., head 0 to head 4, only one floating capacitor connected between pins CX1 and CX2 is required. Care should be taken to use low inductance high frequency capacitors and to locate them as close to the pins as possible — because the stray inductance will degrade the amplifier's noise and frequency response performance. The value of the DC blocking capacitors CX2/CX3 will have direct effect on the write to read recovery time. For fast recovery time, the capacitor value should be kept as small as possible. The value of the capacitor CX2/CX3 also sets the low frequency cutoff of the read amplifier. The -3 dB low-frequency corner is given by:

$$f_L = 1/(2\pi \cdot 15\Omega \cdot C2)$$

For example, a 0.1 µF capacitor for C2/C3 will result in the -3 dB low-frequency of about 106 kHz.

The voltage drop across the MR head is monitored internally. The VMR pin provides a monitor voltage referenced to ground of the MR head bias voltage. The maximum output current of the VMR pin should not exceed 1 mA.

To further improve the write to read recovery time, the MR bias current in the selected head can be left on

READ MODE (continued)

during write mode by taking $\overline{\text{RBAW}}$ pin low. With the MR bias current turned on, the voltage change across the DC blocking capacitor C2/C3 between write and read modes will be minimized which would then result in faster write to read recovery time. For the best trade-off between power dissipation and write to read recovery time, the MR bias current does not have to be on for the whole write period. A turn on period in the range of tens of microseconds prior to the write to read transition usually would be sufficient. In read mode, the voltage at the midpoint of the selected MR head is forced to the ground potential. For the unselected MR heads, the head ports become high impedance and thus will prevent the heads from conducting current in the event of head to disk contact.

IDLE MODE

Taking $\overline{\text{CS}}$ high selects Idle mode which deactivates both the write current source and MR bias current. The voltages at RC pin remain active so that an internal dummy head can be switched on to provide proper voltage biasing for the DC blocking capacitor C2/C3. The pins RDX/RDY are switched into high impedance state to facilitate multiple device applications where these pins could be wire OR'ed.

POWER SUPPLY FAULT PROTECTION

A voltage fault detection circuit improves data security by disabling the write current generator and MR bias current during a voltage fault or power startup regardless of mode.

PIN DESCRIPTION

NAME	TYPE	DESCRIPTION
HRnX	I	MR read head input X connection
HRnY	I	MR read head input Y connection
HWnX	O	Inductive write head X connection
HWnY	O	Inductive write head Y connection
CN	I	Noise filter Cap C1; X side, Y side of C1 must be connected to VEE
CX1, CX2	I	Floating DC blocking cap C2; for head 0 to head 4
CX3, CX4	I	Floating DC blocking cap C3: for head 5 to head 9
WDX, WDY	I	Differential PECL write Data Input, a positive transition of (WDX-WDY) toggles the direction of the head current
RDX, RDY	O	Differential MR head read Data Output
WC	I	Write Current set: used to set the magnitude of the write current
RC	I	Read Current set; used to set the magnitude of the MR bias current
WUS	O	Write Unsafe; open collector; a high level indicates an unsafe writing condition
HS0, HS1, HS2, HS3	I	Head Select; select one of ten heads; TTL
$\overline{\text{CS}}$	I	Chip Select; a high inhibits the chip; TTL
R/W	I	Read/Write; a high selects read mode, TTL
$\overline{\text{WSER}}$	I	Write servo; a low enables write in servo mode; TTL
$\overline{\text{RBAW}}$	I	A low level activates the MR bias current in write mode; TTL
VMR	O	MR head DC voltage drop monitor, referenced to ground

PIN DESCRIPTION (continued)

NAME	TYPE	DESCRIPTION
VCC	I	+5V Supply
VEE	I	-3V Supply
GND	I	Ground

ELECTRICAL SPECIFICATIONS

ABSOLUTE MAXIMUM RATINGS

Operation above maximum ratings may result in permanent damage to the device.

PARAMETER		RATING
DC Supply Voltage	VCC	+6 VDC
	VEE	-3.6 VDC
Logic Input Voltage	TTL	-0.3 to VCC + 0.3 VDC
	PECL	0 to VCC VDC
Write Current	Iw	50 mA
MR Bias Current	Ir	30 mA
Output Current	WUS	+8 mA
	RDX/RDY	-5 mA
Operating Junction Temperature	Tj	+125°C
Storage Temperature	Tstg	-65 to +150°C

RECOMMENDED OPERATING CONDITIONS

PARAMETER		RATING
DC Supply Voltage	VCC	+5V, ±10%
	VEE	-3V, ±10%
Operating Ambient Temperature	Ta	0 to 70°C

DC CHARACTERISTICS

Recommended operating conditions apply unless otherwise specified. Ir = 16 mA, Iw = 40 mA

PARAMETER	CONDITION	MIN	NOM	MAX	UNIT
VCC Supply Current	read mode		44 + 1.15 Ir		mA
	write mode, $\overline{RBAW}$ = High		36.1 + 1.2 Iw		mA
	write mode, $\overline{RBAW}$ = Low		50.6 + 1.2 Iw		mA
	servo mode		80.3 + 5.8 Iw		mA
	idle mode		14		mA
VEE Supply Current	read mode		22.9 + 1.1 Ir		mA
	write mode, $\overline{RBAW}$ = High		25.2 + 1.2 Iw		mA
	write mode, $\overline{RBAW}$ = Low		39.9 + 1.2 Iw		mA
	servo mode		64.7 + 6.05 Iw		mA
	idle mode		9		mA
Power Dissipation	read mode		432		mW
	write mode, $\overline{RBAW}$ = High		640		mW
	write mode, $\overline{RBAW}$ = Low		757		mW
	servo mode, Iw = 10 mA		1036		mW
	idle mode		98		mW
VCC Fault Voltage	Iw < 0.2 mA, Ir < 0.2 mA	3.5	3.85	4.2	VDC
VEE Fault Voltage	Iw < 0.2 mA, Ir < 0.2 mA	-2.52	-2.31	-2.10	VDC

DIGITAL INPUTS AND OUTPUTS

Input Low Voltage	VIL	TTL			0.8	V
Input High Voltage	VIH	TTL	2			V
Input Low Current	LIL	Vil = 0.8V	-0.4	-0.2		mA
Input High Current	LIH	Vih = 2V			100	µA
Input Low Voltage	VIL2	WDX, WDY	Vcc -2.2		VIHZ -0.3	V
Input High Voltage	VIH2	WDX, WDY	Vcc -1.08		Vcc - 0.5	V
Input Differential Voltage		V(WDX) - V(WDY)	0.3			V
Input Low Current	LIL2	Vil2 = Vcc - 1.25V			50	µA
Input High Current	LIH2	Vih2 = Vcc - 0.75V			50	µA
Output High Current	LOH	WUS			50	mA
Output Low Current	LOL	WUS			4.0	mA
Output Low Voltage	VOL	WUS, Iol = 4 mA			0.5	V
Input Low Current	LIL3	TTL, HSn inputs	-100			µA
Input High Current	LIH3	TTL, HSn inputs			0.4	mA

READ CHARACTERISTICS, MR HEAD AMPLIFIER
Recommended operating conditions apply unless otherwise specified.
Rmr = 23Ω; Rrc = 3.64K; Rwc = 1.33K
CL (RDX, RDY) < 20 pFRL (RDX, RDY) > 1K

PARAMETER	CONDITION	MIN	NOM	MAX	UNIT
MR Head Resistance		10	23	32	Ω
MR Current Range		6	11	16	mA
MR Current Gain AR	read mode		20		mA/mA
	idle mode			0.01	mA/mA
MR Current Setting Voltage VRC	all modes		2		V
"Kr" Factor	Kr = Ar • Vrc	36	40	44	V
MR Head Potential	selected head	-250		250	mV
	unselected heads	-1.0		-0.3	V
Unselected MR Current				0.1	mA
Differential Voltage Gain	Vin = 1 mVp-p @ 5 MHz	125	150	180	V/V
Voltage BW -1 dB	Rmr = 23Ω Lmr = 20 nH	40			MHz
-3 dB	Vin = 1 mVp-p	60			MHz
Input Noise Voltage	exclude head noise		0.75		nV/√Hz
Differential Input Resistance	Vin = 1 mVp-p @ 5 MHz C2 = C3 = 0.1 µF	900			Ω
Differential Input Capacitance	Vin = 1 mVp-p @ 5 MHz C2 = C3 = 0.1 µF		12		pF
Input Dynamic Range	AC input voltage where gain falls to 90% of its small signal value, @ 5 MHz	8			mVp-p
CMRR	Vin = 100 mVp-p @ 5 MHz	45			dB
PSRR	100 mVp-p @ 5 MHz on VCC or VEE	45			dB
Channel Separation	unselected channels driven with 100 mVp-p @ 5 MHz	45			dB
Output Offset Voltage		-100		100	mV
MR Head Voltage Monitor VMR			264		mV
Output Resistance	singled-ended		35	70	Ω
Output Current		1.5	2.2		mA
RDX/RDY Common Mode Output Voltage			Vcc - 1.65		V
RDX/RDY High Imp Leakage			200		µA

WRITE CHARACTERISTICS
Recommended operating conditions apply unless otherwise specified.
Iw = 30 mA, Lh = 220 nH, Rh = 25Ω

PARAMETER	CONDITION	MIN	NOM	MAX	UNIT
Write Current Range		10		40	mA
Write Current Gain Aw	write mode		20		mA/mA
Write Current Setting Voltage Vwc	write mode		2		V
"Kw" Factor	Kw = Aw • Vwc	36	40	44	V
Differential Head Voltage Swing	open head		10		Vp-p
Unselected Head Current	DC			0.1	mA
	AC			1	mApk
Head Differential Damping Resistance Rd		360	450	540	Ω
Head Differential Load Capacitance				15	pF

SWITCHING CHARACTERISTICS
Recommended operating conditions apply unless otherwise specified.
Rmr = 23Ω, 10% variation; Rrc = 3.64K; Rwc = 1.33K; CL (RDX, RDY) < 20 pF;
RL (RDX, RDY) > 1K; Lh = 220 nH, Rh = 25Ω; F (WDX/WDY) = 5 MHz

R/W	Read to Write	to 90% of write current			100	ns
	Write to Read	to 90% of 100 mV 5 MHz read signal envelope; $\overline{RBAW}$ = 0			2	µs
$\overline{CS}$	Idle to Read	to 90% of 100 mV 5 MHz read signal envelope			5	µs
HSO, 1, 2, 3	to any MR	to 90% of 100 mV 5 MHz read signal envelope			5	µs
WUS	Safe to Unsafe TD1	write mode, from loss of WDX/WDY transition		0.7	1.4	µs
	Unsafe to Safe TD2	fault cleared, from first positive (WDX-WDY) transition			0.5	µs
Head Current	Propagation Delay TD3	50% (WDX - WDY) to 50% (Ix - Iy)	6		20	ns
	Rise/Fall Time	Iw = 30 mA, Lh = 220 nH, Rh = 25Ω 10% to 90% points		2.7	5	ns
		Iw = 30 mA, Lh = 0, Rh = 0		1.1		ns
Write Current Asymmetry		propagation delay difference			0.5	ns

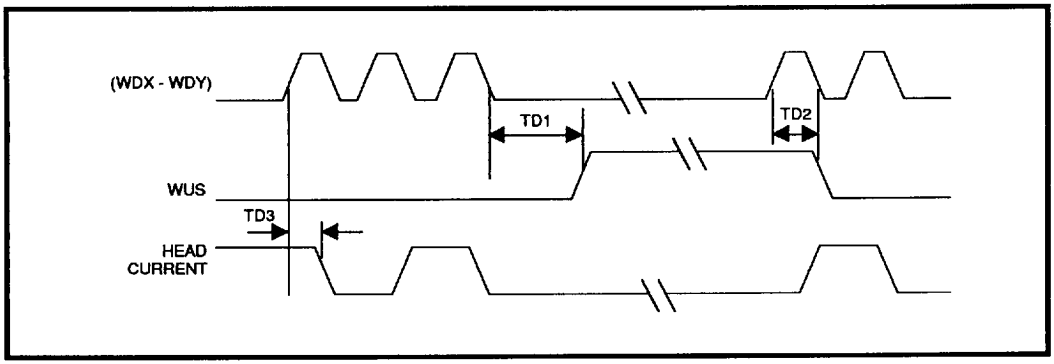


FIGURE 1: 32R1560R Write Mode Timing

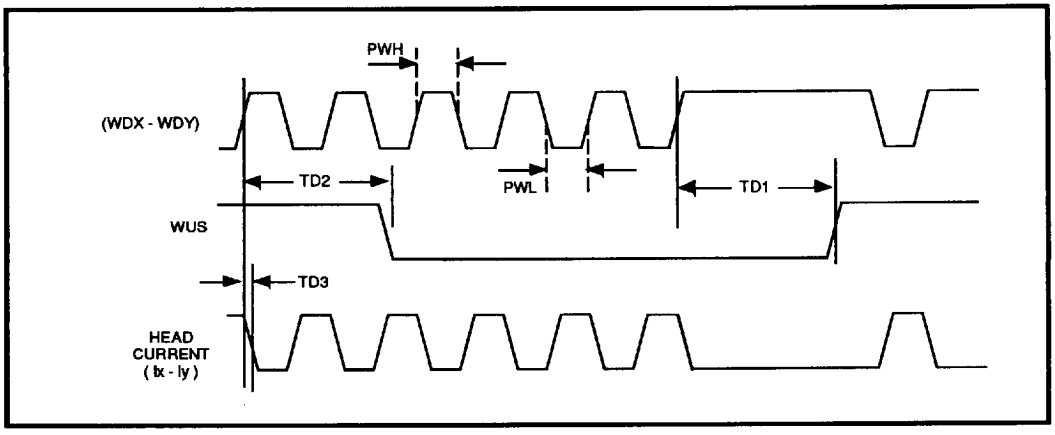
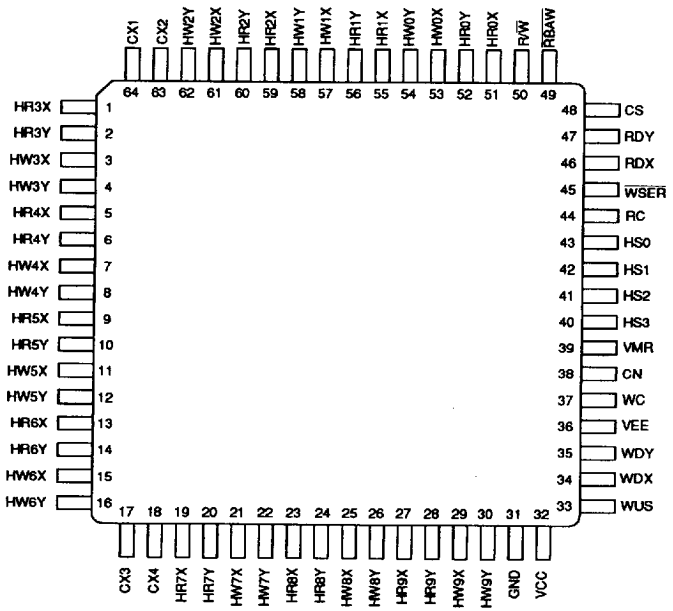


FIGURE 2: 32R1561R Write Mode Timing

SSI 32R1560R/61R
+5, -3V, 10-Channel
MR Read/Write/Servo Write

PACKAGE PIN DESIGNATIONS
(Top View)



64-Lead TQFP

CAUTION: Use handling procedures necessary for a static sensitive component.

Advance Information: Indicates a product still in the design cycle, and any specifications are based on design goals only. Do not use for final design.

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