1 PRODUCT OVERVIEW

SAM87RC PRODUCT FAMILY

Samsung's new SAM87RC family of 8-bit single-chip CMOS microcontrollers offers a fast and efficient CPU, a wide range of integrated peripherals, and various mask-programmable ROM sizes.

Timer/counters with selectable operating modes are included to support real-time operations. Many SAM87RC microcontrollers have an external interface that provides access to external memory and other peripheral devices.

A sophisticated interrupt structure recognizes up to eight interrupt levels. Each level can have one or more interrupt sources and vectors. Fast interrupt processing (within a minimum six CPU clocks) can be assigned to one interrupt level at a time.

S3C8478/C8475 MICROCONTROLLER

The S3C8478/C8475 single-chip 8-bit microcontroller is designed for useful 10-bit resolution A/D converter, UART, PWM application field. Its powerful SAM87RC CPU architecture includes. The internal register file is logically expanded to increase the on-chip register space.

The S3C8478/C8475 has 8/16K bytes of on-chip program ROM. Following Samsung's modular design approach, the following peripherals are integrated with the SAM87RC core:

— Large number of programmable I/O ports (42 SDIP: 34 pins, 44 QFP: 36 pins)
— One asynchronous UART module
— Analog-to-digital converter with eight input channels and 10-bit resolution
— One 8-bit basic timer for watchdog function
— One 8-bit timer/counter with three operating modes (Timer 0)
— One general-purpose 16-bit timer/counters with three operating modes (Timer 1)

The S3C8478/C8475 is a versatile general-purpose microcontroller that is ideal for use in a wide range of electronics applications requiring complex timer/counter, PWM, capture, and UART.
It is available in a 42-pin SDIP or 44-pin QFP package.

OTP

The S3C8475 is an OTP (One Time Programmable) version of the S3C8478/C8475 microcontroller. The S3C8475 microcontroller has an on-chip 16K-byte one-time-programmable EPROM instead of a masked ROM. The S3C8475 is comparable to the S3C8478/C8475, both in function in D.C. electrical characteristics and in pin configuration.

FEATURES

CPU

- SAM87RC CPU core

Memory

- 272-byte general purpose register area
- 8/16K-byte internal program memory

Instruction Set

- 79 instructions
- IDLE and STOP instructions added for power-down modes

Instruction Execution Time

- 333 ns at 12 MHz f_{OSC} (minimum)

Interrupts

- 14 interrupt sources and 14 vectors
- Eight interrupt levels
- Fast interrupt processing

General I/O

- Five I/O ports (total 36 pins)
- Four bit-programmable ports
- Two n-channel open-drain output port

Timer/Counters

- One 8-bit basic timer for watchdog function
- One 8-bit timer/counter with three operating modes (timer 0)
- One 16-bit general-purpose timer/counters with three operation modes (timer 1)

UART

- One UART module
- Full duplex serial I/O interface with three UART modes

A/D Converter

- Eight analog input pins
- 10-bit conversion resolution
- 20 µs conversion time (10 MHz CPU clock)

Buzzer Frequency Output

- 200 Hz to 20 kHz signal can be generated

Oscillator Frequency

- 1 MHz to 12 MHz external crystal oscillator
- Maximum 12 MHz CPU clock

Operating Temperature Range

- – 40°C to + 85°C

Operating Voltage Range

- 1.8 V to 5.5 V

Package Types

- 42-pin SDIP, 44-pin QFP

BLOCK DIAGRAM

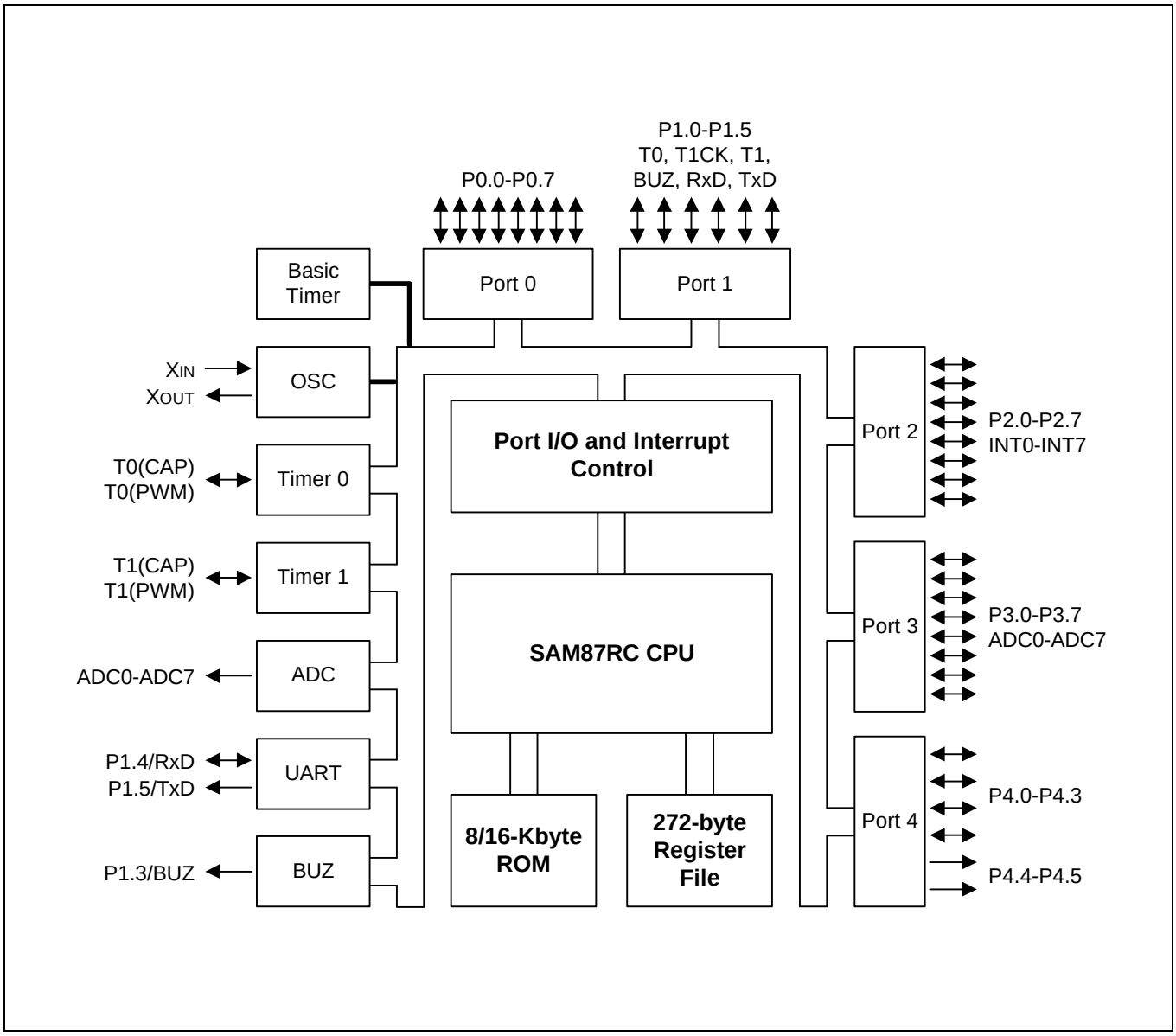


Figure 1-1. Block Diagram

PIN ASSIGNMENTS

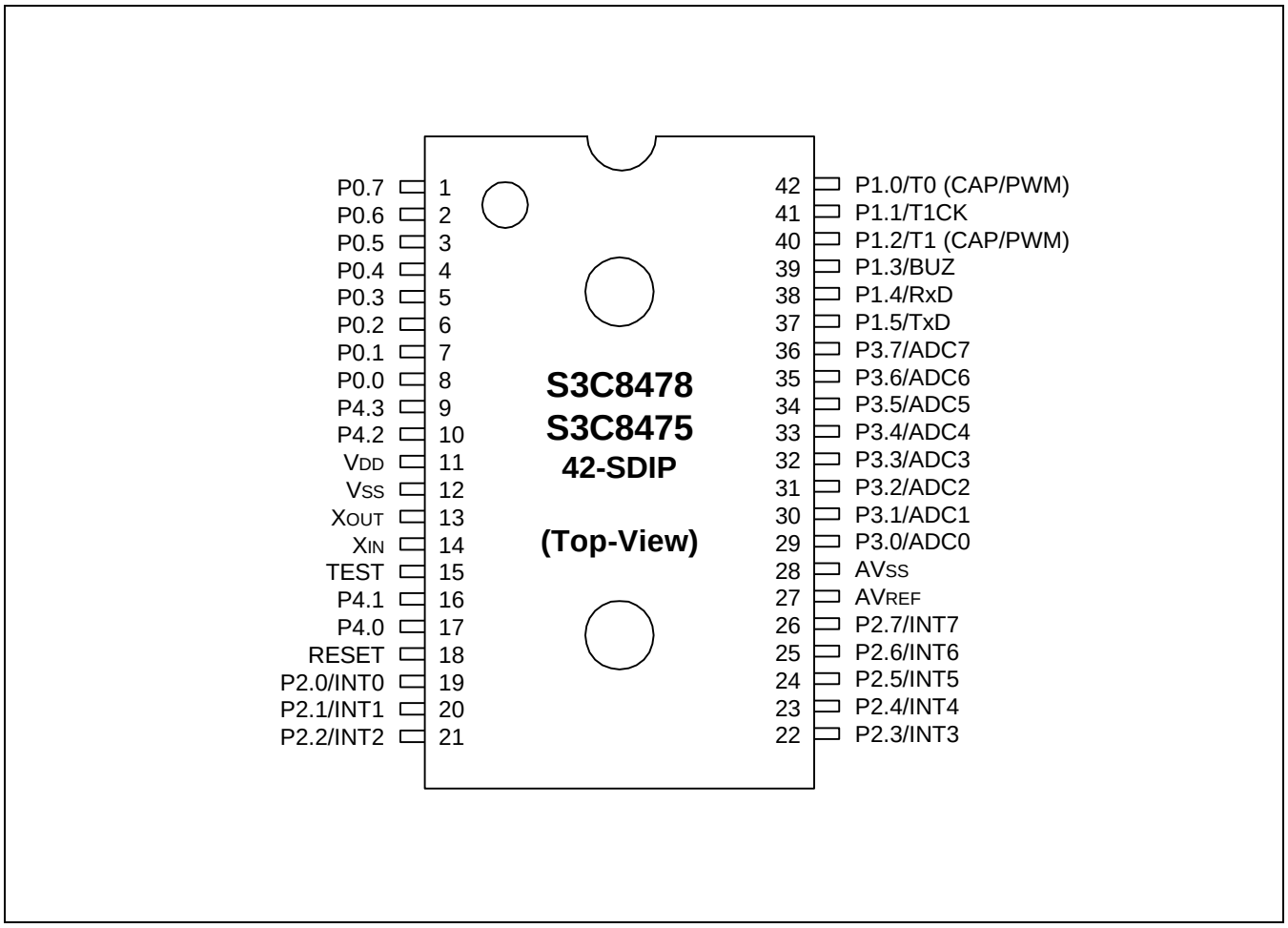


Figure 1-2. Pin Assignment Diagram (42-Pin SDIP Package)

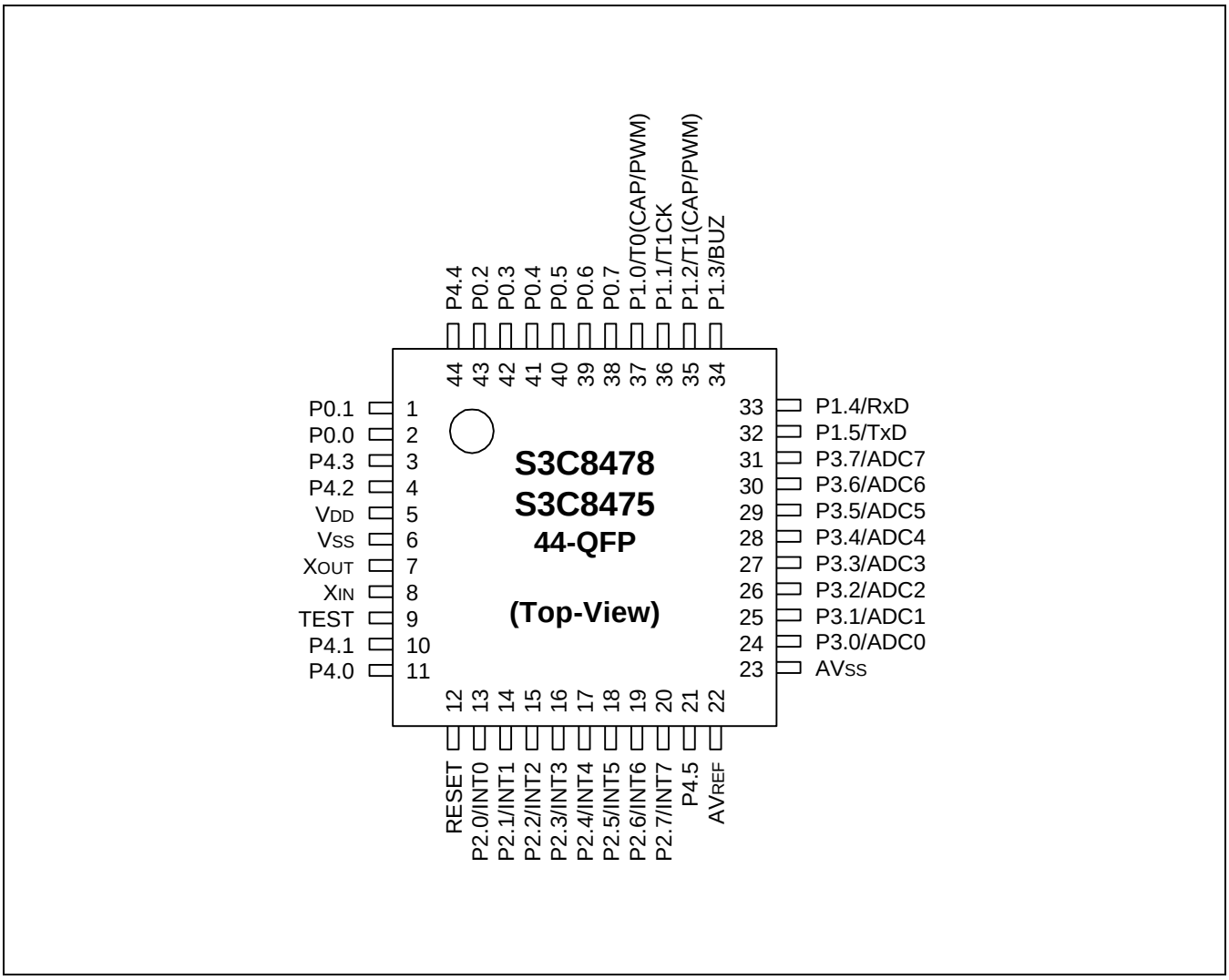


Figure 1-3. Pin Assignment Diagram (44-Pin QFP Package)

Table 1-1. S3C8478/C8475 Pin Descriptions

Pin Name	Pin Type	Pin Description	Circuit Number	Pin Number	Share Pins
P0.0–P0.7	I/O	Nibble-programmable I/O port for Schmitt trigger input or push-pull, open-drain output. Pull-up resistors are assignable by software.	E	8-1 (2-1, 43-38)	–
P1.0–P1.5	I/O	Bit-programmable I/O port for Schmitt trigger input or push-pull output. Pull-up resistors are assignable by software. Port 1 pin can also by used as alternative function (T0, T1CK, T1, BUZ, RxD, TxD)	D	42-37 (37-32)	T0, T1CK, T1, BUZ, RxD, TxD
P2.0–P2.7	I/O	Bit-programmable I/O port for Schmitt trigger input or push-pull output. Pull-up resistors are assignable by software. Port 2 pins can also be used as external interrupt.	D	19-26 (13-20)	INT0-INT7
P3.0–P3.7	I/O	Bit-programmable I/O port for Schmitt trigger input or push-pull output. Pull-up resistors are assignable by software. Port 3 pins can also be used as A/D converter by software.	F	29-36 (24-31)	ADC0-ADC7
P4.0–P4.3	I/O	Bit-programmable I/O port for Schmitt trigger input or push-pull, open-drain output. Pull-up resistors are assingable by software.	E	17-16, 10-9 (11-10, 4-3)	–
P4.4–P4.5	O	Push-pull output only	C	(44, 21)	–
X_{IN}, X_{OUT}	–	Crystal or ceramic oscillator signal for system clock.	–	14, 13 (8, 7)	–
RESET	I	System reset signal input pin.	B	18 (12)	–
TEST	I	Test signal input pin (for factory use only; muse be connected to V_{SS})	–	15 (9)	–
AV_{REF}, AV_{SS}	–	A/D converter reference voltage input and ground	–	27, 28 (22, 23)	–
V_{DD}, V_{SS}	–	Voltage input pin and ground	–	11, 12 (5, 6)	–
T0	I/O	Timer 0 capture input or PWM output pin	D	42 (37)	P1.0
T1CK	I	Timer 1 external clock input pin	D	41 (36)	P1.1
T1	I/O	Timer 1 capture input or PWM output pin	D	40 (35)	P1.2
BUZ	O	200Hz-20kHz frequency output for buzzer sound	D	39 (34)	P1.3
RxD	I/O	UART receive and transmit input or output	D	38 (33)	P1.4
TxD	O	UART transmit output	D	37 (32)	P1.5
INT0-INT7	I	External interrupt input	E	19-26 (13-20)	P2.0-P2.7
ADC0-ADC7	I	A/D converter input	F	29-36 (24-31)	P3.0-P3.7

NOTE: Pin numbers shown in parentheses "( )" are for the 44-pin QFP package.

PIN CIRCUIT DIAGRAMS

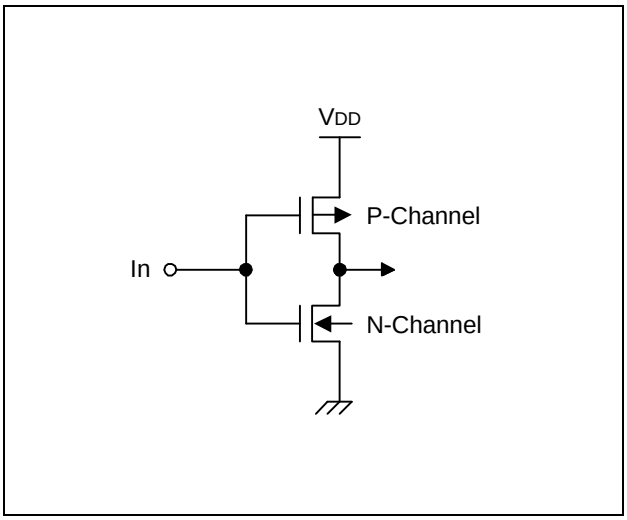


Figure 1-4. Pin Circuit Type A

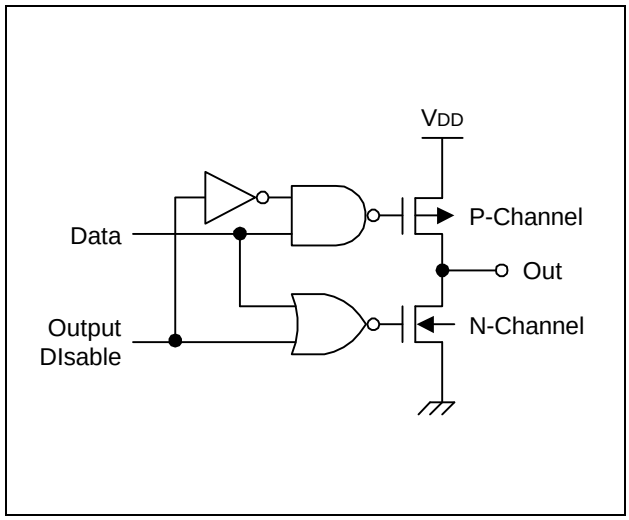


Figure 1-6. Pin Circuit Type C

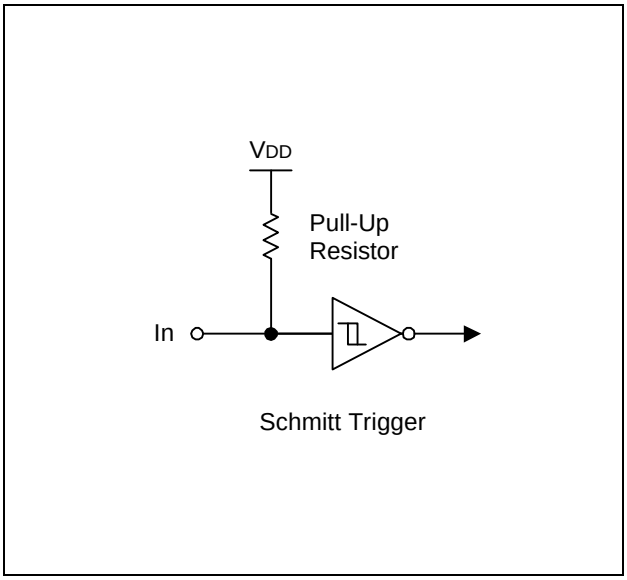


Figure 1-5. Pin Circuit Type B

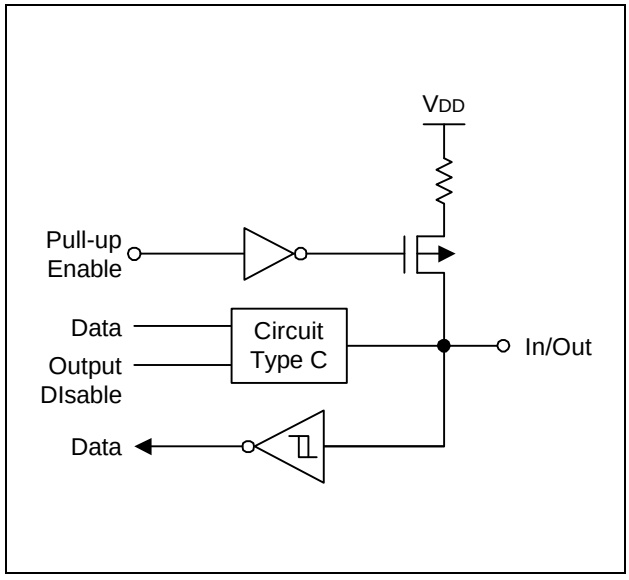


Figure 1-7. Pin Circuit Type D

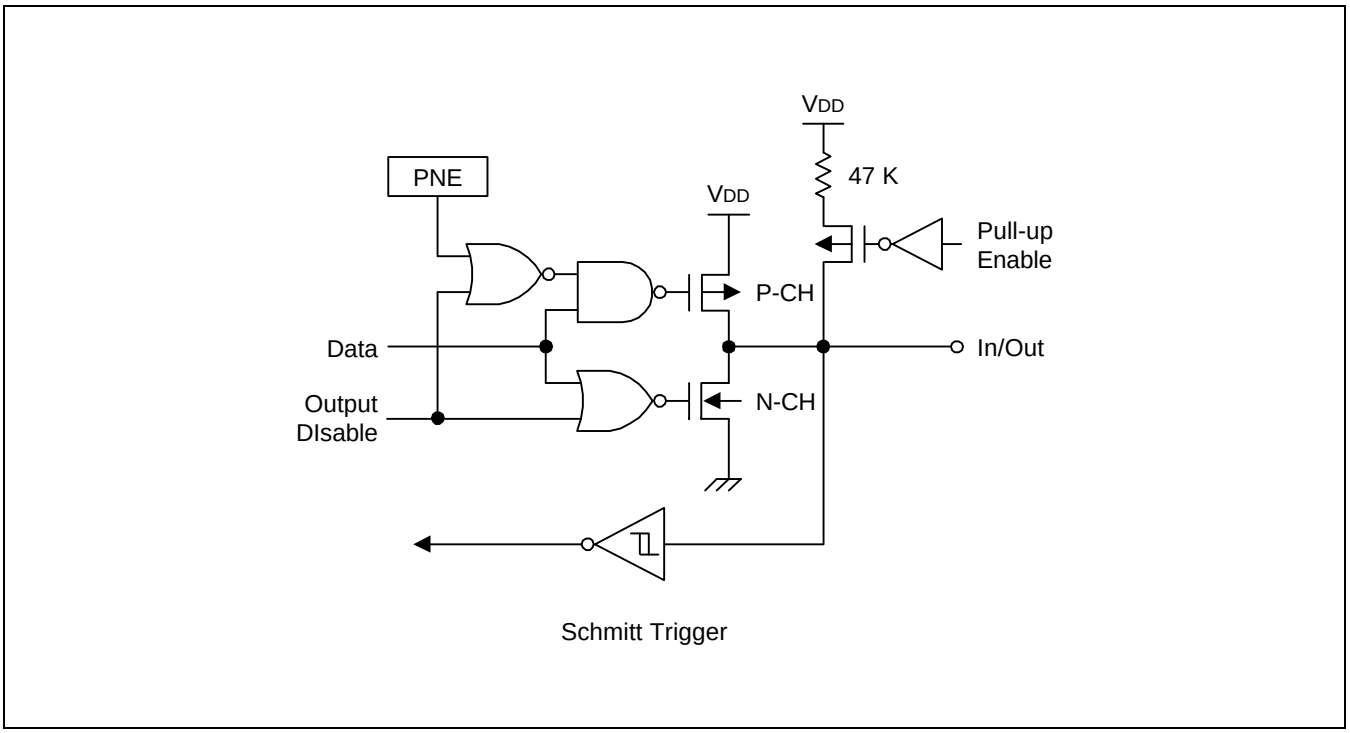


Figure 1-8. Pin Circuit Type E

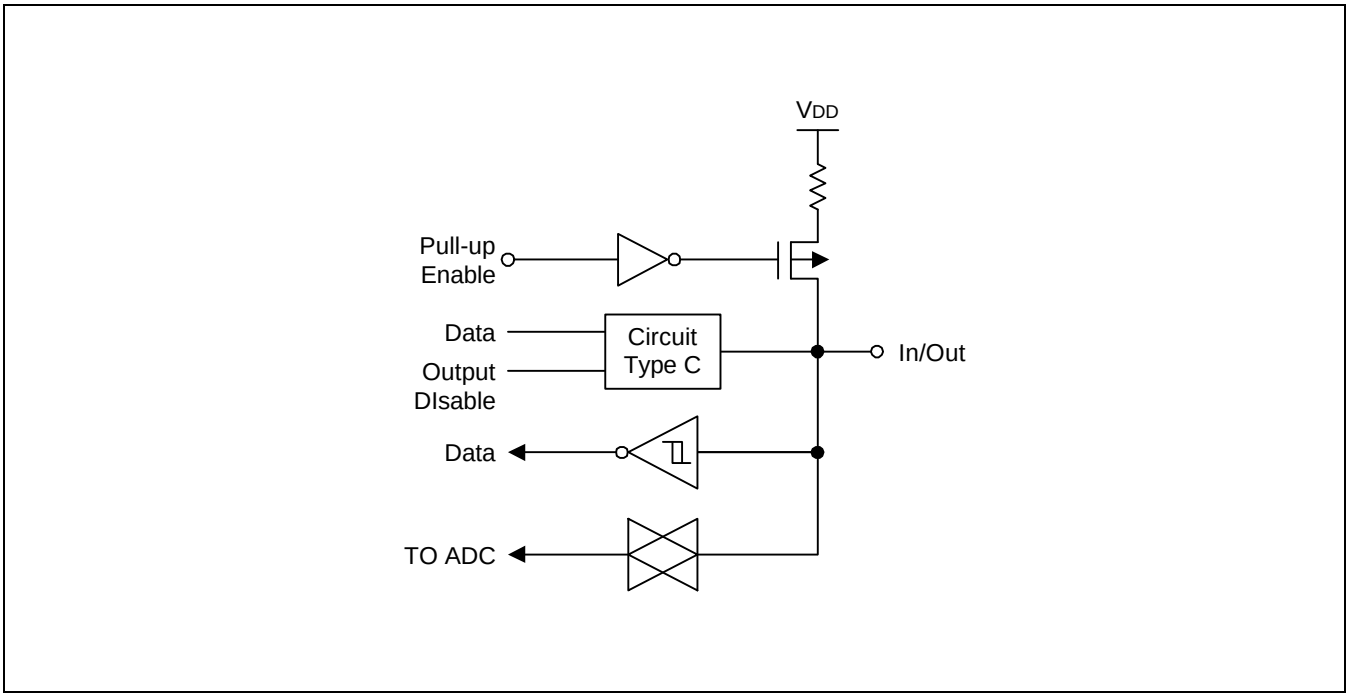


Figure 1-9. Pin Circuit Type F

14 ELECTRICAL DATA

OVERVIEW

In this chapter, S3C8478/C8475 electrical characteristics are presented in tables and graphs. The information is arranged in the following order:

— Absolute maximum ratings
— Input/output capacitance
— D.C. electrical characteristics
— A.C. electrical characteristics
— Oscillation characteristics
— Oscillation stabilization time
— Data retention supply voltage in stop mode
— UART timing characteristics in mode 0
— A/D converter electrical characteristics

Table 1. Absolute Maximum Ratings

(T_A = 25 °C)

Parameter	Symbol	Conditions	Rating	Unit
Supply Voltage	V_{DD}	–	– 0.3 to + 6.5	V
Input Voltage	V_I	All ports	– 0.3 to V_{DD} + 0.3	V
Output Voltage	V_O	All output ports	– 0.3 to V_{DD} + 0.3	V
Output Current High	I_{OH}	One I/O pin active	– 18	mA
		All I/O pins active	– 60	
Output Current Low	I_{OL}	One I/O pin active	+ 30	mA
		Total pin current for ports 1, 2, and 3	+ 100	
		Total pin current for ports 0 and 4	+ 200	
Operating Temperature	T_A	–	– 40 to + 85	°C
Storage Temperature	T_{STG}	–	– 65 to + 150	°C

Table 14-2. D.C. Electrical Characteristics

(T_A = – 40 °C to + 85 °C, V_{DD} = 1.8 V to 5.5 V)

Parameter	Symbol	Test Conditions		Min	Typ	Max	Unit
Input High Voltage	V_{IH1}	Ports 0, 1, 2, 3 ,4 and RESET	V_{DD} = 2.7 to 5.5 V	0.8 V_{DD}	–	V_{DD}	V
	V_{IH3}	$X_{IN,}$ and X_{OUT}		V_{DD}–0.1			
Input Low Voltage	V_{IL1}	Ports 0, 1, 2, 3, 4 and RESET	V_{DD} = 2.7 to 5.5 V	–	–	0.2 V_{DD}	V
	V_{IL3}	X_{IN} and X_{OUT}				0.1	
Output High Voltage	V_{OH}	I_{OH} = – 1 mA Ports 0, 1, 2, 3, 4	V_{DD} = 4.5 to 5.5 V	V_{DD}–1.0	–	–	
Output Low Voltage	V_{OL1}	I_{OL} = 15 mA Port 0, and 4	V_{DD} = 4.5 to 5.5 V	–	0.4	2.0	V
	V_{OL2}	I_{OL} = 4 mA Ports 1, 2, and 3	V_{DD} = 4.5 to 5.5 V		0.4	2.0	V
Input High Leakage Current	I_{LIH1}	All input pins except I_{LIH2} and RESET	V_{IN} = V_{DD}	–	–	1	uA
	I_{LIH2}	$X_{IN,}$ and X_{OUT}	V_{IN} = V_{DD}			20	
Input Low Leakage Current	I_{LIL1}	All input pins except I_{LIL2}	V_{IN} = 0 V	–	–	– 1	uA
	I_{LIL2}	$X_{IN,}$ and X_{OUT}	V_{IN} = 0 V			– 20	
Output High Leakage Current	I_{LOH}	All output pins	V_{OUT} = V_{DD}	–	–	2	uA
Output Low Leakage Current	I_{LOL}	All output pins	V_{OUT} = 0 V	–	–	– 2	uA
Pull-up Resistor	R_{P1}	V_{IN} = 0 V, Ports 0-4	V_{DD} = 5 V	30	47	70	KΩ
	R_{P1}	RESET	V_{DD} = 5 V	100	200	350	
Supply Current	I_{DD1}	RUM mode 12 MHz CPU clock	V_{DD} = 4.5 to 5.5 V	–	10	20	mA
		3 MHz CPU clock	V_{DD} = 1.8 to 2.2 V		1.1	3	
	I_{DD2}	Idle mode 12 MHz CPU clock	V_{DD} = 4.5 to 5.5 V	–	4	8	
		3 MHz CPU clock	V_{DD} = 1.8 to 2.2 V		0.6	1.5	
	I_{DD3}	Stop mode	V_{DD} = 4.5 to 5.5 V	–	0.1	5	uA
			V_{DD} = 1.8 to 2.2 V		0.1	3	

Table 14-3. A.C. Electrical Characteristics

(T_A = – 40 °C to + 85 °C, V_{DD} = 4.5 V to 5.5 V)

Parameter	Symbol	Conditions	Min	Typ	Max	Unit
Interrupt Input High, Low Width	t_{INTH}, t_{INTL}	Ports 2 V_{DD} = 5 V ± 10 %	–	200	–	ns
RESET Input Low Width	t_{RSL}	Input V_{DD} = 5 V ± 10 %	–	1	–	µs

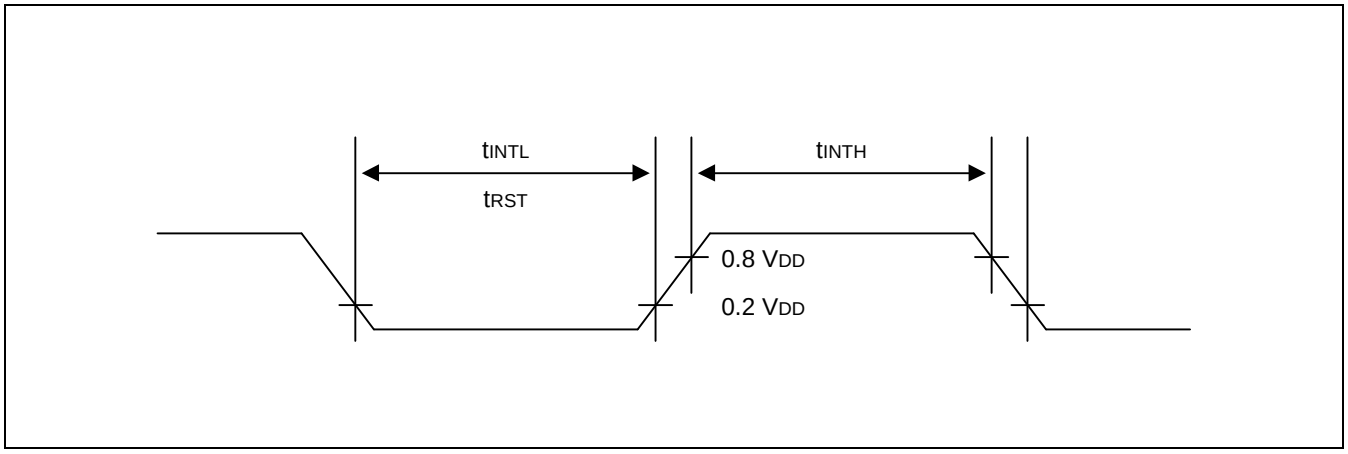
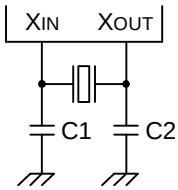
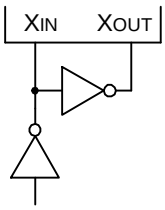


Figure 14-1. Input Timing Measurement Points

Table 14-4. Oscillation Characteristics

(T_A = – 40 °C + 85 °C)

Oscillator	Clock Circuit	Test Condition	Min	Typ	Max	Unit
Main Crystal or Ceramic		V_{DD} = 4.5 V to 5.5 V	1	–	12	MHz
		V_{DD} = 2.7 V to 4.5 V			8	
		V_{DD} = 1.8 V to 2.7 V			3	
External Clock (Main System)		V_{DD} = 4.5 V to 5.5 V	1	–	12	MHz
		V_{DD} = 2.7 V to 4.5 V			8	
		V_{DD} = 1.8 V to 2.7 V			3	

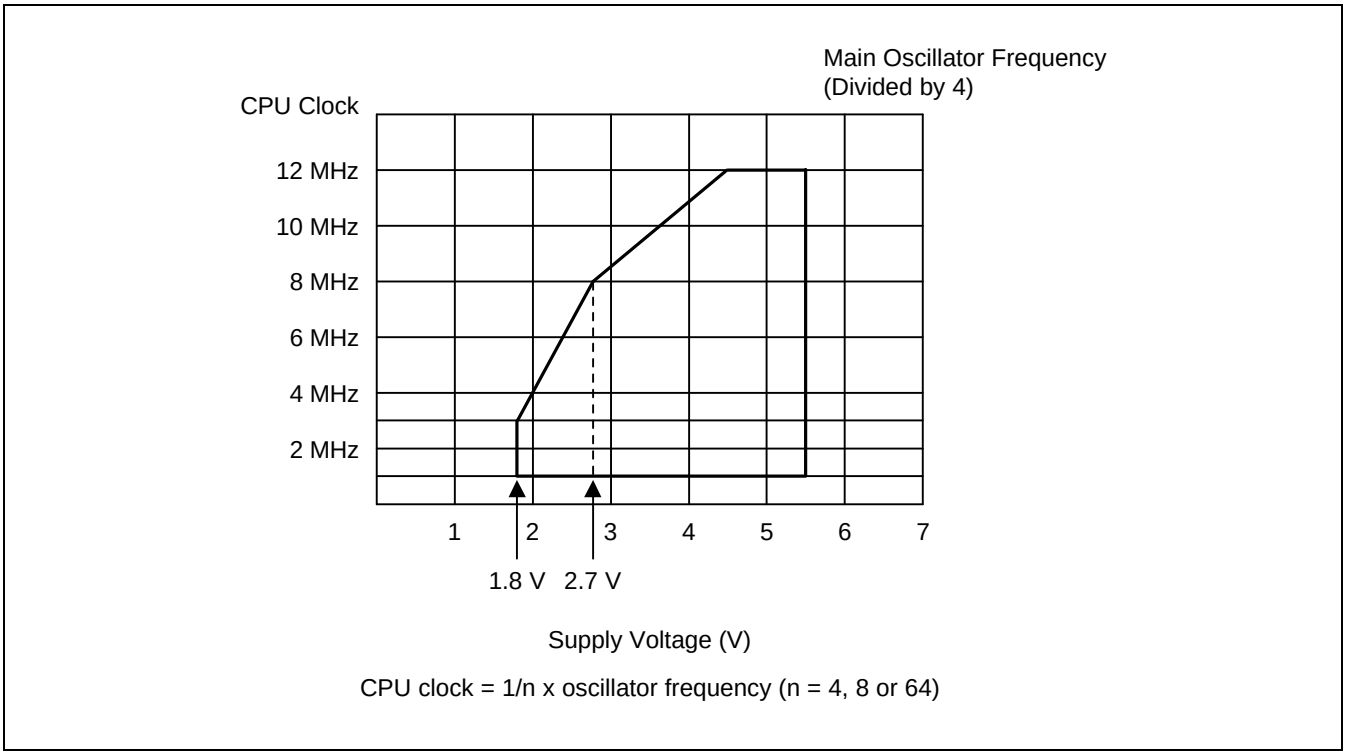


Figure 14-2. Operating Voltage Range

Table 14-5. Oscillation Stabilization Time

(T_A = – 40 °C + 85 °C, V_{DD} = 1.8 V to 5.5 V)

Oscillator	Test Condition	Min	Typ	Max	Unit
Main Crystal	f_{OSC} > 1.0 kHz; Oscillation stabilization occurs when V_{DD} is equal to the minimum oscillator voltage range.	–	–	20	ms
Main Ceramic		–	–	10	ms
External Clock (Main System)	X_{IN} input High and Low width (t_{XH}, t_{XL})	25	–	500	ns
Oscillator Stabilization Wait Time	t_{WAIT} when released by a reset (1)	–	$2^{16}/f_{OSC}$	–	ms
	t_{WAIT} when released by an interrupt (2)	–	–	–	ms

NOTES:
1. f_{OSC} is the oscillator frequency.
2. The duration of the oscillator stabilization wait time, t_{WAIT}, when it is released by an interrupt is determined by the settings in the basic timer control register, BTCON.

Table 14-6. UART Timing Characteristics in Mode 0 (10 MHz)

(T_A = – 40°C to + 85°C, V_{DD} = 1.8 V to 5.5 V, Load capacitance = 80 pF)

Parameter	Symbol	Min	Typ	Max	Unit
Serial port clock cycle time	t_{SCK}	500	$t_{CPU} \times 6$	700	ns
Output data setup to clock rising edge	t_{S1}	300	$t_{CPU} \times 5$	–	
Clock rising edge to input data valid	t_{S2}	–	–	300	
Output data hold after clock rising edge	t_{H1}	$t_{CPU} – 50$	t_{CPU}	–	
Input data hold after clock rising edge	t_{H2}	0	–	–	
Serial port clock High, Low level width	t_{HIGH}, t_{LOW}	200	$t_{CPU} \times 3$	400	

NOTES:
1. All timings are in nanoseconds (ns) and assume a 10-MHz CPU clock frequency.
2. The unit t_{CPU} means one CPU clock period.

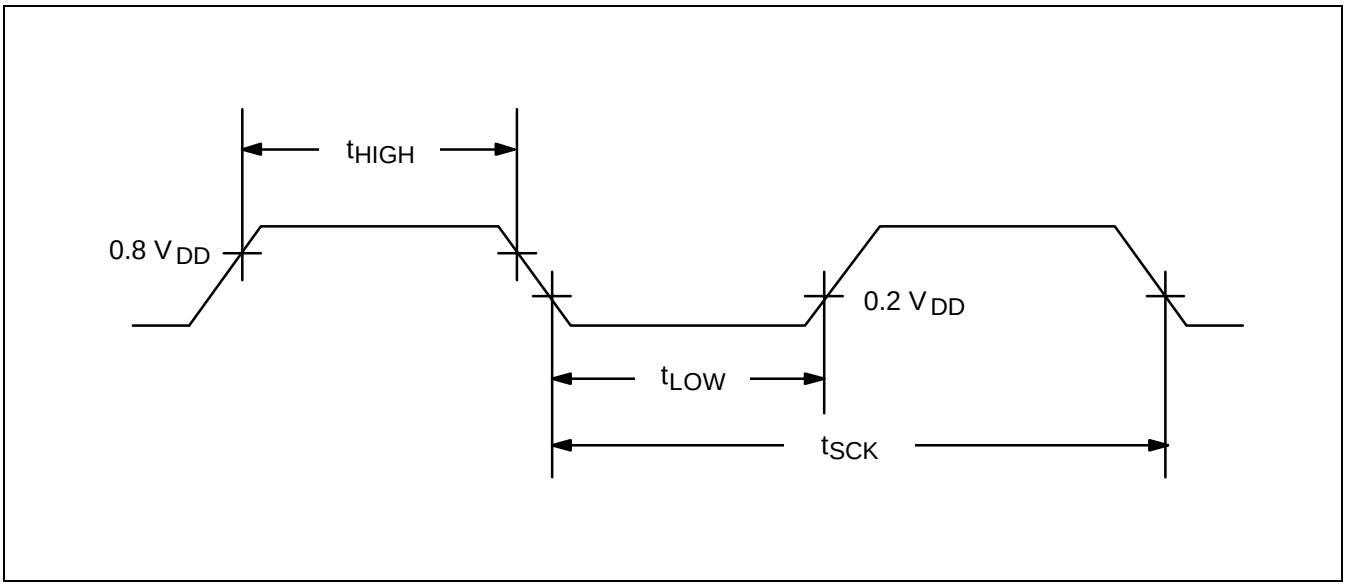
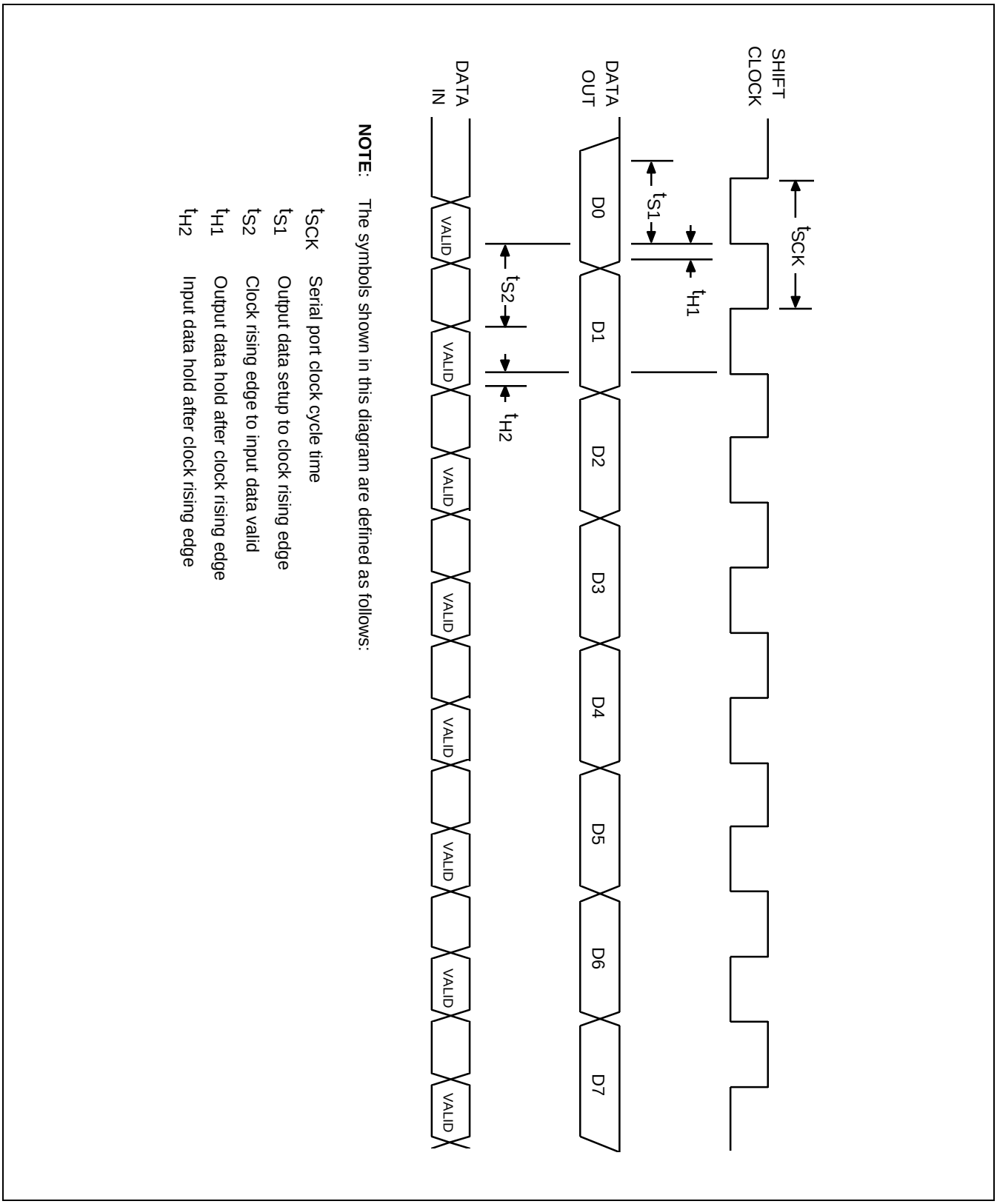


Figure 14-3. Waveform for UART Timing Characteristics



NOTE: The symbols shown in this diagram are defined as follows:

t_{SCK}	Serial port clock cycle time
t_{S1}	Output data setup to clock rising edge
t_{S2}	Clock rising edge to input data valid
t_{H1}	Output data hold after clock rising edge
t_{H2}	Input data hold after clock rising edge

Figure 14-4. A.C. Timing Waveform for the UART Module

Table 14-7. Data Retention Supply Voltage in Stop Mode

(T_A = – 40 °C to + 85 °C, V_{DD} = 1.8 V to 5.5 V)

Parameter	Symbol	Conditions	Min	Typ	Max	Unit
Data Retention Supply Voltage	V_{DDDR}	Stop mode	1.8	–	5.5	V
Data Retention Supply Current	I_{DDDR}	Stop mode, V_{DDDR} = 1.8 V	–	0.1	5	µA

NOTE: Supply current does not include current drawn through internal pull-up resistors or external output current loads.

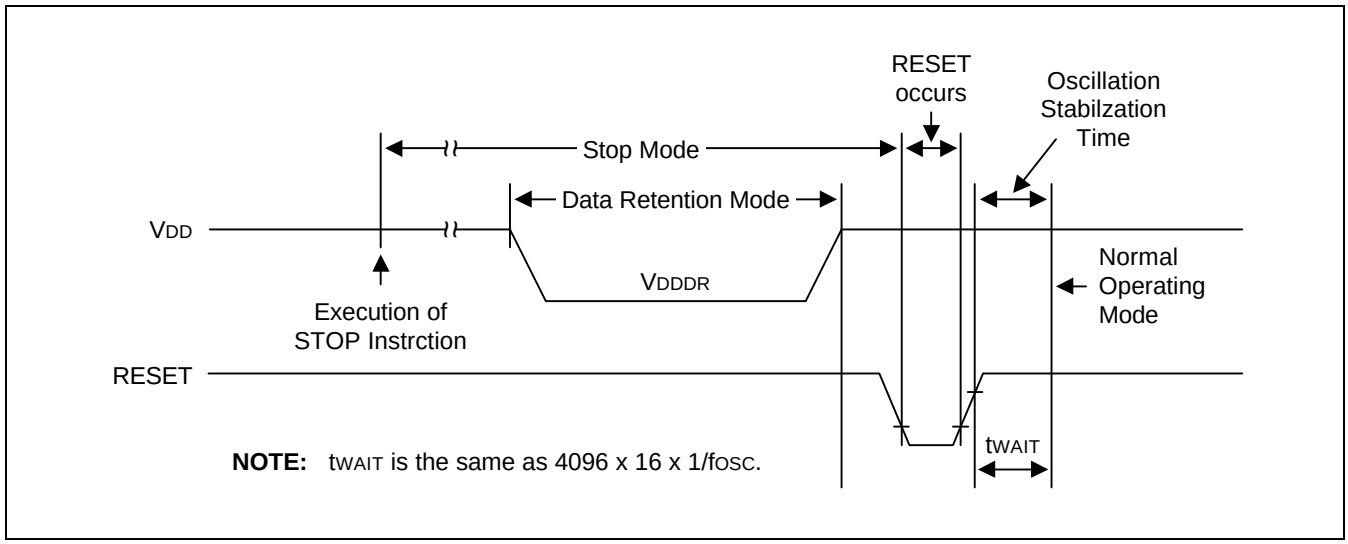


Figure 14-5. Stop Mode Release Timing When Initiated by a Reset

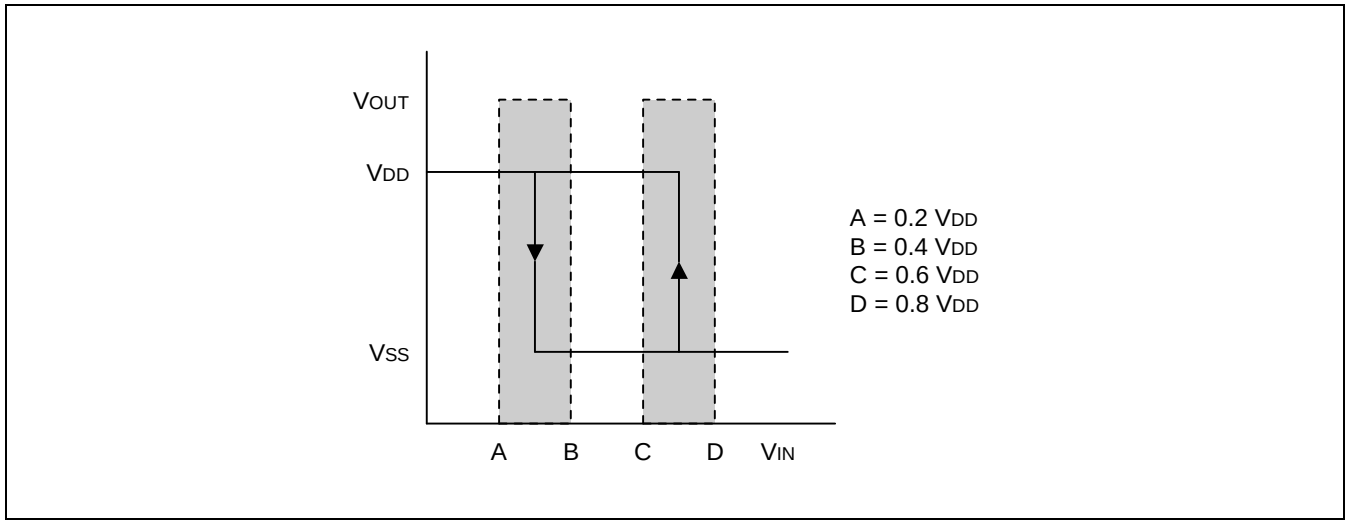


Figure 14-6. Schmitt Trigger Input Characteristics

Table 14-8. A/D Converter Electrical Characteristics

(T_A = – 40°C to + 85°C, V_{DD} = 2.7 V to 5.5 V, V_{SS} = 0 V)

Parameter	Symbol	Test Conditions	Min	Typ	Max	Unit
Total accuracy	–	V_{DD} = 5.12 V	–	–	± 3	LSB
Integral linearity error	ILE	CPU clock = 8 MHz AV_{REF} = 5.12 V		–	± 2	
Differential linearity error	DLE	AV_{SS} = 0 V		–	± 1	
Offset error of top	EOT			± 1	± 3	
Offset error of bottom	EOB			± 1	± 2	
Conversion time (1)	t_{CON}	f_{OSC} = 10 MHz (3)	20	–	–	µs
Analog input voltage	V_{IAN}	–	AV_{SS}	–	AV_{REF}	V
Analog input impedance	R_{AN}	–	2	–	–	MΩ
ADC reference voltage	AV_{REF}	–	2.5	–	V_{DD}	V
ADC reference ground	AV_{SS}	–	V_{SS}	–	V_{SS} + 0.3	V
Analog input current	I_{ADIN}	AV_{CC} = V_{CC} = 5 V	–	–	10	µA
Analog block current (2)	I_{ADC}	AV_{CC} = V_{CC} = 5 V	–	1	3	mA
		AV_{CC} = V_{CC} = 3 V		0.5	1.5	
		AV_{CC} = V_{CC} = 5 V power down mode		100	500	nA

NOTES:

1. "Conversion time" is the time required from the moment a conversion operation starts until it ends.
2. I_{ADC} is operating current during A/D conversion.
3. f_{OSC} is the main oscillator clock.

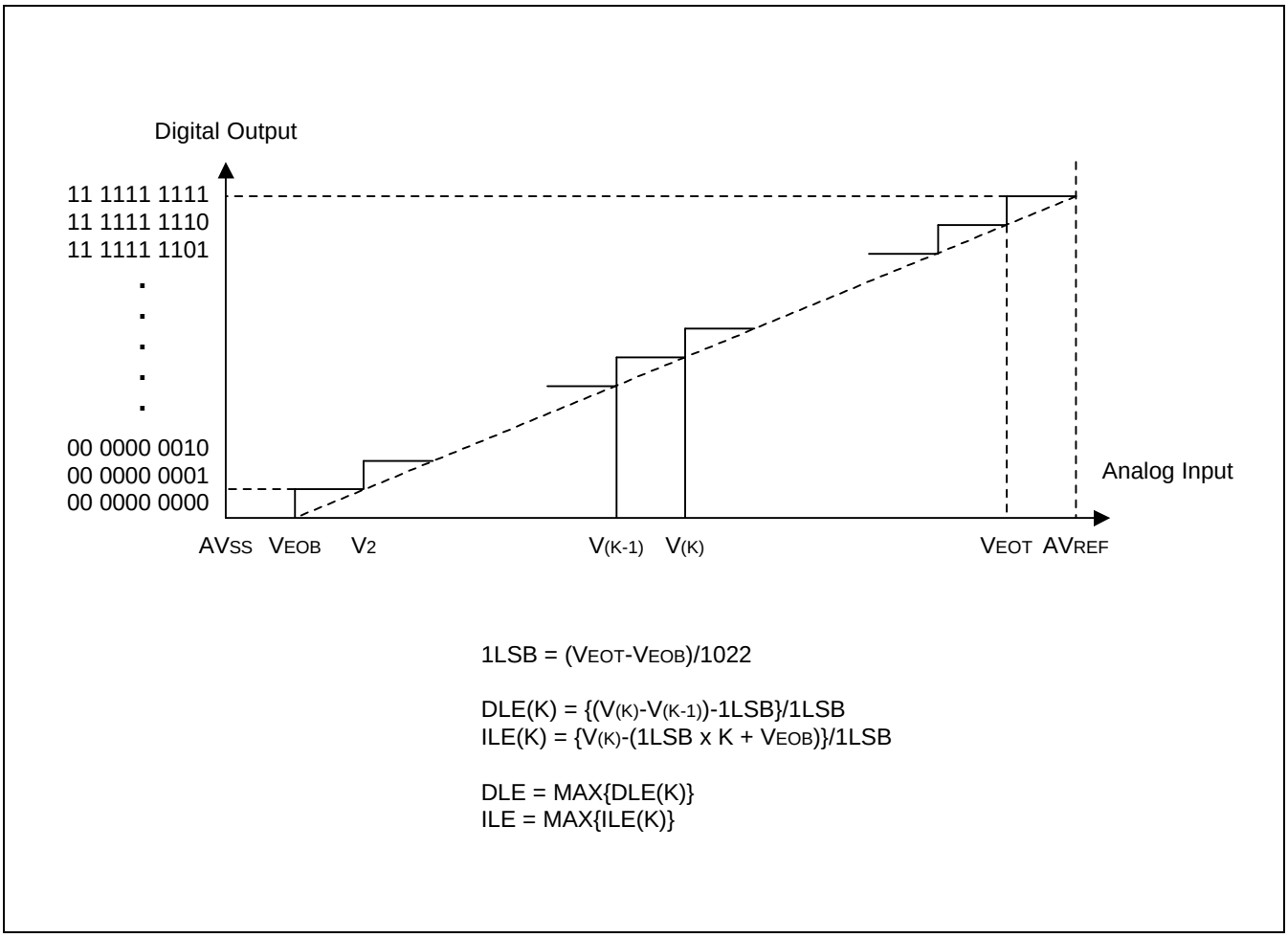


Figure 14-7. Definition of DLE and ILE

15 MECHANICAL DATA

OVERVIEW

This section contains the following information about the device package:

— Package dimensions in millimeters
— Pad diagram

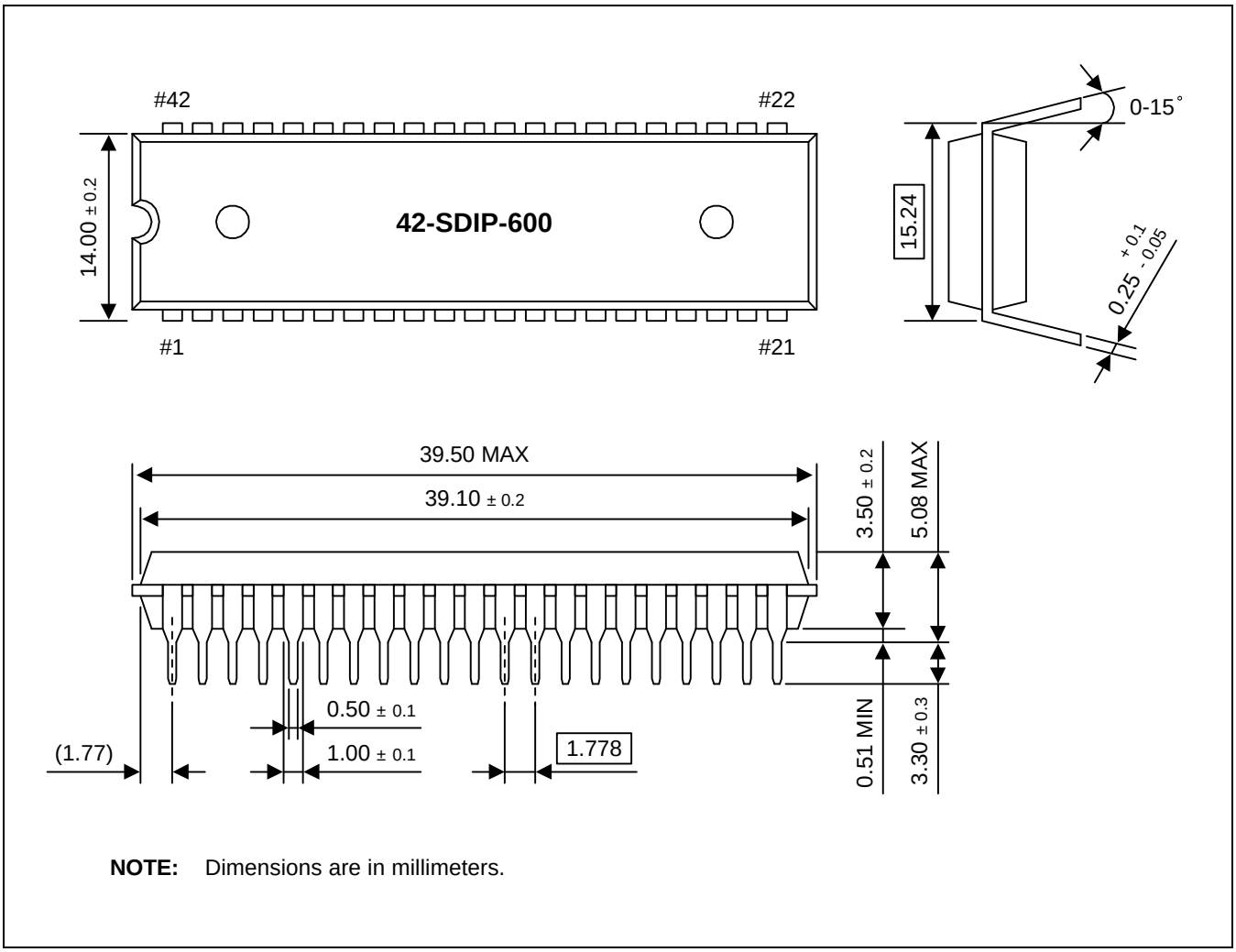
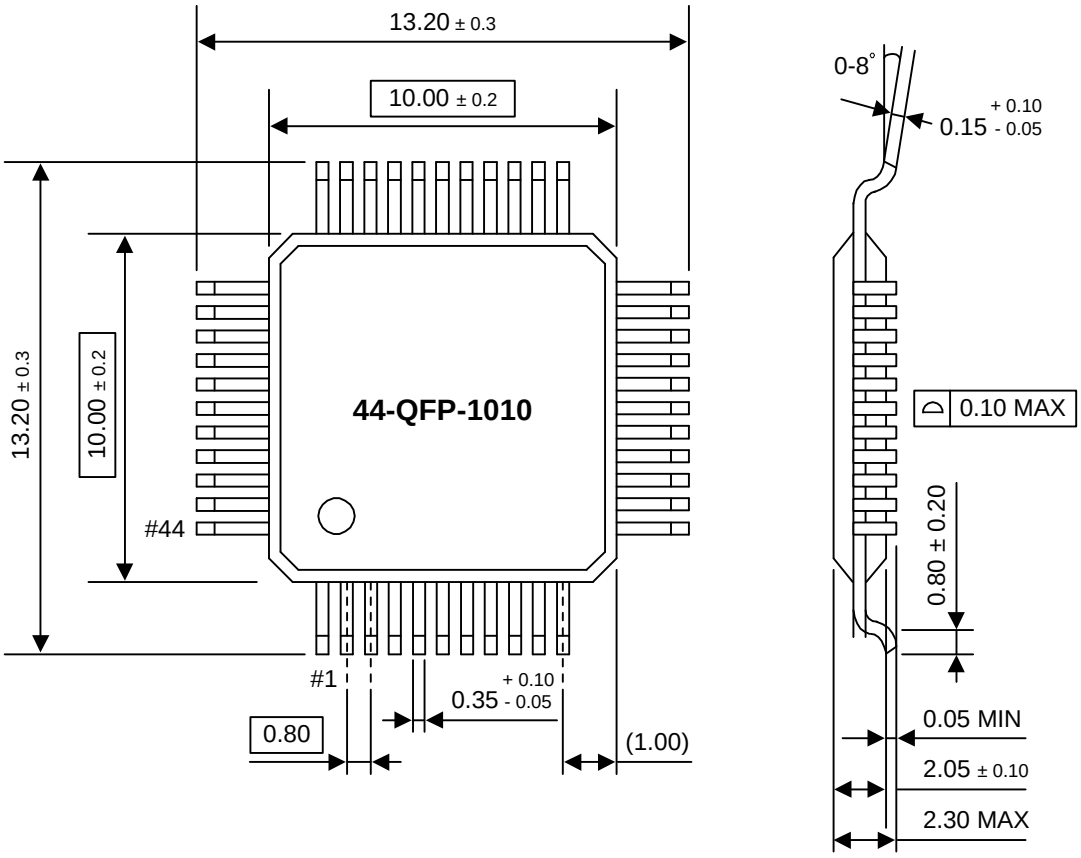


Figure 15-1. 42-SDIP-600 Package Dimensions



NOTE: Dimensions are in millimeters.

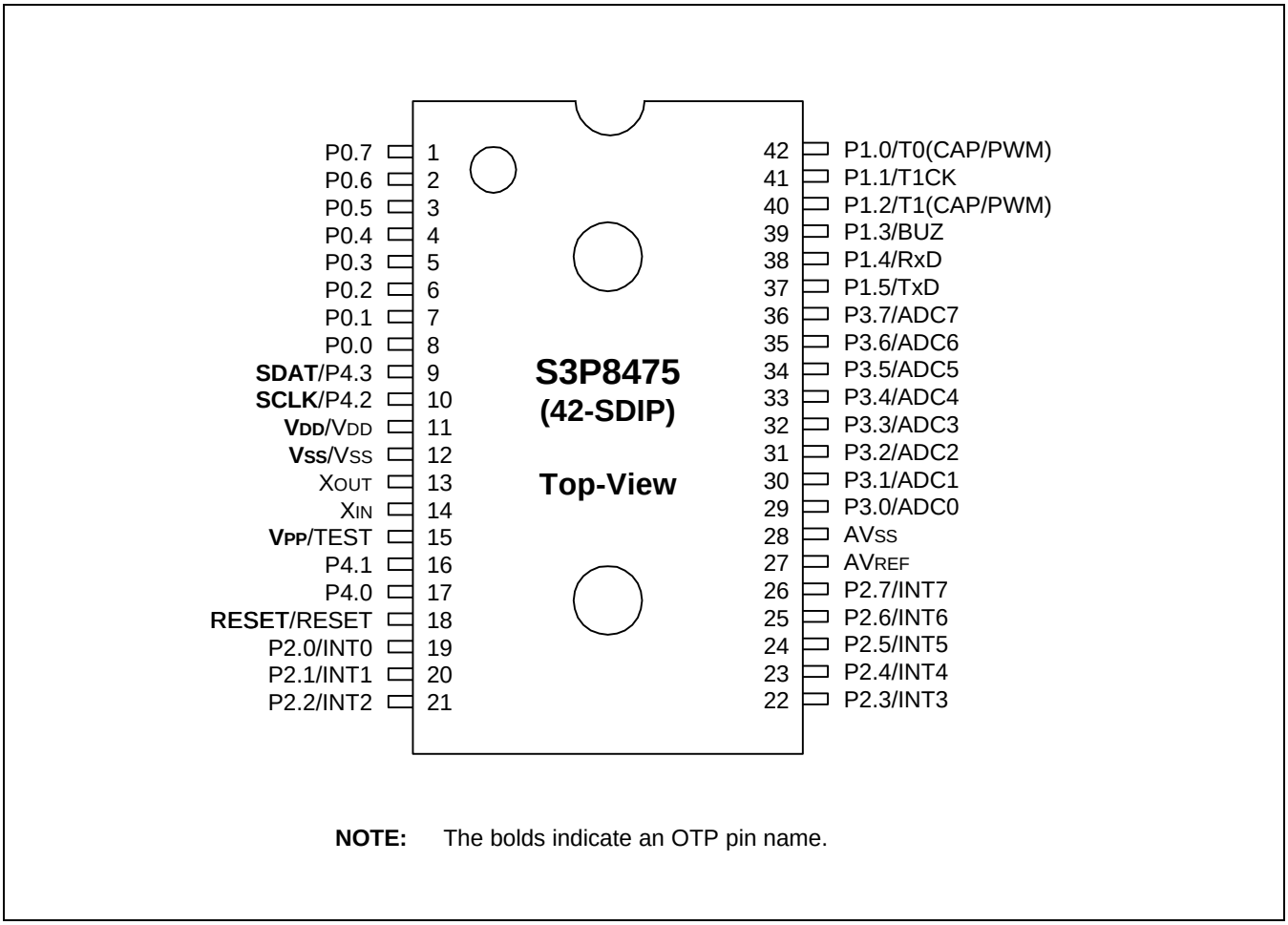
Figure 15-2. 44-QFP-1010 Package Dimensions

16 S3P8475 OTP

OVERVIEW

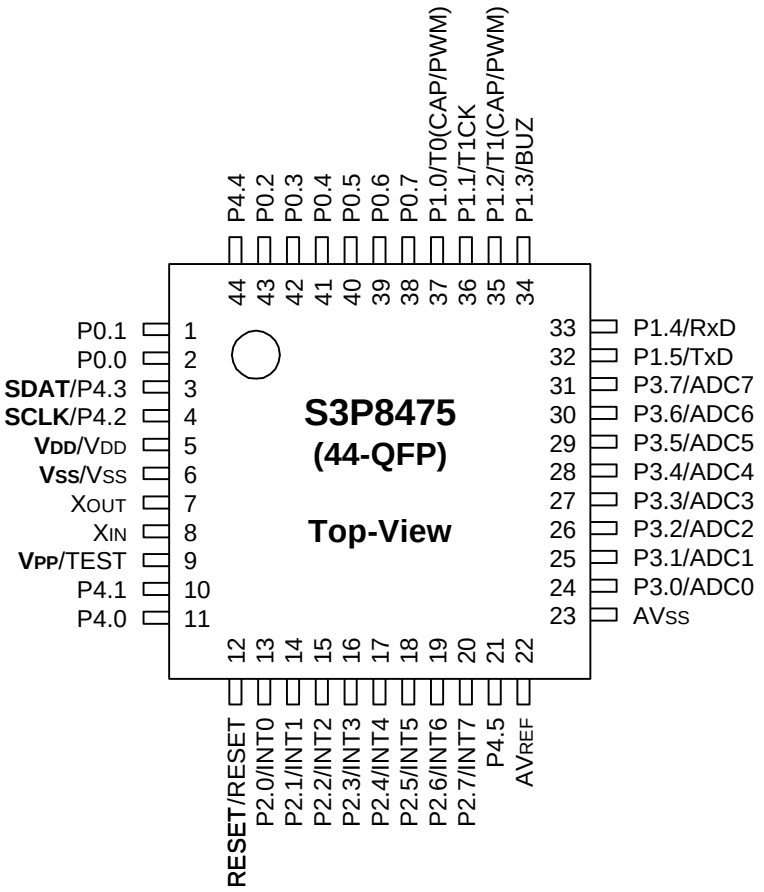
The S3P8475 single-chip CMOS microcontroller is the OTP (One Time Programmable) version of the S3C8478/C8475 microcontroller. It has an on-chip OTP ROM instead of a masked ROM. The EPROM is accessed by serial data format.

The S3P8475 is fully compatible with the S3C8478/C8475, both in function in D.C. electrical characteristics and in pin configuration. Because of its simple programming requirements, the S3P8475 is ideal as an evaluation chip for the S3C8478/C8475.



NOTE: The bolds indicate an OTP pin name.

Figure 16-1. S3P8475 Pin Assignments (42-SDIP Package)



NOTE: The bolds indicate an OTP pin name.

Figure 16-2. S3P8475 Pin Assignments (44-QFP Package)

Table 16-1. Descriptions of Pins Used to Read/Write the EPROM

Main Chip	During Programming			
Pin Name	Pin Name	Pin No.	I/O	Function
P4.3	SDAT	9(3)	I/O	Serial data pin. Output port when reading and input port when writing. Can be assigned as a Input/push-pull output port.
P4.2	SCLK	10(4)	I	Serial clock pin. Input only pin.
TEST	V_{PP}	14(16)	I	Power supply pin for EPROM cell writing (indicates that OTP enters into the writing mode). When 12.5 V is applied, OTP is in writing mode and when 5 V is aplied, OTP is in reading mode. (Option)
RESET	RESET	18(12)	I	Chip Initialization
V_{DD}/V_{SS}	V_{DD}/V_{SS}	11(5)/12(6)	–	Logic power supply pin. V_{DD} should be tied to +5 V during programming.

NOTE: ( ) means 44 QFP package.

Table 16-2. Comparison of S3C8475 and S3C8478/C8475 Features

Characteristic	S3C8475	S3C8478/C8475
Program Memory	16-Kbyte EPROM	8/16-Kbyte mask ROM
Operating Voltage (V_{DD})	1.8 V to 5.5 V	1.8 V to 5.5 V
OTP Programming Mode	V_{DD} = 5 V, V_{PP} (EA) = 12.5 V	
Pin Configuration	42 SDIP/44 QFP	42 SDIP/44 QFP
EPROM Programmability	User Program 1 time	Programmed at the factory

OPERATING MODE CHARACTERISTICS

When 12.5 V is supplied to the V_{PP} (TEST) pin of the S3C8475, the EPROM programming mode is entered. The operating mode (read, write, or read protection) is selected according to the input signals to the pins listed in Table 16-3 below.

Table 16-3. Operating Mode Selection Criteria

V_{DD}	V_{PP} (TEST)	REG/ MEM	ADDRESS (A15–A0)	R/W	MODE
5 V	5 V	0	0000H	1	EPROM read
	12.5 V	0	0000H	0	EPROM program
	12.5 V	0	0000H	1	EPROM verify
	12.5 V	1	0E3FH	0	EPROM read protection

NOTE: "0" means Low level; "1" means High level.