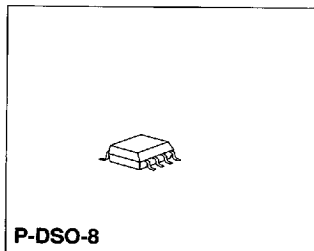


Preliminary Data

Bipolar IC

Features

- Low Current Consumption
- Wide Input Sensitivity
- Wide Input Frequency Range
- TTL/CMOS compatible MOD input
- Standby Mode
- Switchable divider ratios 64/65 or 128/129



Applications

- With its very low (5.7 mA) current consumption the IC has been particularly designed for use in mobile communications. Furthermore, it can be switched to a low-power standby mode. Depending on the external network configuration, dividing ratios of 64/65 or 128/129 can be selected.

Type	Ordering Code	Package
PMB 2312	Q67000-A6039	P-DSO-8 (SMD)

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Circuit Description

The symmetrical differential inputs of the IC may be connected asymmetrically. In this case the unused input must be RF-grounded with a capacitor (ca. 1.5 nF) with a low serial inductance.

Depending on the logic level at SW input the basic divide ratio of the ECL-stages is fixed to 1 : 64/65 or 1 : 128/129. The MOD input determines whether modulus 1 : n or 1 : n + 1 (n = 64 or 128 according to SW-level) is active.

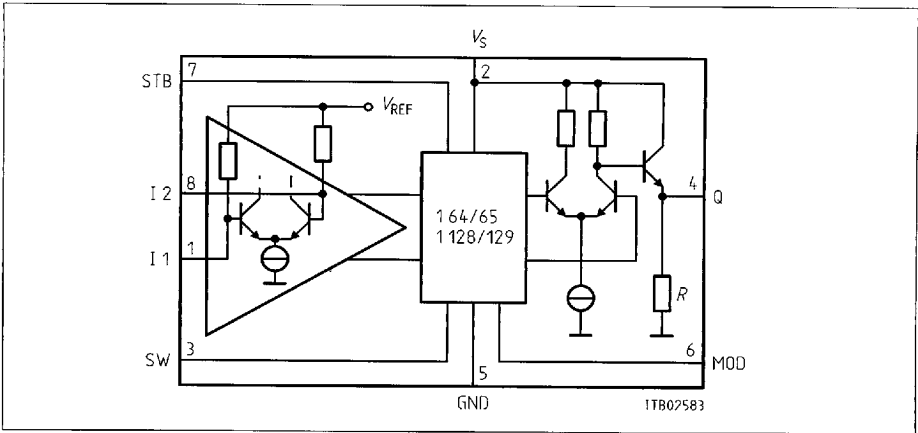
The IC can be switched to a low-power standby mode (input STB).

The MOD input is TTL/CMOS compatible.

The open-emitter output is CMOS compatible according to the **application circuit**. The minimum logic swing is fixed to 1 V_{pp}.

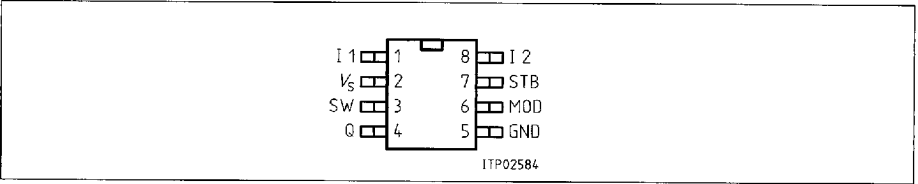
Function Table

Input Pin	Logic Level	Prescaler Function
SW	high = 3.0 to V_s low = GND to 0.8 V or open	1 : 64/65 1 : 128/129
MOD	high = 2.0 V to V_s or open low = GND to 0.8 V	1 : 64/1 : 128 1 : 65/1 : 129
STB	high = $V_s - 0.1$ V to V_s or open low = GND to 0.8 V	Divider Q = high, standby-mode



Block Diagram

Pin Configuration
(top view)



Pin Definitions and Functions

Pin No.	Symbol	Function
1	I1	Input I1
2	V_s	Supply voltage
3	SW	Divide ratio 1 : 64/65 – 1 : 128/129 control input
4	Q	Output
5	GND	Ground
6	MOD	Modulus 1 : n/n + 1 (n = 64 or 128) control input
7	STB	Standby mode control input
8	I2	Input I2

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Electrical Characteristics

Absolute Maximum Ratings

 $T_A = -40$ to $85\text{ }^{\circ}\text{C}$

Parameter	Symbol	Limit Values		Unit
		min.	max.	
Supply voltage	V_S	-0.3	6	V
Input level (pin 1; pin 8)	V_I	1	5	V
Voltage swing (pin 1 to pin 8)	V_{I18}	-3	3	V
Input level (pin 3; pin 6; pin 7)	V_{SW}, V_{MOD}, V_{STB}	-0.3	6	V
Output level (pin 4)	V_Q		V_S	V
Output current (pin 4)	$-I_Q$		10	mA
Junction temperature	T_J		125	$^{\circ}\text{C}$
Storage temperature	T_{stg}	-65	125	$^{\circ}\text{C}$
Thermal resistance system-ambient	R_{thSA}		185	K/W

Operating Range

Supply Voltage	V_S	4.0	5.5	V
Input frequency	f	130	1100	MHz
Ambient temperature	T_A	-40	85	$^{\circ}\text{C}$

AC/DC Characteristics

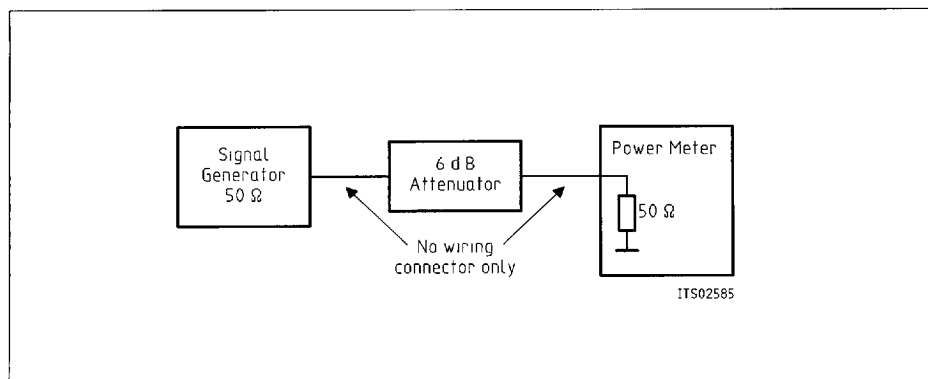
$V_S = 4.0$ to 5.5 V; $T_A = -40$ to 85 °C; refer to test circuit

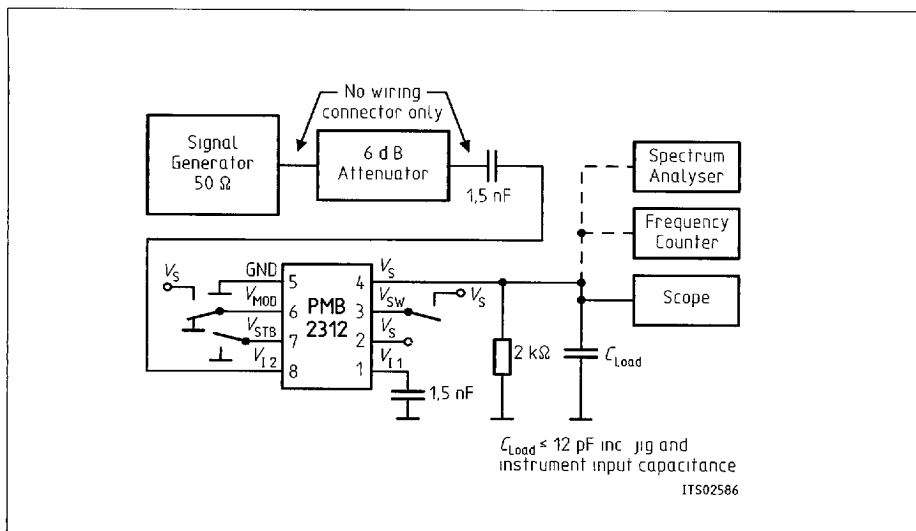
Parameter	Symbol	Limit Values			Unit	Test Condition
		min.	typ.	max.		
Supply current	I_S		5.7	7.4	mA	inputs RF-grounded, $V_S = 4.0$ V, $T_A = 25$ °C STB open, output open
Supply current	I_S		5.8	7.5	mA	inputs RF-grounded, $V_S = 5.0$ V, $T_A = 25$ °C STB open, output open
Supply current	I_S		5.9	7.7	mA	inputs RF-grounded, $V_S = 5.5$ V, $T_A = 25$ °C STB open, output open
Supply current in standby-mode	I_{SSTB}		0.3	0.45	mA	inputs RF-grounded, output open, STB = GND
Input level	V_I	25		400	mVrms	140 – 1000 MHz
Input sensitivity (diagram 2)		– 19		5	dBm	sine wave
Output logic swing	V_O	1			Vpp	$C_L \leq 12$ pF
SW threshold voltage high	V_{SWH}	3.0		V_S	V	
SW threshold voltage low	V_{SWL}	GND		0.8	V	
SW input current high	I_{SWH}			100	μA	SW = V_S
SW input current low	$-I_{SWL}$			50	μA	SW = GND
MOD threshold voltage high	V_{MODH}	2.0		V_S	V	
MOD threshold voltage low	V_{MODL}	GND		0.8	V	
MOD input current high	I_{MODH}			50	μA	MOD = V_S
MOD input current low	$-I_{MODL}$			100	μA	MOD = GND
STB threshold voltage high	V_{STBH}	$V_S - 0.1$		V_S	V	
STB threshold voltage low	V_{STBL}			0.8	V	
STB input current high	I_{STBH}			50	μA	STB = V_S
STB input current low	$-I_{STBL}$			160	μA	STB = GND
Internal load resistance (see block diagram)	R		50		kΩ	

Delay Times

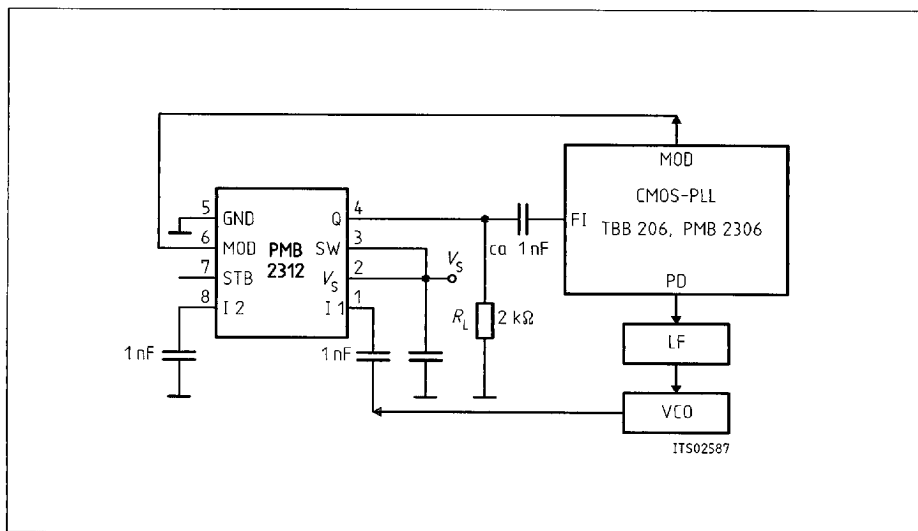
MOD setup time (diagram 1)	t_{set}			29	ns	
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**Test Circuits Calibration of the Signal Generator**



Input Sensitivity and Output Logic Swing Measurement



Application Circuit

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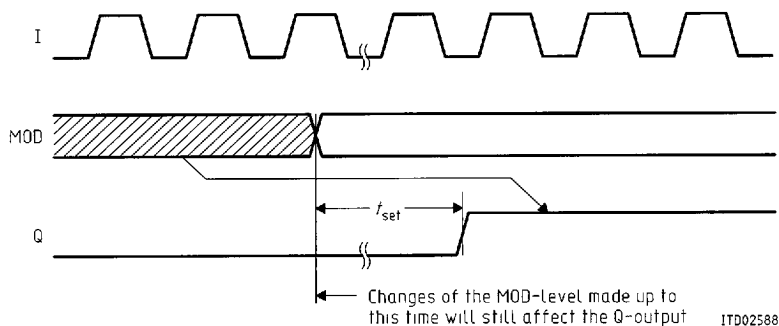
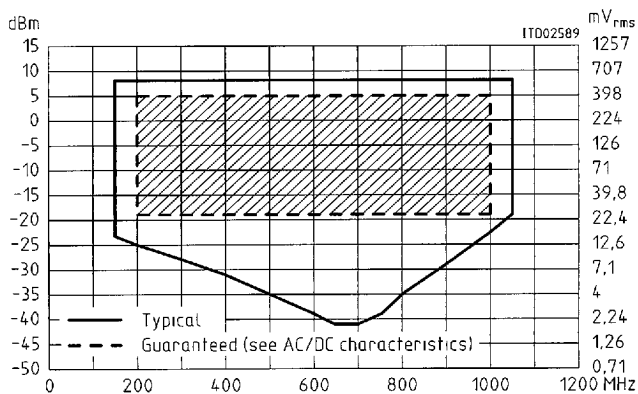


Diagram 1

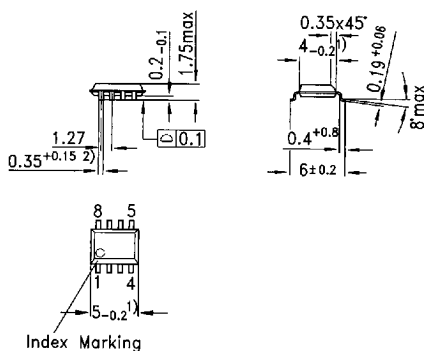
Diagram 2
Input Sensitivity

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Plastic Package, P-DSO-8 (SMD)
(Plastic Dual Small Outline)



- 1) Does not include plastic or metal protrusions of 0.15 max per side
- 2) Does not include dambar protrusion of 0.05 max per side

GPS05121

Sorts of Packing

Package outlines for tubes, trays etc. are contained in our
 Data Book "Package Information"

SMD = Surface Mounted Device

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Dimensions in mm

B115-H6626-
 G1-X-7600