Advance Information

High Resolution Frequency Generator

General Description

The ICS9123 is a multiple output frequency generator utilizing PLL (Phase-Lock Loop) frequency synthesis. It contains three PLL frequency synthesizers and an internal crystal oscillator reference circuit. Thus, with only an external crystal and the necessary power supply decoupling capacitors, four different output clock frequencies can be provided.

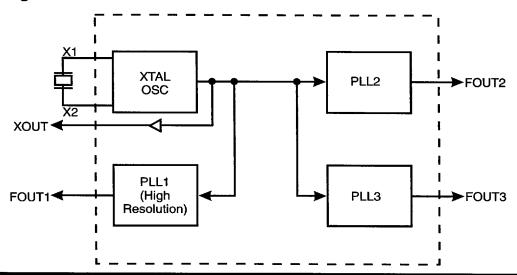
PLL1 of the device has the ability to provide high output frequency resolution (±50 ppm). This makes it suitable for providing clocks for system functions such as modems, ethernet, and sound synthesis. PLL2 and PLL3 provide output clocks for other system applications such as microprocessors and DSP chips. For example, in modem applications, the ICS9123 generates the high resolution clock generator for the A/D converter and two lower resolution clocks for the microprocessor and DSP.

Each of the PLL clock generators has a ROM based frequency selection table which is addressed through device input pins. PLL1 has eight frequency select locations; PLL2 and PLL3 each has four. The ROM based tables are preprogrammed. However, they can be customized for the user specific applications.

Features

- Cost effective solution for MODEM, ETHERNET and AD1848 applications
- Three independent PLLs
- Four clock frequencies generated from one crystal
- One high resolution PLL provides ±50 ppm accuracy
- Eight ROM based frequency selections for the high resolution PLL1
- Four ROM based frequency selections each for PLL2 and PLL3
- 3.3V or 5V power supply
- On-chip loop filter components
- Low power CMOS technology
- 20- or 16-pin PDIP or SOIC package

Block Diagram



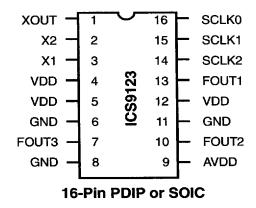
ICS9123RevA111095

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ICS9123



Pin Configuration



Decoding Table for Clock Frequency (Using 14.318 MHz Input Frequency)

SCLK2	SCLK1	SCLK0	FOUT1* (MHz)	FOUT2 (MHz)	FOUT3 (MHz)
0 0 0 0 1 1 1	0 0 1 1 0 0	0 1 0 1 0 1 0	8.06400 19.66080 29.49120 11.05920 13.82400 3.68640 14.74560 16.00031	19.7 29.5 8.06 14.6 19.7 29.5 8.06 14.6	29.5 8.06 19.7 16.5 29.5 8.06 19.7 16.5

*FOUT1 frequencies shown are accurate to within 2 PPM.

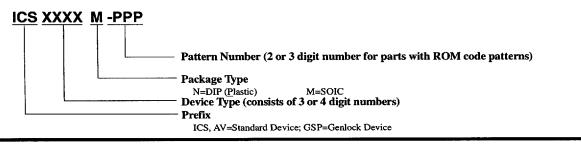
Pin Descriptions

PIN NUMBER	PIN NAME	TYPE	DESCRIPTION	
1	XOUT	Output	Crystal buffered output.	
2	X2	Output	Connect crystal.	
3	X1	Input	Connect crystal.	
4	VDD	-	3V or 5V power supply.	
5	VDD	-	3V or 5V power supply.	
6	GND	<u>-</u>	GROUND.	
7	FOUT3	Output	Output frequency of one of 3 PLLs.	
8	GND	_	GROUND.	
9	VDD	-	3V or 5V power supply.	
10	FOUT2	Output	Output frequency of one of 3 PLLs.	
11	GND	-	GROUND.	
12	VDD	-	3V or 5V power supply.	
13	FOUT1	Output	Output frequency of the high resolution PLL.	
14	SCLK2	Input	CPU clock frequency SELECT2 (has pull-up).	
15	SCLK1	Input	CPU clock frequency SELECT1 (has pull-up).	
16	SCLK0	Input	CPU clock frequency SELECTO (has pull-up).	

Ordering Information ICS9123N-01 or ICS9123M-01

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Example:



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