HY51V16400B Series

4M x 4-bit CMOS DRAM

PRELIMINARY

DESCRIPTION

The HY51V16400B is the new generation and fast dynamic RAM organized 4,194,304 x 4-bit. The HY51V16400B utilizes Hyundai's CMOS silicon gate process technology as well as advanced circuit techniques to provide wide operating margins to the users. Multiplexed address inputs permit the HY51V16400B to be packaged in standard 24/26 pin plastic SOJ, TSOP-II and Reverse TSOP-II.

The package size provides high system bit densities and is compatible with widely available automated testing and insertion equipments. System oriented feature includes single power supply of 3.3V±10% tolerance and direct interfacing capability with high performance logic families such as Schottky TTL.

FEATURES

- **Low power dissipation**
  Max. battery back-up 2.2mW (SL-part)
  Max. CMOS standby 0.72mW (SL-part)
  1.8mW
  Max. TTL standby 3.6mW
  Max. operating

Speed	Power
60	324mW
70	288mW
80	252mW

- **Single power supply of 3.3V±10%**
- **TTL compatible inputs and outputs**
- **Fast access and cycle time**

Speed	tRAC	tCAC	tPC
60	60ns	15ns	40ns
70	70ns	18ns	45ns
80	80ns	20ns	50ns

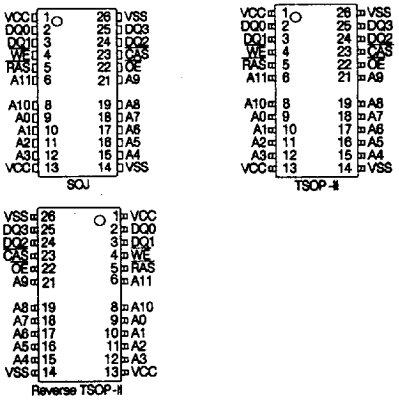
- **Fast page mode operation**
- **Multi-bit test capability**
- **Read-Modify-Write capability**
- **$\overline{CAS}$-before-$\overline{RAS}$, $\overline{RAS}$-only, Hidden refresh and Self Refresh capability**
- **4096 refresh cycles / 256ms (SL-part)**
  4096 refresh cycles / 64ms

PIN DESCRIPTION

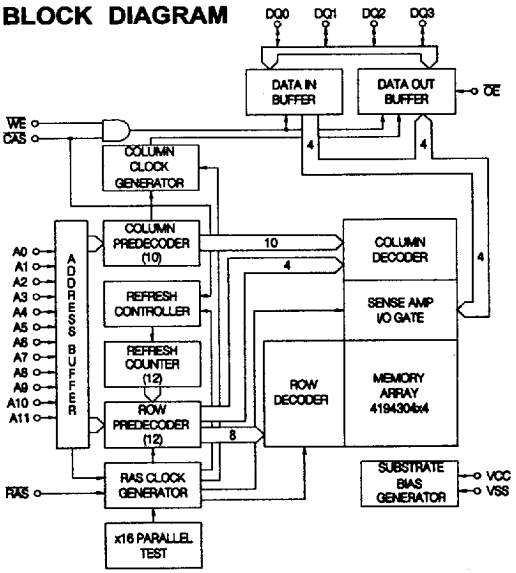
$\overline{RAS}$	Row Address Strobe
$\overline{CAS}$	Column Address Strobe
$\overline{WE}$	Write Enable
$\overline{OE}$	Output Enable
A0-A11*	Address input
DQ0-DQ3	Data Input/Output
Vcc	Power (+3.3V)
Vss	Ground

*A10 and A11 are applied to row address input only.

PIN CONNECTION



BLOCK DIAGRAM



ABSOLUTE MAXIMUM RATING

SYMBOL	PARAMETER	RATING	UNIT
T_A	Ambient Temperature	0 to 70	°C
T_{STG}	Storage Temperature	-55 to 150	°C
V_{IN}, V_{OUT}	Voltage on Any Pin Relative to Vss	-0.5 to 4.6	V
V_{CC}	Voltage on Vcc Relative to Vss	-0.5 to 4.6	V
I_{OS}	Short Circuit Output Current	20	mA
P_D	Power Dissipation	1	W
T_{SOLDER}	Soldering Temperature • Time	260 • 10	°C • sec

NOTE:Operation at or above Absolute Maximum Ratings can adversely affect device reliability.

RECOMMENDED DC OPERATING CONDITIONS

(T_A = 0°C to 70°C)

SYMBOL	PARAMETER	MIN.	TYP.	MAX.	UNIT
V_{CC}	Supply Voltage	3.0	3.3	3.6	V
V_{IH}	Input High Voltage	2.0	-	Vcc+0.3	V
V_{IL}	Input Low Voltage	-0.3	-	0.8	V

NOTE: All Voltage are referenced to V_{SS}.

DC CHARACTERISTICS

(T_A=0°C to 70°C, V_{CC}=3.3V ± 10%, V_{SS}=0V, unless otherwise noted.)

SYMBOL	PARAMETER	TEST CONDITIONS	SPEED/ POWER	MIN.	MAX.	UNIT	NOTE
I_{LI}	Input Leakage Current (Any Input Pins)	$V_{SS} \le V_{IN} \le V_{CC}$+1.0V All other pins not under test=V_{SS}		-10	10	µA	
I_{LO}	Output Leakage Current (High impedance State)	$V_{SS} \le V_{OUT} \le V_{CC}$ $\overline{RAS}$ & $\overline{CAS}$ at V_{IH}		-10	10	µA	
I_{CC1}	V_{CC} Supply Current, Operating	t_{RC} = t_{RC}(min.)	60 70 80	- - -	90 80 70	mA	1,2,3
I_{CC2}	V_{CC} Supply Current, TTL Standby	$\overline{RAS}$ & $\overline{CAS}$ at V_{IH}, other inputs≥V_{SS}		-	1	mA	
I_{CC3}	V_{CC} Supply Current, $\overline{RAS}$-only refresh	t_{RC} = t_{RC}(min.)	60 70 80	- - -	90 80 70	mA	1,3
I_{CC4}	V_{CC} Supply Current, Fast page mode	t_{PC} = t_{RC}(min.)	60 70 80	- - -	80 70 60	mA	1,2,3
I_{CC5}	V_{CC} Supply Current, CMOS Standby	$\overline{RAS}$ & $\overline{CAS}$≥V_{CC}-0.2V	 SL-part	- -	0.5 0.2	mA	5
I_{CC6}	V_{CC} Supply Current, $\overline{CAS}$-before-$\overline{RAS}$ Refresh	t_{RC} = t_{RC}(min.)	60 70 80	- - -	90 80 70	mA	1,3
I_{CC7}	V_{CC} Supply Current, Battery Back up (SL-part only)	t_{RC}=62.5µs, $\overline{CAS}$=CBR cycling or 0.2V $\overline{WE}$=V_{CC}-0.2V, A0-A11=V_{CC}-0.2V or 0.2V, DQ0-DQ3=V_{CC}-0.2V, 0.2V or open	t_{RAS}≤ 300ns t_{RAS}≤ 1µs	- -	350 600	µA	1,4,5
I_{CC8}	V_{CC} Supply Current, Self Refresh (SL-part only)	$\overline{RAS}$ & $\overline{CAS}$ ≤ 0.2V, $\overline{OE}$ & $\overline{WE}$ & A0-A11=V_{CC}-0.2V or 0.2V, DQ0-DQ3=V_{CC}-0.2V, 0.2V or open		-	300	µA	5
V_{OL}	Output Low Voltage	I_{OL} = 2.0mA		-	0.4	V	
V_{OH}	Output High Voltage	I_{OH} = -2.0mA		2.4	-	V	

NOTE:
1. I_{CC1}, I_{CC3}, I_{CC4}, I_{CC6} and I_{CC7} depend on cycle rate.
2. I_{CC1}, I_{CC3}, I_{CC4} and I_{CC6} depend on output loading. Specified values are obtained with the output open.
3. I_{CC} is specified as average current. I_{CC1}, I_{CC3}, I_{CC6}, Address can be changed maximum two times while $\overline{RAS}$=V_{IL}. I_{CC4}, Address can be changed maximum once while $\overline{CAS}$=V_{IH}.
4. t_{RAS}(max.)=1µs is only applied to refresh of battery backup but t_{RAS}(max.)=10µs is applied to normal functional operating.
5. I_{CC5}(max.)=0.2mA and I_{CC7} and I_{CC8} are applied to SL-part only.

AC CHARACTERISTICS

(TA=0°C to 70°C, Vcc=3.3V ± 10%, Vss=0V, unless otherwise noted.) NOTE: 1,2,3

#	SYMBOL	PARAMETER	HY51V16400BJ/T/R/SLJ/SLT/SLR						UNIT	NOTE
			-60		-70		-80			
			MIN.	MAX.	MIN.	MAX.	MIN.	MAX.		
1	tRC	Random Read or Write Cycle Time	110	-	130	-	150	-	ns	
2	tRWC	Read-Modify-Write Cycle Time	160	-	180	-	200	-	ns	
3	tPC	Fast Page Mode Cycle Time	40	-	45	-	50	-	ns	
4	tPRWC	Fast Page Mode Read-Modify-Write Cycle Time	85	-	90	-	100	-	ns	
5	tRAC	Access Time form $\overline{RAS}$	-	60	-	70	-	80	ns	4,9,10
6	tCAC	Access Time from $\overline{CAS}$	-	15	-	18	-	20	ns	4,9
7	tAA	Access Time from Column Address	-	25	-	30	-	35	ns	4,10
8	tCPA	Access Time from $\overline{CAS}$ Precharge	-	35	-	40	-	45	ns	4
9	tCLZ	$\overline{CAS}$ to Output Low Impedance	0	-	0	-	0	-	ns	
10	tOFF	Output Buffer Turn-off Delay	0	13	0	15	0	15	ns	
11	tT	Transition Time (Rise and Fall)	3	50	3	50	3	50	ns	3
12	tRP	$\overline{RAS}$ Precharge Time	40	-	50	-	60	-	ns	
13	tRAS	$\overline{RAS}$ Pulse Width	60	10K	70	10K	80	10K	ns	
14	tRASP	$\overline{RAS}$ Pulse Width (Fast Page Mode)	60	200K	70	200K	80	200K	ns	
15	tRSH	$\overline{RAS}$ Hold Time	15	-	18	-	20	-	ns	
16	tCSH	$\overline{CAS}$ Hold Time	60	-	70	-	80	-	ns	
17	tCAS	$\overline{CAS}$ Pulse width	15	10K	18	10K	20	10K	ns	
18	tRCD	$\overline{RAS}$ to $\overline{CAS}$ Delay	20	45	20	52	20	60	ns	9
19	tRAD	$\overline{RAS}$ to Column Address Delay Time	15	30	15	35	15	40	ns	10
20	tCRP	$\overline{CAS}$ to $\overline{RAS}$ Precharge Time	5	-	5	-	5	-	ns	
21	tCP	$\overline{CAS}$ Precharge Time	10	-	10	-	10	-	ns	
22	tASR	Row Address Set-up Time	0	-	0	-	0	-	ns	
23	tRAH	Row Address Hold Time	10	-	10	-	12	-	ns	
24	tASC	Column Address Set-up Time	0	-	0	-	0	-	ns	
25	tCAH	Column Address Hold Time	10	-	10	-	15	-	ns	
26	tAR	Column Address Hold Time from $\overline{RAS}$	50	-	50	-	55	-	ns	
27	tRAL	Column Address to $\overline{RAS}$ Lead Time	30	-	35	-	40	-	ns	
28	tRCS	Read Command Set-up Time	0	-	0	-	0	-	ns	
29	tRCH	Read Command Hold Time Referenced to $\overline{CAS}$	0	-	0	-	0	-	ns	6
30	tRRH	Read Command Hold Time Referenced to $\overline{RAS}$	0	-	0	-	0	-	ns	6
31	tWCH	Write Command Hold Time	10	-	10	-	15	-	ns	
32	tWCR	Write Command Hold Time from $\overline{RAS}$	45	-	55	-	60	-		
33	tWP	Write Command Pulse Width	10	-	10	-	15	-	ns	
34	tRWL	Write Command to $\overline{RAS}$ Lead Time	15	-	18	-	20	-	ns	
35	tCWL	Write Command to $\overline{CAS}$ Lead Time	15	-	18	-	20	-	ns	
36	tDS	Data-In Set-up Time	0	-	0	-	0	-	ns	7
37	tDH	Data-In Hold Time	10	-	10	-	10	-	ns	7
38	tDHR	Data-in Hold Time Referenced to $\overline{RAS}$	50	-	50	-	55	-	ns	
39	tREF	Refresh Period(4096) SL-part	- -	64 256	- -	64 256	- -	64 256	ms ms	12 11
40	tWCS	Write Command Set-up Time	0	-	0	-	0	-	ns	8

AC CHARACTERISTICS

(continued)

#	SYMBOL	PARAMETER	HY51V16400BJ/T/R/SLJ/SLT/SLR						UNIT	NOTE
			-60		-70		-80			
			MIN.	MAX.	MIN.	MAX.	MIN.	MAX.		
41	tCWD	$\overline{CAS}$ to $\overline{WE}$ Delay Time	38	-	43	-	45	-	ns	8
42	tRWD	$\overline{RAS}$ to $\overline{WE}$ Delay Time	83	-	95	-	105	-	ns	8
43	tAWD	Colunm Address to $\overline{WE}$ Delay Time	53	-	60	-	65	-	ns	8
44	tCSR	$\overline{CAS}$ Set-up Time(CBR Cycle)	5	-	5	-	5	-	ns	
45	tCHR	$\overline{CAS}$ Hold Time (CBR Cycle)	10	-	10	-	10	-	ns	
46	tRPC	$\overline{RAS}$ to $\overline{CAS}$ Precharge Time	5	-	5	-	5	-	ns	
47	tCPT	$\overline{CAS}$ Precharge Time (CBR Counter Test)	20	-	25	-	25	-	ns	
48	tROH	$\overline{RAS}$ Hold Time Reference to $\overline{OE}$	0	-	0	-	0	-	ns	
49	tOEA	$\overline{OE}$ Access Time	-	15	-	18	-	20	ns	
50	tOED	$\overline{OE}$ to Data Delay	15	-	15	-	15	-	ns	
51	tOEZ	Output Buffer Turn Off Delay Time	0	13	0	15	0	15	ns	
52	tOEH	$\overline{OE}$ Command Hold Time	10	-	10	-	10	-	ns	
53	tCPWD	$\overline{WE}$ Delay Time from $\overline{CAS}$ Precharge	35	-	40	-	45	-	ns	
54	tRHCP	$\overline{RAS}$ Hold Time from $\overline{CAS}$ Precharge	35	-	40	-	45	-	ns	8
55	tWRP	$\overline{WE}$ to $\overline{RAS}$ Precharge Time (CBR Cycle)	10	-	10	-	10	-	ns	
56	tWRH	$\overline{WE}$ to $\overline{RAS}$ Hold Time(CBR Cycle)	10	-	10	-	10	-	ns	
57	tWTS	Write Command Set-up (Test Mode In)	10	-	10	-	10	-	µs	
58	tWTH	Write Command Hold (Test Mode In)	10	-	10	-	10	-	ns	
59	tRASS	$\overline{RAS}$ Pulse Width (Self Refresh Cycle)	100	-	100	-	100	-	µs	
60	tRPS	$\overline{RAS}$ Precharge Time (Self Refresh Cycle)	90	-	110	-	130	-	ns	
61	tCHS	$\overline{CAS}$ Hold Time (Self Refresh Cycle)	-50	-	-50	-	-50	-	ns	

AC CHARACTERISTICS IN TEST MODE

NOTE 13

#	SYMBOL	PARAMETER	HY51V16400BJ/T/R/SLJ/SLT/SLR						UNIT	NOTE
			-60		-70		-80			
			MIN.	MAX.	MIN.	MAX.	MIN.	MAX.		
1	tRC	Random Read or Write Cycle Time	105	-	135	-	155	-	ns	
2	tRWC	Read-Modify-Write Cycle Time	165	-	185	-	205	-	ns	
3	tPC	Fast Page Mode Cycle Time	45	-	50	-	55	-	ns	
4	tPRWC	Fast Page Mode Read-Modify-Write Cycle Time	90	-	95	-	105	-	ns	
5	tRAC	Access Time From $\overline{RAS}$	-	65	-	75	-	85	ns	4,9,10
6	tCAC	Access Time From $\overline{CAS}$	-	20	-	23	-	25	ns	4,9
7	tAA	Access Time From Column Address	-	35	-	40	-	45	ns	4,10
8	tCPA	Access Time From $\overline{CAS}$ Precharge	-	40	-	45	-	50	ns	4
13	tRAS	$\overline{RAS}$ Pulse Width	65	10K	75	10K	85	10K	ns	
14	tRASP	$\overline{RAS}$ Pulse Width(Fast Page Mode)	65	200K	75	200K	85	200K	ns	
15	tRSH	$\overline{RAS}$ Hold Time	20	-	23	-	25	-	ns	
16	tCSH	$\overline{CAS}$ Hold Time	65	-	75	-	85	-	ns	
17	tCAS	$\overline{CAS}$ Pulse Width	20	10K	23	10K	25	10K	ns	
27	tRAL	Column Address to $\overline{RAS}$ Lead Time	35	-	40	-	45	-	ns	
41	tCWD	$\overline{CAS}$ to $\overline{WE}$ Delay Time	43	-	48	-	50	-	ns	8
42	tRWD	$\overline{RAS}$ to $\overline{WE}$ Delay Time	88	-	100	-	110	-	ns	8
43	tAWD	Column Address to $\overline{WE}$ Delay Time	58	-	65	-	70	-	ns	8
49	tOEA	$\overline{OE}$ Access Time	-	20	-	20	-	25	ns	
50	tOED	$\overline{OE}$ to Data Delay	20	-	20	-	25	-	ns	
52	tOEH	$\overline{OE}$ Command Hold Time	15	-	15	-	15	-	ns	

NOTE:

1. An intial pause of 200μs is required after power-up followed by any 8 $\overline{RAS}$ only or $\overline{CAS}$-before-$\overline{RAS}$ refresh cycle before proper device operaion is achieved.
2. If $\overline{RAS}$=Vss during power-up, this device could begin an active cycle. This condition results in higher current than necessary which is demanded from the power supply during power-up. It is recommended that $\overline{RAS}$ and $\overline{CAS}$ track with Vcc during power-up or be held at a valid VIH in order to minimize the power-up current.
3. VIH(min.) and VIL(max.) are reference levels for measuring timing of input signals. Also, transition times are measured between VIH(min.) and VIL(max.), and are assumed to be 5ns for all inputs.
4. Measured with a load equivalent to 100pF and VOH=2.0V (Iout=2mA), VOL=0.8V (Iout=2mA).
5. tOFF(max.) and tOEZ define the time at which the output achieves the open circuit condition and is not referenced to output voltage levels.
6. Either tRCH or tRRH must be satisfied for a read cycle.
7. These Parameters are referenced to $\overline{CAS}$ leading edge in early write cycles and $\overline{WE}$ leading edge in Read-Modify-Write cycles.
8. tWCS, tRWD, tCWD, tAWD and tCPWD are not restrictive operating parameters. They are included in the data sheet as electrical parameters only. If tWCS≥tWCS(min.), the cycle is an early write cycle and data output will remain open circuit (high impedance) through the entire cycle. If tRWD≥tRWD(min.), tCWD≥tCWD(min.), tAWD≥tAWD(min.), and tCPWD≥tCPWD(min.), the cycle is a Read-Modify-Write cycle and data will contain data read from the selected cell. If neither of the above sets of conditions is satisfied, the condition of the data out(at access time) is indetermined.
9. Operation within the tRCD(max.) limit insured that tRAC(max.) can be met. tRCD(max.) is specified point only. If tRCD is greater than the specified tRCD(max.) limit, then access time is controlled by tAA.
10. Operation within the tRAD(max.) limit insures that tRAC(max.) can be met. tRAD(max.) is specified as a reference point only. If tRAD is greater than the specified tRAD(max.) limit, then access time is controlled by tCAC.
11. tREF(max.)=256ms is applied to SL-Parts.
12. A burst of 4096 $\overline{CAS}$-before-$\overline{RAS}$ refresh cycles must be executed within 64ms(256ms for SL-part) after exiting self refresh.
13. These specifications are applied to the Test Mode.

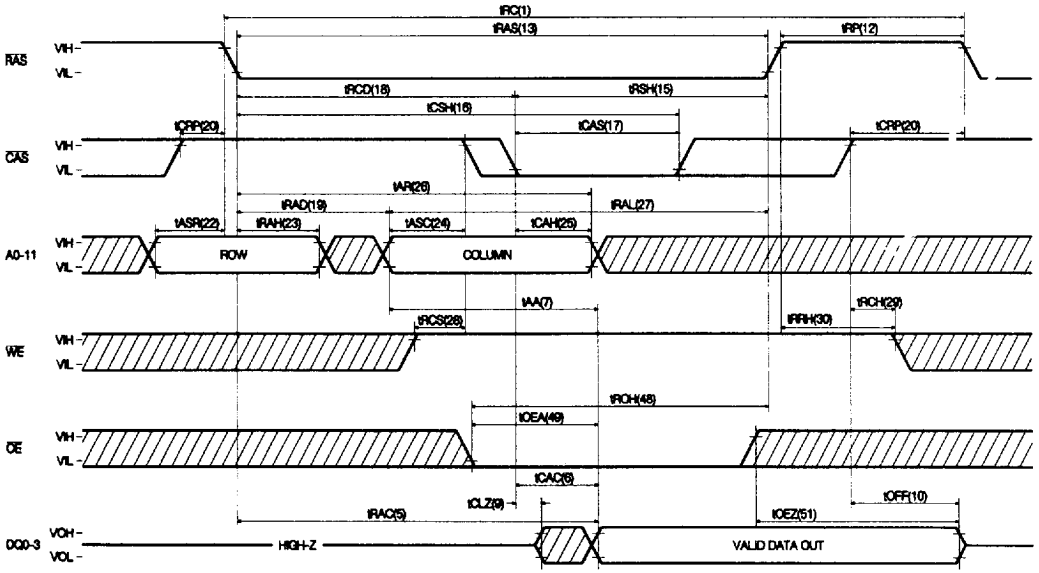
CAPACITANCE

(TA=25°C, Vcc=3.3V±10%, Vss=0V, f=1MHz, unless otherwise noted.)

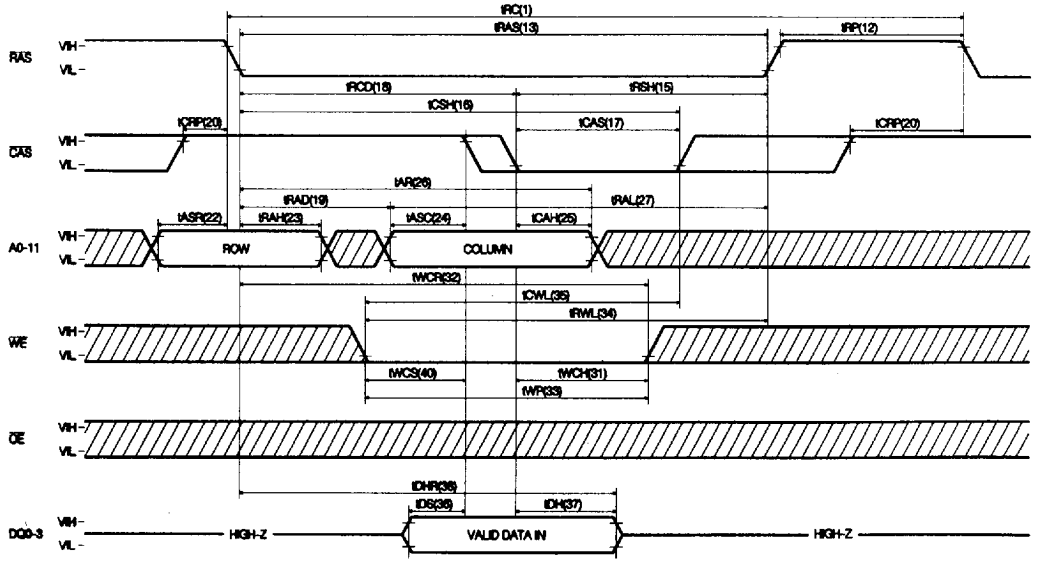
SYMBOL	PARAMETER	TYP.	MAX.	UNIT
CIN1	Input Capacitance (A0-A11)	-	5	pF
CIN2	Input Capacitance ($\overline{RAS}$, $\overline{CAS}$, $\overline{WE}$, $\overline{OE}$)	-	7	pF
CDQ	Data Input/Output Capacitance (DQ0 - 3)	-	7	pF

TIMING DIAGRAM

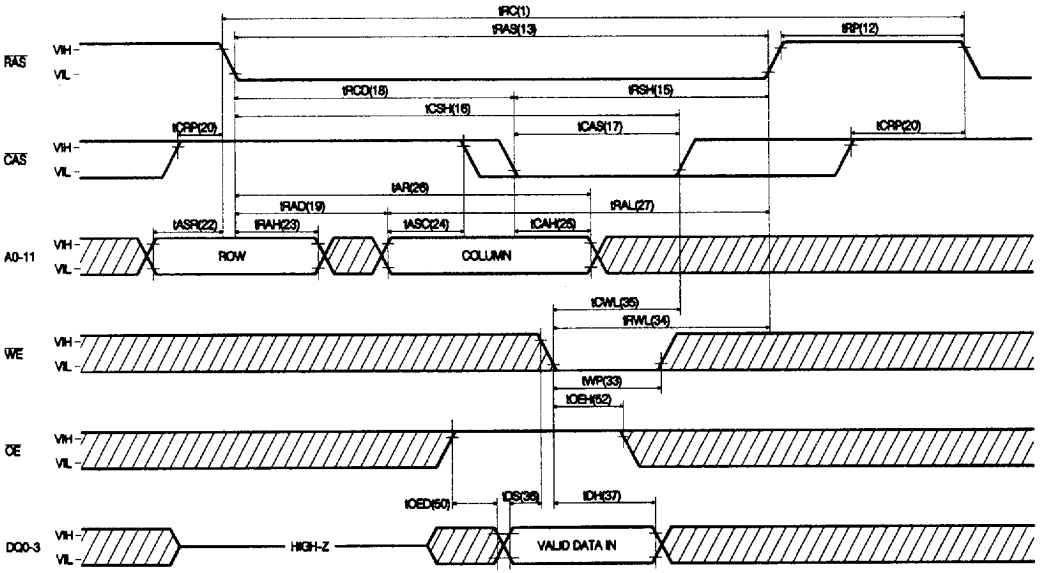
READ CYCLE



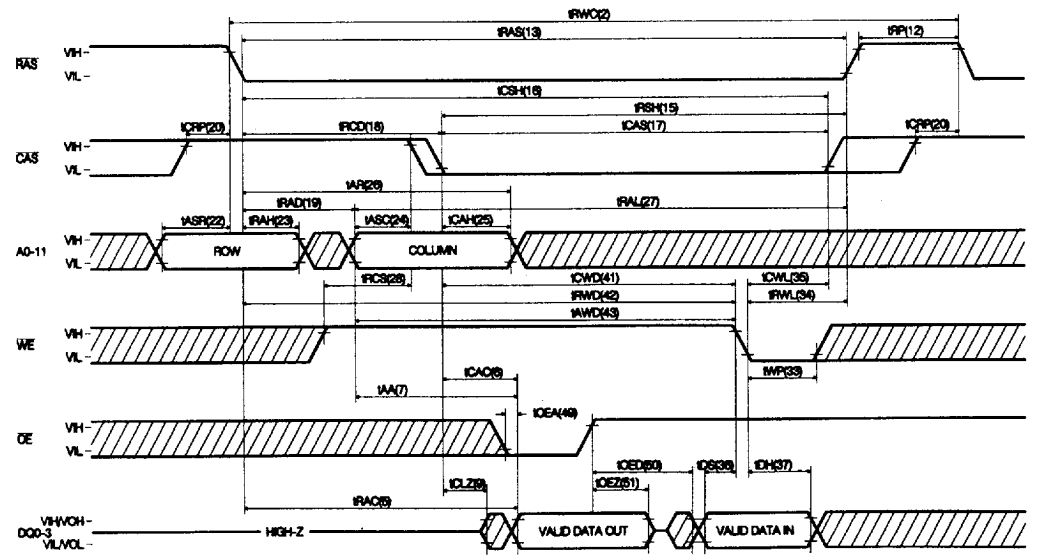
EARLY WRITE CYCLE



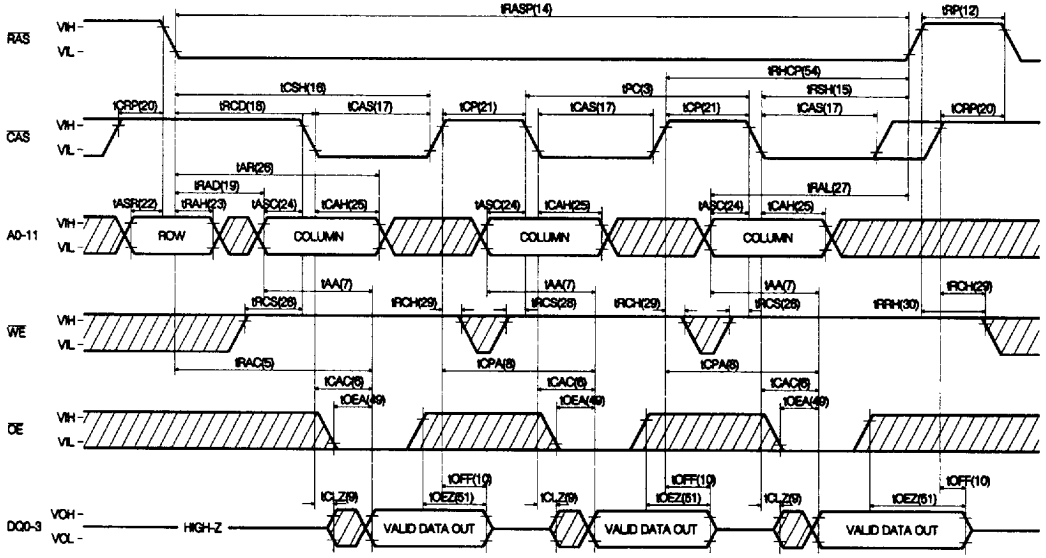
WRITE CYCLE ($\overline{OE}$ CONTROLLED WRITE)



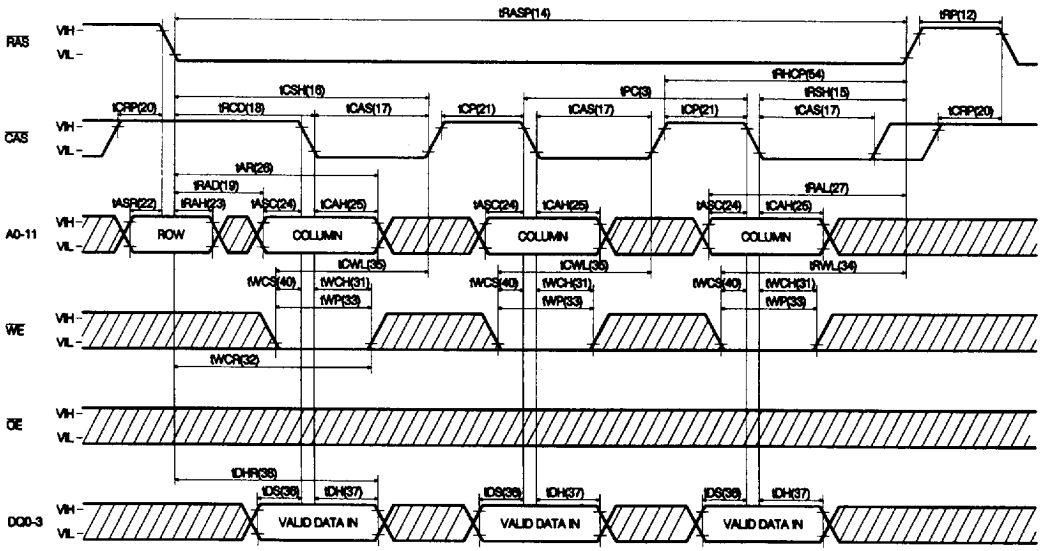
READ-MODIFY-WRITE CYCLE



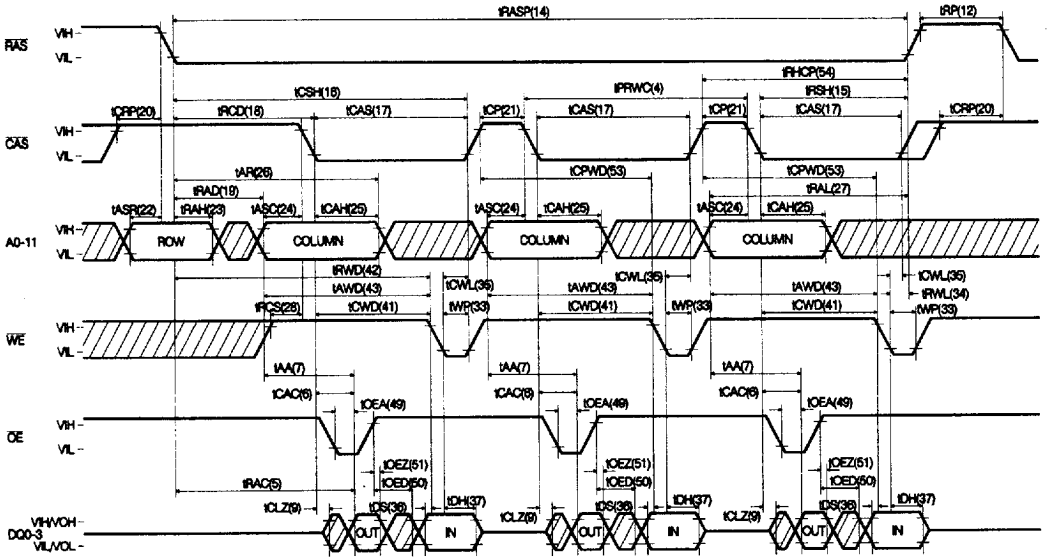
FAST PAGE MODE READ CYCLE



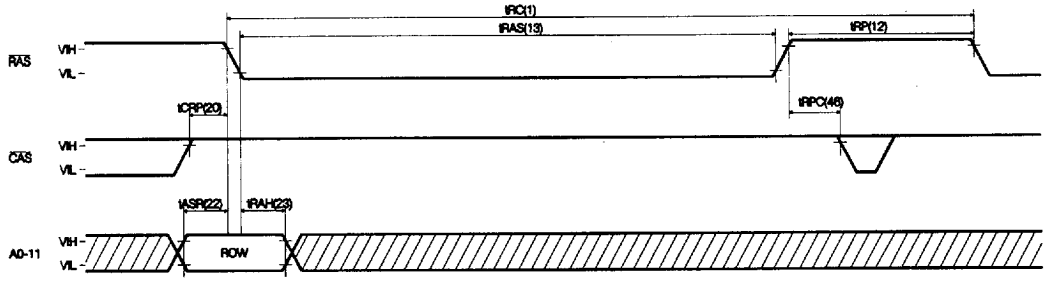
FAST PAGE MODE EARLY WRITE CYCLE



FAST PAGE MODE READ-MODIFY-WRITE CYCLE

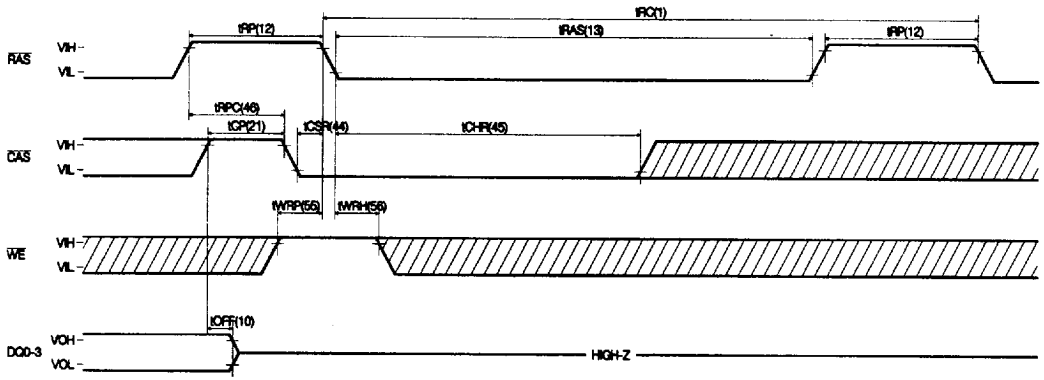


RAS-ONLY REFRESH CYCLE



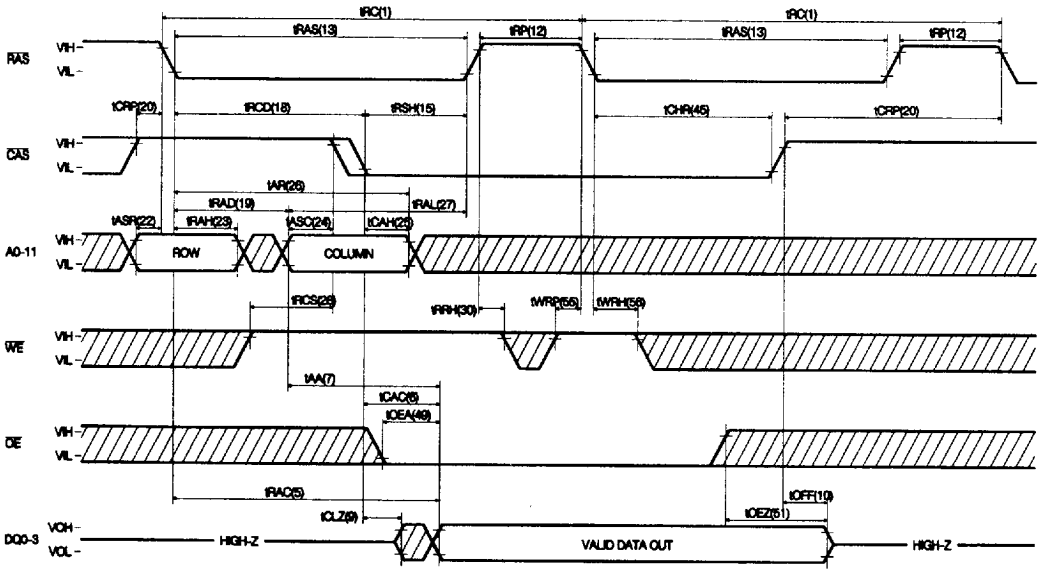
NOTE : $\overline{OE}$ and $\overline{WE}$ = "H" or "L"

CAS-BEFORE-RAS REFRESH CYCL

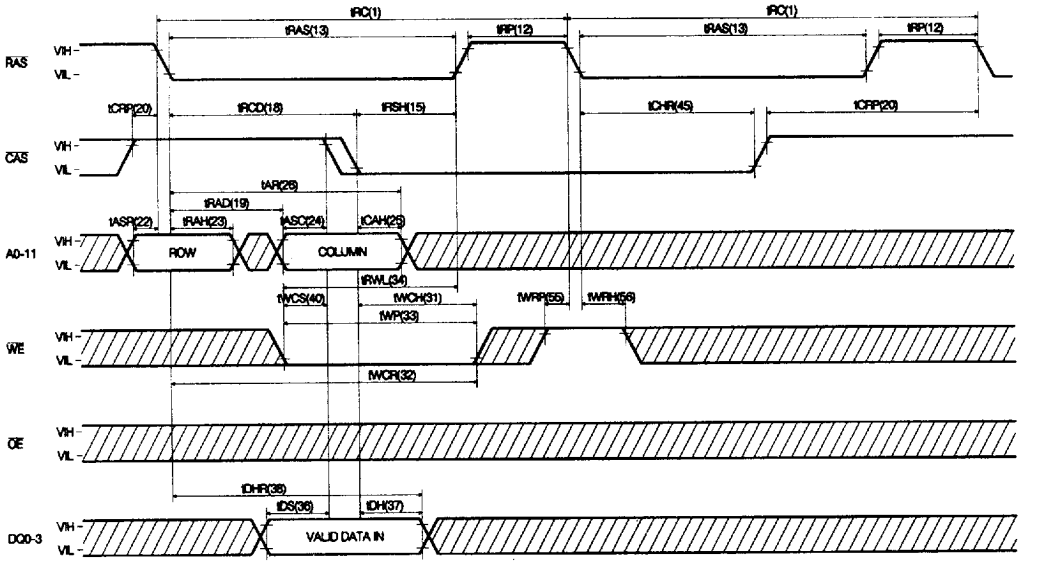


NOTE : A0-11 and OE = "H" or "L"

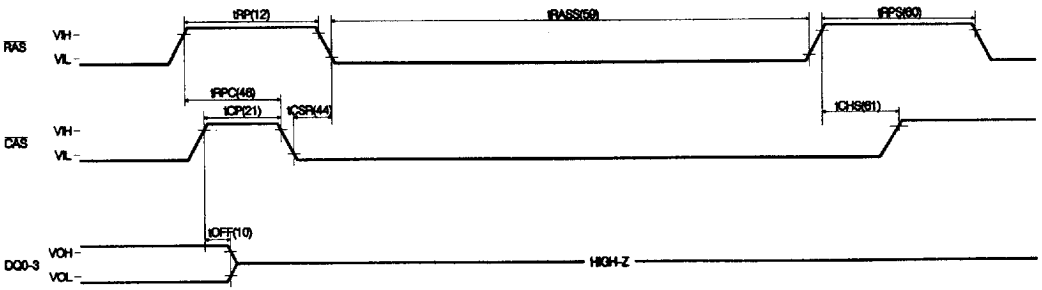
HIDDEN REFRESH CYCLE (READ)



HIDDEN REFRESH CYCLE (WRITE)

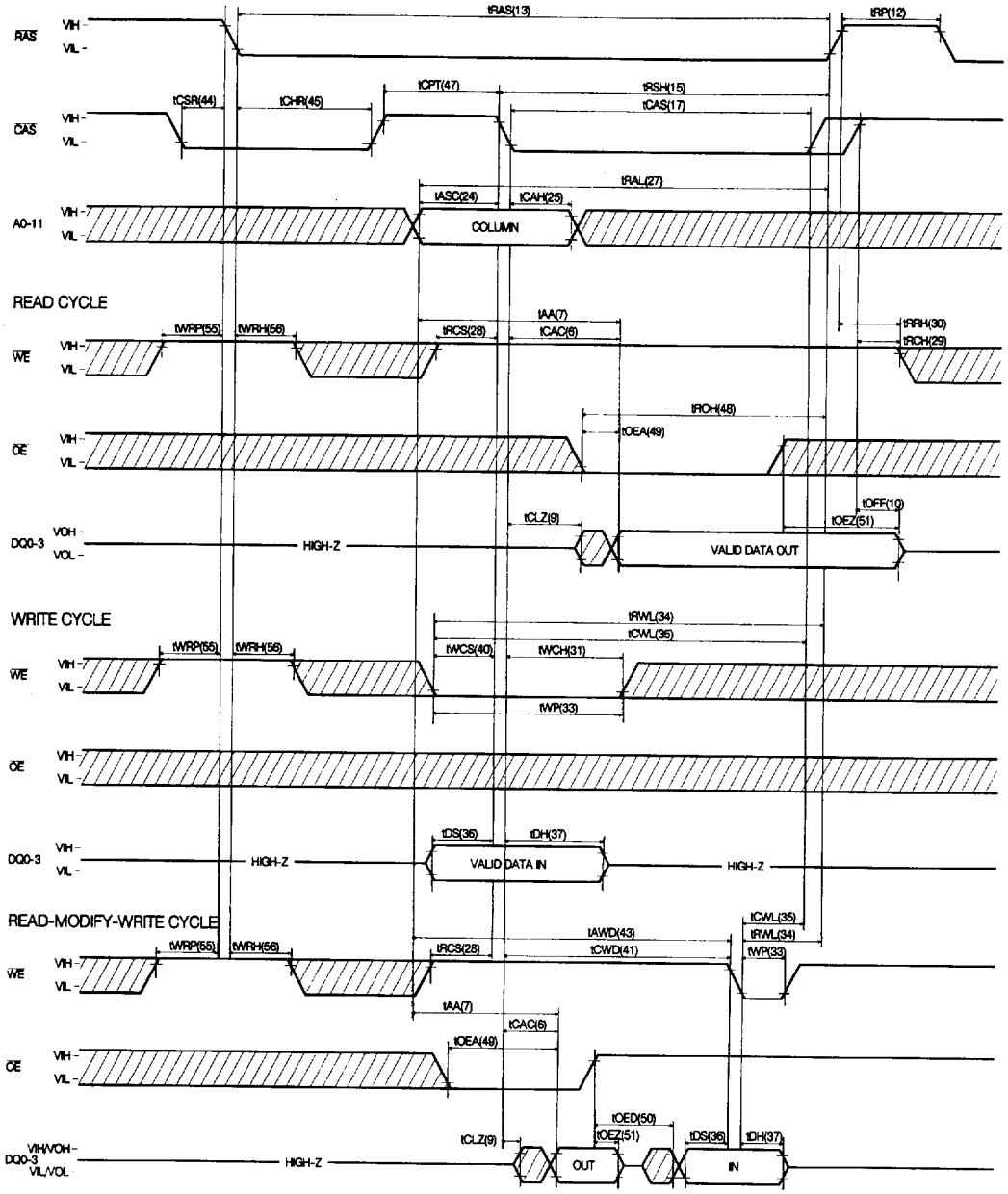


CAS-BEFORE-RAS REFRESH COUNTER TEST CYCLE



NOTE : A0-11, $\overline{OE}$ and $\overline{WE}$ = "H" or "L"

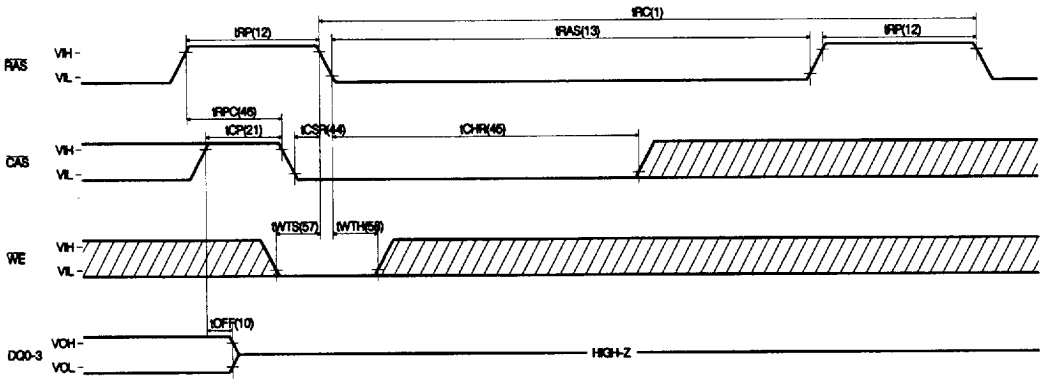
CAS-BEFORE-RAS REFRESH COUNTER TEST CYCLE



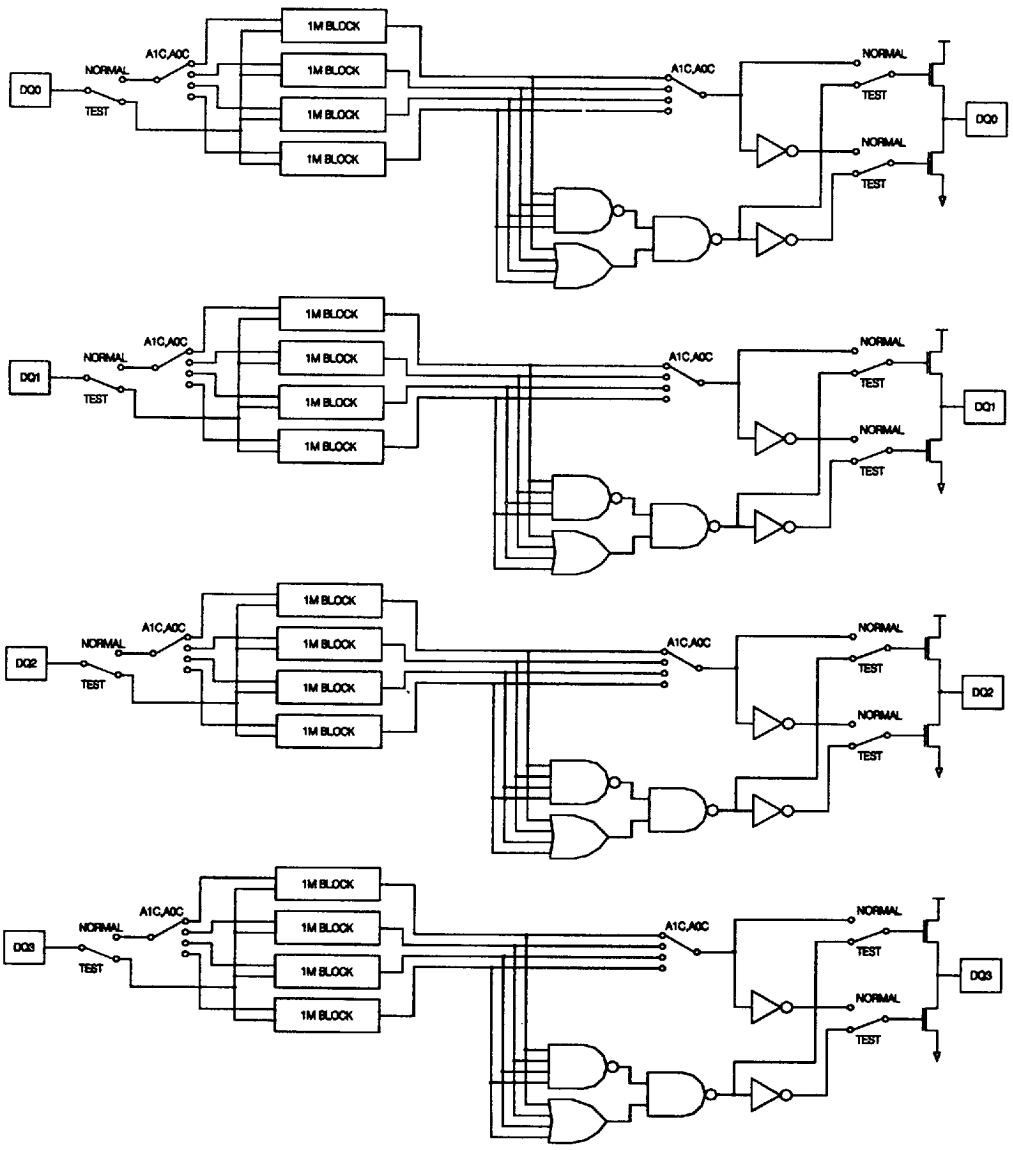
TEST MODE

The HY51V16400B is a DRAM organized 4,194,304×4-bit. It is internally organized 1,048,576×16-bit. In Test Mode, data are written into 16 sectors (Each is composed of 1M bits) in parallel and retrived the same way. Column address A0 and A1 are not used. If, upon reading, 4-bit data from 4 sectors connected to one DQ pin are equal (all "1"s or "0"s), the DQ pin indicates a "1". If they are not equal, the DQ pin indicates a "0". Belowing shows the timing diagram of the HY51V16400B to enter Test Mode. In Test Mode, the 4M×4 DRAM can be tested as if it were a 1M×4 DRAM. $\overline{WE}$, $\overline{CAS}$-before-$\overline{RAS}$ cycle(Test Mode In Cycle)puts the HY51V16400B into Test Mode and $\overline{CAS}$-before-$\overline{RAS}$ or $\overline{RAS}$-only refresh cycle puts it back into Normal Mode. In Test Mode, $\overline{WE}$, $\overline{CAS}$-before-$\overline{RAS}$ cycle shall be used for the refresh operation. The Test Mode function reduces test time (1/4 in case of N test pattern).

TEST MODE IN CYCLE

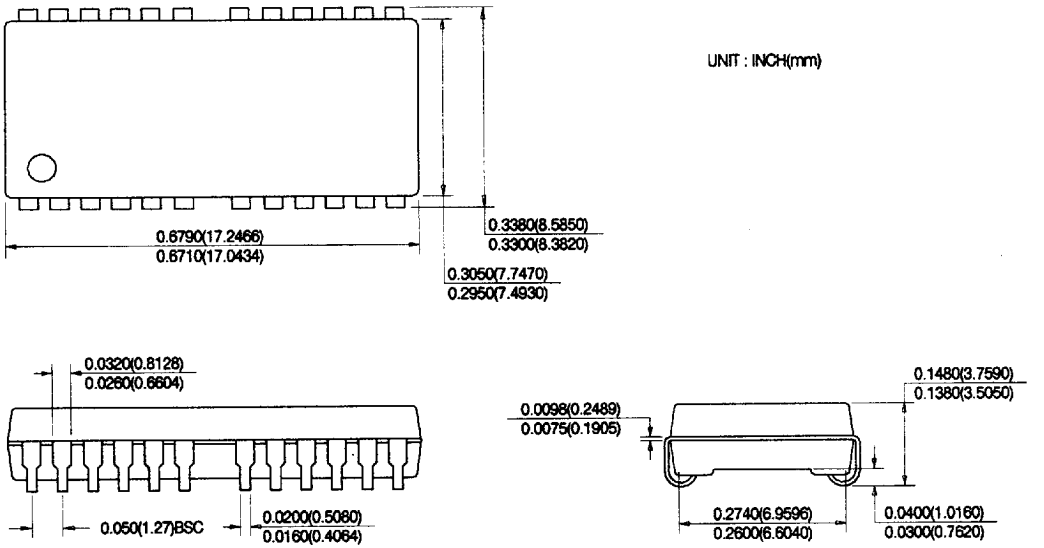


BLOCK DIAGRAM IN TEST MODE

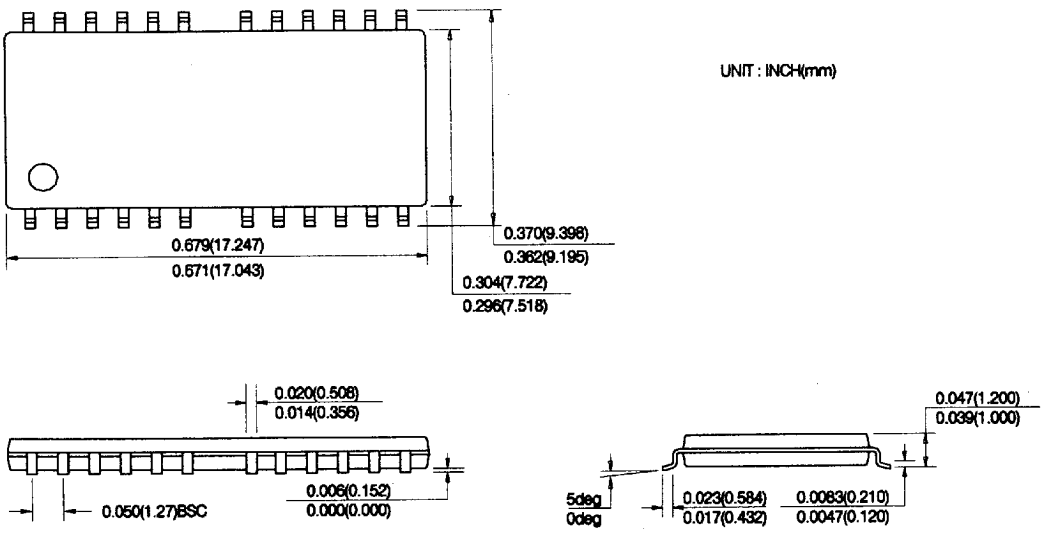


PACKAGE INFORMATION

300 mil 24/26 pin Small Outline J-form Package (J)



300 mil 24/26 pin Thin Small Outline Package (T) (R)



ORDERING INFORMATION

PART NO	SPEED	POWER	PACKAGE
HY51V16400BJ	60/70/80		SOJ
HY51V16400BSL	60/70/80	SL-part	SOJ
HY51V16400BT	60/70/80		TSOP-II
HY51V16400BSLT	60/70/80	SL-part	TSOP-II
HY51V16400BR	60/70/80		TSOP-II(R)
HY51V16400BSLR	60/70/80	SL-part	TSOP-II(R)