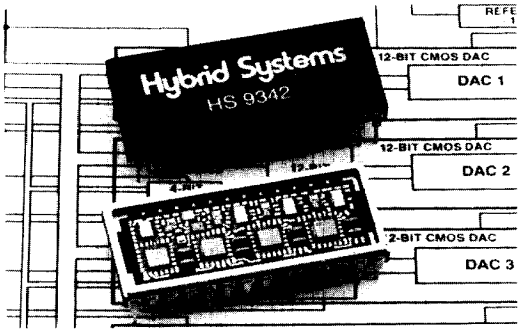
HS9342

12-BIT, SPACE SAVING QUAD DAC

FEATURES

- Four 12-bit DAC's in a single package
- Low power: 750 mW typ, 1.12W max
- Double buffered input structure for μP interface
- 5μsec max voltage output settling to 0.012% for a 10V step
- Accepts internal or external voltage reference



DESCRIPTION

The HS9342 consists of four complete 12-bit digital-to-analog converters with a bipolar voltage output and reference circuit in a single 28-pin hybrid package. The design features latched monolithic 12-bit CMOS DACs, which provides low power and high reliability. The HS9342 is ideally suited for applications where board space is at a premium.

The HS9342 is packaged in a 28-pin DIP and is specified for operation from 0°C to 70°C for commercial grades and −55°C to +125°C for military grades. Full screening to MIL-STD-883C is available.

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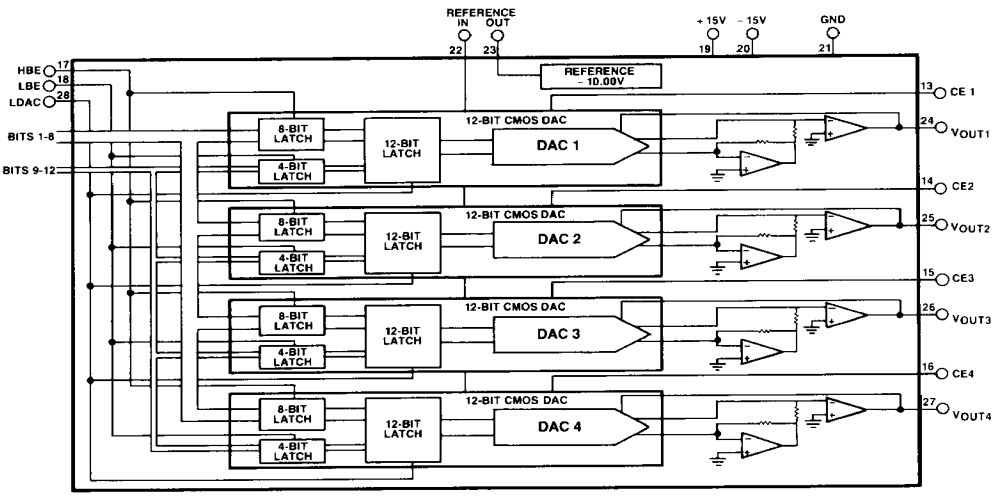
FUNCTIONAL DIAGRAM



SPECIFICATIONS

(Typical @ +25°C with V_{DD} = +15V, V_{EE} = −15V unless otherwise noted)

MODEL	HS 9342
DIGITAL INPUTS	
Resolution	12-Bits
V_{IH} Logic Level[1]	2.4V min
V_{IL} Logic Level[1]	0.8V max
I_{IN} Input Current (0V V_{IN} V_{DD})	1.0 μA typ, 4.0 μA max
Data Set-Up Time[2]	250 nsec min
Strobe Width[3]	250 nsec min
Data Hold Time	0 nsec min
Four-Quadrant Coding	Offset Binary
VOLTAGE REFERENCE INPUT	
Input Voltage Range	±10V
Input Impedance	1.2 KΩ min, 2.5 KΩ nom, 3.8 KΩ max
VOLTAGE REFERENCE OUTPUT (REF OUT connected to REF IN)	
Output Voltage Error	±10 mV max
Noise Voltage (peak-to-peak wide band)	100 μV typ, 200 μV max
Total Available Current (T_{min} to T_{max}) (I_{REF} + I_{EXT})	15 mA min, 20 mA max
Voltage Drift (T_{min} to T_{max})[4]	5 ppm/°C typ, 8 ppm/°C max
Current (Available for External Use)	12 mA max
STATIC DAC PERFORMANCE	
Integral Linearity[5]	±¼ LSB typ, ±½ LSB max
Differential Linearity	±¼ LSB typ, ±1 LSB max
Bipolar Zero Error	±1 LSB typ, ±2 LSB max
Gain Error	±2 LSB typ, ±4 LSB max
Gain Error Matching	±3 LSB typ
DYNAMIC PERFORMANCE	
Small Signal Settling (to 0.012%)	2.0 μsec
Full Scale Settling (to 0.012%)	5.0 μsec
Slew Rate	8V/μsec min, 12V/μsec typ
LDAC to Output Delay	300 nsec
DRIFT (T_{min} to T_{max})	
Gain	10 ppm/°C typ, 15 ppm/°C max
Bipolar Zero	3 ppm/°C typ, 5 ppm/°C max
Integral Linearity	0.5 ppm/°C typ, 1 ppm/°C max
Differential Linearity	0.5 ppm/°C typ, 1 ppm/°C max
POWER SUPPLY	
V_{DD}	+13.5V to +16.5V
V_{EE}	−13.5V to −16.5V
I_{DD} @ V_{DD} = +15V ±5%[6]	20 mA typ, 35 mA max
I_{EE} @ V_{EE} = −15V ±5%[6]	25 mA typ, 35 mA max
I_{DD} @ V_{DD} = +15V ±5%[7]	20 mA typ, 35 mA max
I_{EE} @ V_{EE} = −15V ±5%[7]	22 mA typ, 30 mA max
Power Supply Rejection	V_{DD} 0.002%/% typ V_{EE} 0.001%/% typ
POWER DISSIPATION	
	675 mW typ, 900 mW max[6] 530 mW typ, 825 mW max[7]
TEMPERATURE RANGE	
Operating	
C-Model	0°C to 70°C
B-Model	−55°C to +125°C
Storage	−65°C to +150°C
PACKAGE	
28-Pin Ceramic	
9342B	Case A
9342C	Case A
θ_{JA}	30°C/W

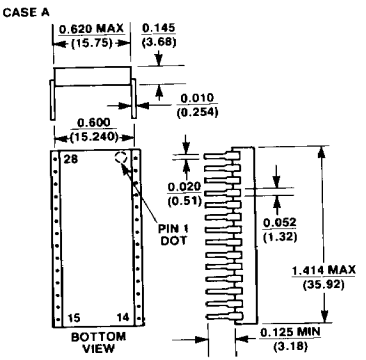
NOTES:
1. Digital inputs must never exceed V_{DD} or go below −0.3V
2. Data must be stable before strobe (HBE, LBE, LDAC) goes to 0
3. CE, LBE, HBE, LDAC (All strobes are level triggered.)
4. The error band is defined graphically in terms of a box (voltage vertically, temperature horizontally) whose diagonals extend from 25°C to T_{max} and 25°C to T_{min}, with a slope equal to the stated temperature coefficient.
5. Integral linearity, for this product, is measured as the arithmetic mean value of the magnitudes of the greatest positive deviation and the greatest negative deviation from the theoretical value of any combination.
6. Utilizing internal voltage reference
7. Applying external voltage reference to REF IN

ABSOLUTE MAXIMUM RATINGS (Referenced to GND)

(Exceeding any *one* of these parameters may cause permanent damage to the unit)

V_{DD}	−0.3V to +18V
V_{EE}	+0.3V to −18V
V_{IN} (Bits 1-12, LBE, HBE, $\overline{CE}_{1-4}$)	−0.3V to (V_{DD} + 0.3V)
$V_{REF\ IN}$	±20V
DAC Outputs	Infinite short to GND
Reference Output	Infinite short to GND
Temperature Soldering Duration	10 sec @ 300°C
Power Dissipation	1800 mW

PACKAGE OUTLINE



PIN ASSIGNMENTS

PIN	FUNCTION	PIN	FUNCTION
1	BIT 1 (MSB)	15	$\overline{CE}$3
2	BIT 2	16	$\overline{CE}$4
3	BIT 3	17	HBE
4	BIT 4	18	LBE
5	BIT 5	19	+15V
6	BIT 6	20	−15V
7	BIT 7	21	GND
8	BIT 8	22	REF IN
9	BIT 9	23	REF OUT
10	BIT 10	24	V_{OUT1}
11	BIT 11	25	V_{OUT2}
12	BIT 12 (LSB)	26	V_{OUT3}
13	$\overline{CE}$1	27	V_{OUT4}
14	$\overline{CE}$2	28	LDAC

APPLICATIONS INFORMATION

The HS 9342 has been designed for maximum flexibility in connecting to bus oriented systems. The HS 9342 is designed to accept 12-bit parallel data or 8-bit/4-bit data formatted by control pins CE1-CE4, HBE, LBE, and LDAC. The input registers are double buffered allowing any primary register to be updated independently of the others. Loading of any given primary register is accomplished by bringing the appropriate chip enable low, HBE and LBE high. All four DAC outputs are simultaneously updated by a single LDAC command.

CONTROL FUNCTIONS

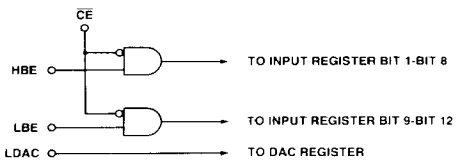
PIN	DEFINITION	FUNCTION
$\overline{CEX}$	Chip Enable X	Enables the primary register of DACX for loading data in conjunction with the HBE and/or LBE function.
HBE	High Byte Enable	Enables the 8 MSBs to be loaded into the primary register of the DACs selected by $\overline{CEX}$.
LBE	Low Byte Enable	Enables the 4 LSBs to be loaded into the primary register of the DACs selected by $\overline{CEX}$.
LDAC	Load DAC	Loads all data in all four DACs, from the primary to secondary registers and updates all DAC outputs.

HS 9342 TRUTH TABLE

$\overline{CE1}$	$\overline{CE2}$	$\overline{CE3}$	$\overline{CE4}$	HBE	LBE	LDAC	DESCRIPTION
0	1	1	1	1	1	0	Enables 1st rank of DAC1
1	0	1	1	1	1	0	Enables 1st rank of DAC2
1	1	0	1	1	1	0	Enables 1st rank of DAC3
1	1	1	0	1	1	0	Enables 1st rank of DAC4
X	X	X	X	X	X	1	Load DACs 1-4 secondary register from primary registers.

NOTE:
By enabling HBE, LBE and LDAC, all latches become transparent on selected DACs

CONTROL LOGIC

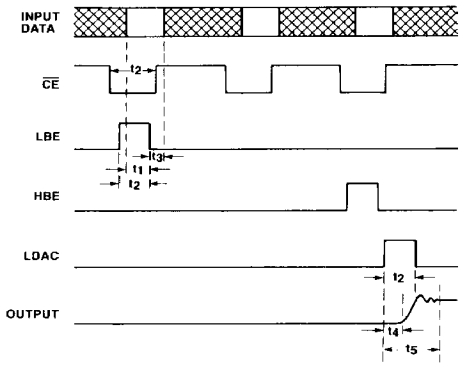


NOTE:
The transfer from input register to DAC register can be performed without Enabling Chip.

STROBE LOGIC

STROBE	FUNCTION
0	Data Latched (Held)
1	Data Changing (Transfer)

TIMING DIAGRAM



TIME AXIS NOT TO SCALE. ALL STROBES ARE LEVEL TRIGGERED.
t_1: Data Setup Time. Time data must be stable before strobe (byte enable/LDAC) goes to "0", t_1 (min) = 250 nsec.
t_2: Strobe Width. t_2 (min) = 250 nsec. (CE, LBE, HBE, LDAC).
t_3: Hold Time. Time data must be stable after strobe goes to "0", t_3 = 0 nsec.
t_4: Delay from LDAC to Output. t_4 = 300 nsec
t_5: Settling Time. 5μ sec (typical).

NOTE:
Minimum common active time for $\overline{CE}$ and any byte enable is 250 nsec.

TRANSFER CHARACTERISTICS

DIGITAL INPUT CODE			ANALOG OUTPUT VOLTAGE	
0000	0000	0000	−10.000V	−FULL SCALE
0100	0000	0000	− 5.000V	−1/2 SCALE
1000	0000	0000	0.000V	ZERO
1000	0000	0001	+ 4.88 mV	+1 LSB
1100	0000	0000	+ 5.000V	+1/2 SCALE
1111	1111	1111	+ 9.9951V	+FULL SCALE-1 LSB

REFERENCE CIRCUITRY

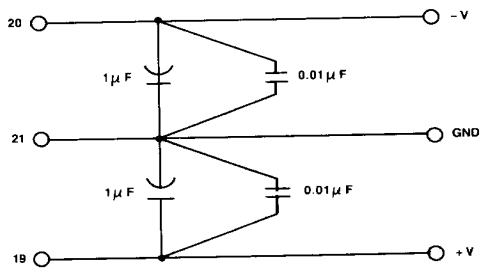
The HS 9342 is supplied with a precision internal −10V reference, trimmed to within ±5 millivolts. The reference is available for external use and can supply up to 8 mA of output current. In normal operation, the REF OUT (Pin 23) is connected to REF IN (Pin 22)[1]. The REF OUT is then fully loaded. If a system reference is available, an external reference may be used. It is recommended if an external reference is used, it supplies a minimum of 8 milliamps of current.

1. The reference is then fully loaded.

APPLICATIONS INFORMATION (continued)

POWER SUPPLY CONSIDERATION

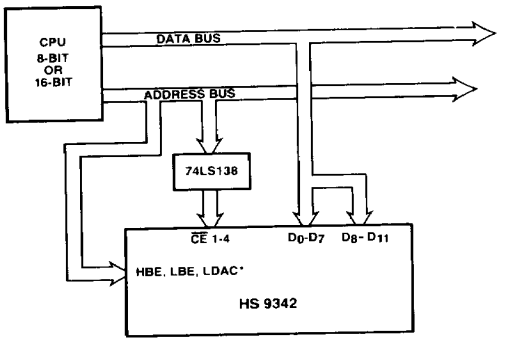
Power supplies used for the HS 9342 should be selected for low noise operation. In particular, they should be free of high frequency noise. Decoupling capacitors are recommended on all power supply pins located as close to the unit as possible. Suitable decoupling capacitors are 1 μF tantulum type in parallel with 0.1 μF disc ceramic type.



Recommended Power Supply Bypass

MICROPROCESSOR INTERFACE

The HS 9342 control logic is easily interfaced to most common microprocessors. Due to the 8-Bit/4-Bit input architecture, no external latches are required for interface to 8- or 16-bit bus structures.



**For 8-Bit Data Bus, HBE and LBE addressed separately as high byte and low byte. For 16-Bit Data Bus, HBE and LBE are tied together and addressed as one word.*

HS 9342 8- or 16-Bit Bus Interface

CAUTION: ESD (Electro-Static Discharge) sensitive device. Permanent damage may occur when unconnected devices are subjected to high energy electro-static fields. Unused devices must be stored in conductive foam or shunts. Protective foam should be discharged to the destination socket before devices are removed. Devices should be handled at static safe workstations only. Unused digital inputs must be grounded or tied to the logic supply voltage. Unless otherwise noted, the voltage at any digital input should never exceed the supply voltage by more than 0.5 volts or go below −0.5 volts. If this condition cannot be maintained, limit input current on digital inputs by using series resistors or contact Hybrid Systems for technical assistance.

ORDERING INFORMATION

MODEL	TEMPERATURE RANGE	DESCRIPTION
HS 9342C	0°C to 70°C	12-Bit, QUAD DAC
HS 9342B	−55°C to +125°C	12-Bit, QUAD DAC 883C

Specifications subject to change without notice.