HB56D236 Series - HITACHI/ LOGIC/ARRAYS/MEM

2,097,152-Word × 36-Bit High Density Dynamic RAM Module

The HB56D236 is a 2M × 36 dynamic RAM module, mounted 16 pieces of 4-Mbit DRAM (HM514400AS/ALS) sealed in SOJ package and 8 pieces of 1-Mbit DRAM (HM511000AT/ALT) sealed in TSOP package. An outline of the HB56D236 is 72-pin single in-line package. Therefore, the HB56D236 makes high density mounting possible without surface mount technology. The HB56D236 provides common data inputs and outputs. Decoupling capacitors are mounted beneath each SOJ or beside each TSOP but only on the one side of its module board.

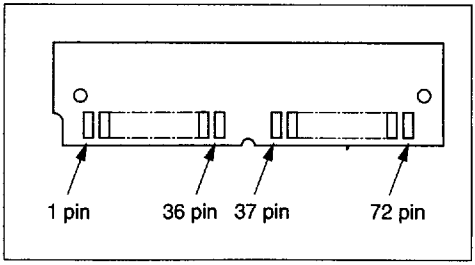
Features

- 72-pin single in-line package
  - Lead pitch: 1.27 mm
- Single 5 V (± 5%) supply
- High speed
  - Access time: 70 ns/80 ns/100 ns (max)
- Low power dissipation
  - Active mode: 6.20 W/5.57 W/4.94 W (max)
  - Standby mode: 252 mW (max)
- Fast page mode capability
- 1,024 refresh cycle/16 ms, 128 ms (L-version)
- 2 variations of refresh
  - $\overline{\text{RAS}}$-only refresh
  - $\overline{\text{CAS}}$-before-$\overline{\text{RAS}}$ refresh
- TTL compatible

Ordering Information

Type No.	Access time	Package	Contact pad
HB56D236BS-7A/7AL	70 ns	72-pin SIP socket type	gold
HB56D236BS-8A/8AL	80 ns		
HB56D236BS-10A/10AL	100 ns		
HB56D236SBS-7A/7AL	70 ns	72-pin SIP socket type	solder
HB56D236SBS-8A8AL	80 ns		
HB56D236SBS-10A/10AL	100 ns		

Pin Arrangement



HB56D236 Series

Pin Arrangement (cont)

Pin No.	Pin name	Pin No.	Pin name	Pin No.	Pin name	Pin No.	Pin name
1	V_{SS}	19	NC	37	DQ17	55	DQ12
2	DQ0	20	DQ4	38	DQ35	56	DQ30
3	DQ18	21	DQ22	39	V_{SS}	57	DQ13
4	DQ1	22	DQ5	40	$\overline{CAS0}$	58	DQ31
5	DQ19	23	DQ23	41	$\overline{CAS2}$	59	V_{CC}
6	DQ2	24	DQ6	42	$\overline{CAS3}$	60	DQ32
7	DQ20	25	DQ24	43	$\overline{CAS1}$	61	DQ14
8	DQ3	26	DQ7	44	$\overline{RAS0}$	62	DQ33
9	DQ21	27	DQ25	45	$\overline{RAS1}$	63	DQ15
10	V_{CC}	28	A7	46	NC	64	DQ34
11	NC	29	NC	47	$\overline{WE}$	65	DQ16
12	A0	30	V_{CC}	48	NC	66	NC
13	A1	31	A8	49	DQ9	67	PD1
14	A2	32	A9	50	DQ27	68	PD2
15	A3	33	$\overline{RAS3}$	51	DQ10	69	PD3
16	A4	34	$\overline{RAS2}$	52	DQ28	70	PD4
17	A5	35	DQ26	53	DQ11	71	NC
18	A6	36	DQ8	54	DQ29	72	V_{SS}

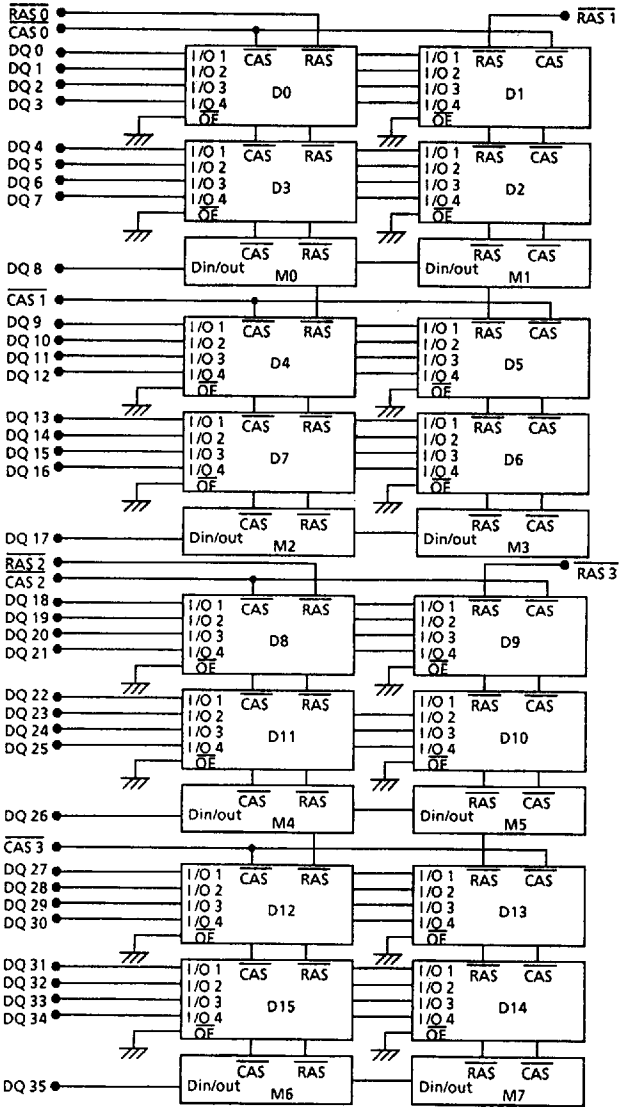
Pin Description

Pin name	Function
A0 – A9	Address input
A0 – A9	Refresh address input
DQ0 – DQ35	Data-in/data out
$\overline{CAS0}$ – $\overline{CAS3}$	Column address strobe
$\overline{RAS0}$ – $\overline{RAS3}$	Row address strobe
$\overline{WE}$	Read/write enable
V_{CC}	Power supply (+5 V)
V_{SS}	Ground
PD1 – PD4	Presence detect pin
NC	No connection

Presence Detect Pin Arrangement

		HB56D236BS/SBS		
Pin No	Pin name	70 ns	80 ns	100 ns
67	PD1	NC	NC	NC
68	PD2	NC	NC	NC
69	PD3	V_{SS}	NC	V_{SS}
70	PD4	NC	V_{SS}	V_{SS}

Block Diagram



Absolute Maximum Ratings

Parameter		Symbol	Value	Unit
Voltage on any pin relative to V_{SS}	Input	Vin	−1.0 to +7.0	V
	Output	Vout	−1.0 to +7.0	V
Supply voltage relative to V_{SS}		V_{CC}	−1.0 to +7.0	V
Short circuit output current		Iout	50	mA
Power dissipation		P_T	12	W
Operating temperature		Topr	0 to +70	°C
Storage temperature		Tstg	−55 to +125	°C

Recommended DC Operating Conditions (Ta = 0 to +70°C)

Parameter	Symbol	Min	Typ	Max	Unit	Note
Supply voltage	V_{SS}	0	0	0	V	
	V_{CC}	4.75	5.0	5.25	V	1
Input high voltage	V_{IH}	2.4	—	5.5	V	1
Input low voltage	V_{IL}	−1.0	—	0.8	V	1

Note: 1. All voltage referenced to V_{SS}.

Capacitance (Ta = 25°C, V_{CC} = 5 V ± 5%)

Parameter	Symbol	Typ	Max	Unit	Notes
Input capacitance (Address)	C_{I1}	—	161	pF	1
Input capacitance ($\overline{WE}$)	C_{I2}	—	193	pF	1
Input capacitance ($\overline{RAS}$, $\overline{CAS}$)	C_{I3}	—	62	pF	1
Output capacitance (DQ0 – DQ7, DQ9 – DQ16 DQ18 – DQ25, DQ27 – DQ34)	$C_{I/O1}$	—	29	pF	1,2
Output capacitance (DQ8, DQ17, DQ26, DQ35)	$C_{I/O2}$	—	39	pF	1,2

Notes: 1. Capacitance measured with Boonton Meter or effective capacitance measuring method.
2. $\overline{CAS}$ = V_{IH} to disable Dout.

DC Characteristics (Ta = 0 to +70°C, V_{CC} = 5 V ± 5%, V_{SS} = 0 V)

		HB56D236BS/SBS								
		-7A/7AL		-8A/8AL		-10A/10AL				
Parameter	Symbol	Min	Max	Min	Max	Min	Max	Unit	Test conditions	Notes
Operating current	I_{CC1}	—	1180	—	1060	—	940	mA	t_{RC} = min	1, 2
Standby current	I_{CC2}	—	48	—	48	—	48	mA	TTL interface $\overline{RAS}$, $\overline{CAS}$ = V_{IH} Dout = High-Z	
		—	24	—	24	—	24	mA	CMOS interface $\overline{RAS}$, $\overline{CAS}$ ≥ V_{CC} – 0.2 V Dout = High-Z	
Standby current (L-version)		—	4.8	—	4.8	—	4.8	mA	CMOS interface $\overline{RAS}$, $\overline{CAS}$ = V_{IH} $\overline{WE}$, address, Din = V_{IH} or V_{IL}, Dout = High-Z	4
$\overline{RAS}$-only refresh current	I_{CC3}	—	1180	—	1020	—	900	mA	t_{RC} = min	2
Standby current	I_{CC5}	—	120	—	120	—	120	mA	$\overline{RAS}$ = V_{IH}, $\overline{CAS}$ = V_{IL} Dout = enable	1
$\overline{CAS}$-before-$\overline{RAS}$ refresh current	I_{CC6}	—	1140	—	1020	—	900	mA	t_{RC} = min	
Page mode current	I_{CC7}	—	1140	—	980	—	900	mA	t_{PC} = min	1, 3
Battery back up operation current (CBR refresh) (L-version)	I_{CC10}	—	7.2	—	7.2	—	7.2	mA	t_{RC} = 125 µs, t_{RAS} ≤ 1 µs $\overline{WE}$ = V_{IH}, $\overline{CAS}$ = V_{IL} address, Din = V_{IH} or V_{IL} Dout = High-Z	4
Input leakage current	I_{LI}	–10	10	–10	10	–10	10	µA	0 V ≤ Vin ≤ 7 V	
Output leakage current	I_{LO}	–10	10	–10	10	–10	10	µA	0 V ≤ Vout ≤ 7 V Dout = disable	
Output high voltage	V_{OH}	2.4	V_{CC}	2.4	V_{CC}	2.4	V_{CC}	V	High Iout = –5 mA	
Output low voltage	V_{OL}	0	0.4	0	0.4	0	0.4	V	Low Iout = 4.2 mA	

Notes:
1. I_{CC} depends on output load condition when the device is selected. I_{CC} max is specified at the output open condition.
2. Address can be changed once or less while $\overline{RAS}$ = V_{IL}.
3. Address can be changed once or less while $\overline{CAS}$ = V_{IH}.
4. V_{CC} –0.2 V ≤ V_{IH} ≤ 6.5 V, 0 V ≤ V_{IL} ≤ 0.2 V.

AC Characteristics ($Ta = 0$ to $+70°C$, $V_{CC} = 5\ V \pm 5\%$, $V_{SS} = 0\ V$) *1, *12

Read, Write and Refresh Cycle (Common parameters)

		HB56D236							
		-7A/7AL		-8A/8AL		-10A/10AL			
Parameter	Symbol	Min	Max	Min	Max	Min	Max	Unit	Notes
Random read or write cycle time	t_{RC}	130	—	160	—	190	—	ns	
$\overline{RAS}$ precharge time	t_{RP}	50	—	70	—	80	—	ns	
$\overline{RAS}$ pulse width	t_{RAS}	70	10000	80	10000	100	10000	ns	
$\overline{CAS}$ pulse width	t_{CAS}	20	10000	25	10000	25	10000	ns	
Row address setup time	t_{ASR}	0	—	0	—	0	—	ns	
Row address hold time	t_{RAH}	10	—	12	—	15	—	ns	
Column address setup time	t_{ASC}	0	—	0	—	0	—	ns	
Column address hold time	t_{CAH}	15	—	20	—	20	—	ns	
$\overline{RAS}$ to $\overline{CAS}$ delay time	t_{RCD}	20	50	22	55	25	75	ns	8
$\overline{RAS}$ to column address delay time	t_{RAD}	15	35	17	40	20	55	ns	9
$\overline{RAS}$ hold time	t_{RSH}	20	—	25	—	25	—	ns	
$\overline{CAS}$ hold time	t_{CSH}	70	—	80	—	100	—	ns	
$\overline{CAS}$ to $\overline{RAS}$ precharge time	t_{CRP}	10	—	10	—	10	—	ns	
Transition time (rise and fall)	t_T	3	50	3	50	3	50	ns	7
Refresh period	t_{REF}	—	16	—	16	—	16	ms	15

Read Cycle

		HB56D236							
		-7A/7AL		-8A/8AL		-10A/10AL			
Parameter	Symbol	Min	Max	Min	Max	Min	Max	Unit	Notes
Access time from $\overline{RAS}$	t_{RAC}	—	70	—	80	—	100	ns	2, 3
Access time from $\overline{CAS}$	t_{CAC}	—	20	—	25	—	25	ns	3, 4
Access time from address	t_{AA}	—	35	—	40	—	45	ns	3, 5

Read Cycle (cont)

		HB56D236							
		-7A/7AL		-8A/8AL		-10A/10AL			
Parameter	**Symbol**	**Min**	**Max**	**Min**	**Max**	**Min**	**Max**	**Unit**	**Notes**
Read command setup time	t_{RCS}	0	—	0	—	0	—	ns	
Read command hold time to $\overline{CAS}$	t_{RCH}	0	—	0	—	0	—	ns	
Read command hold time to $\overline{RAS}$	t_{RRH}	10	—	10	—	10	—	ns	
Column address to $\overline{RAS}$ lead time	t_{RAL}	35	—	40	—	45	—	ns	
Output buffer turn-off time	t_{OFF}	—	20	—	20	—	25	ns	6

Write Cycle

		HB56D236							
		-7A/7AL		-8A/8AL		-10A/10AL			
Parameter	**Symbol**	**Min**	**Max**	**Min**	**Max**	**Min**	**Max**	**Unit**	**Notes**
Write command setup time	t_{WCS}	0	—	0	—	0	—	ns	10
Write command hold time	t_{WCH}	15	—	20	—	20	—	ns	
Write command pulse width	t_{WP}	10	—	15	—	20	—	ns	
Data-in setup time	t_{DS}	0	—	0	—	0	—	ns	11
Data-in hold time	t_{DH}	15	—	20	—	20	—	ns	11

Refresh Cycle

		HB56D236							
		-7A/7AL		-8A/8AL		-10A/10AL			
Parameter	**Symbol**	**Min**	**Max**	**Min**	**Max**	**Min**	**Max**	**Unit**	**Notes**
$\overline{CAS}$ setup time ($\overline{CAS}$-before-$\overline{RAS}$ refresh cycle)	t_{CSR}	10	—	10	—	10	—	ns	
$\overline{CAS}$ hold time ($\overline{CAS}$-before-$\overline{RAS}$ refresh cycle)	t_{CHR}	15	—	20	—	20	—	ns	
$\overline{RAS}$ precharge to $\overline{CAS}$ hold time	t_{RPC}	10	—	10	—	10	—	ns	

Fast Page Mode Cycle

Parameter	Symbol	HB56D236 -7A/7AL Min	-7A/7AL Max	-8A/8AL Min	-8A/8AL Max	-10A/10AL Min	-10A/10AL Max	Unit	Notes
Fast page mode cycle time	t_{PC}	50	—	55	—	55	—	ns	
Fast page mode $\overline{CAS}$ precharge time	t_{CP}	10	—	10	—	10	—	ns	
Fast page mode $\overline{RAS}$ pulse width	t_{RASC}	70	100000	80	100000	100	100000	ns	13
Access time from $\overline{CAS}$ precharge	t_{ACP}	—	45	—	50	—	50	ns	14
$\overline{RAS}$ hold time from $\overline{CAS}$ precharge	t_{RHCP}	45	—	50	—	50	—	ns	

Notes:
1. AC measurements assume $t_T = 5$ ns.
2. Assumes that $t_{RCD} \leq t_{RCD}$ (max) and $t_{RAD} \leq t_{RAD}$ (max). If t_{RCD} or t_{RAD} is greater than the maximum recommended value shown in this table, t_{RAC} exceeds the value shown.
3. Measured with a load circuit equivalent to 2TTL loads and 100 pF.
4. Assumes that $t_{RCD} \geq t_{RCD}$ (max), $t_{RAD} \leq t_{RAD}$ (max).
5. Assumes that $t_{RCD} \leq t_{RCD}$ (max), $t_{RAD} \geq t_{RAD}$ (max).
6. t_{OFF} (max) is defined as the time at which the output achieves the open circuit condition and is not referenced to output voltage levels.
7. V_{IH} (min) and V_{IL} (max) are reference levels for measuring timing of input signals. Also, transition times are measured between V_{IH} and V_{IL}.
8. Operation with the t_{RCD} (max) limit insures that t_{RAC} (max) can be met, t_{RCD} (max) is specified as a reference point only, if t_{RCD} is greater than the specified t_{RCD} (max) limit, then access time is controlled exclusively by t_{CAC}.
9. Operation with the t_{RAD} (max) limit insures that t_{RAC} (max) can be met, t_{RAD} (max) is specified as a reference point only, if t_{RAD} is greater than the specified t_{RAD} (max) limit, then access time is controlled exclusively by t_{AA}.
10. Early write cycle only ($t_{WCS} \geq t_{WCS}$ (min)).
11. These parameters are referenced to $\overline{CAS}$ leading edge in an early write cycle.
12. An initial pause of 100 µs is required after power up followed by a minimum of eight initialization cycles ($\overline{RAS}$-only refresh cycle or $\overline{CAS}$-before-$\overline{RAS}$ refresh cycle).
13. t_{RASC} is determined by $\overline{RAS}$ pulse width in fast page mode cycles.
14. Access time is determined by the longer of t_{AA} or t_{CAC} or t_{ACP}.
15. t_{REF} is determined by 1,024 refresh cycles.

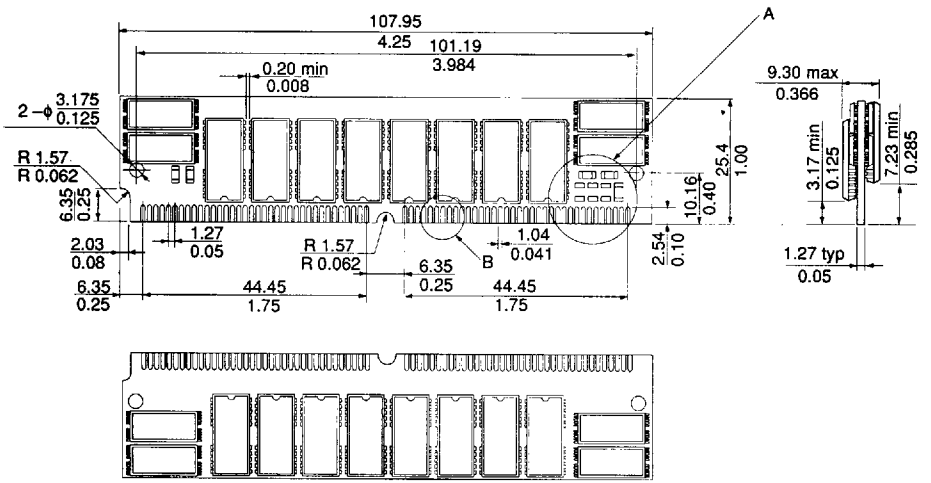
Timing Waveforms

- Refer to the HM514400A data sheet.
- The HB56D236 writes data only in early write cycle ($t_{WCS} \geq t_{WCS}$ (min)) Delayed write cycle is not available. $\overline{OE}$ pin is fixed to V_{SS}.

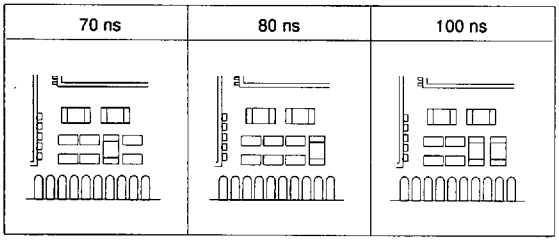
Physical Outline

Unit: mm/inch

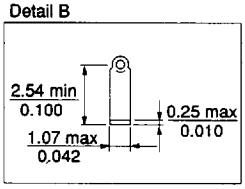
HB56D236BS/SBS Series



Detail A



Detail B



Note: Following the specification of the contact pads.

Part No.	Contact pad
HB56D236BS-XX	gold
HB56D236SBS-XX	solder