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# HB52D48GB-F

32 MB Unbuffered SDRAM Micro DIMM  
4-Mword  $\times$  64-bit, 100 MHz Memory Bus, 1-Bank Module  
(4 pcs of 4 M  $\times$  16 components)  
PC100 SDRAM

# HITACHI

ADE-203-1149 (Z)  
Preliminary  
Rev. 0.0  
Jan. 13, 2000

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## Description

The HB52D48GB is a 4M  $\times$  64  $\times$  1 banks Synchronous Dynamic RAM Micro Dual In-line Memory Module (Micro DIMM), mounted 4 pieces of 64-Mbit SDRAM (HM5264165FTT) sealed in TSOP package and 1 piece of serial EEPROM (2-kbit EEPROM) for Presence Detect (PD). An outline of the product is 144-pin Zig Zag Dual tabs socket type compact and thin package. Therefore, it makes high density mounting possible without surface mount technology. It provides common data inputs and outputs. Decoupling capacitors are mounted beside TSOP on the module board.

## Features

- 144-pin Zig Zag Dual tabs socket type (dual lead out)
  - Outline: 38.00 mm (Length)  $\times$  30.00 mm (Height)  $\times$  3.80 mm (Thickness)
  - Lead pitch: 0.50 mm
- 3.3 V power supply
- Clock frequency: 100 MHz (max)
- LVTTTL interface
- Data bus width:  $\times$  64 Non parity
- Single pulsed  $\overline{\text{RAS}}$
- 4 Banks can operates simultaneously and independently
- Burst read/write operation and burst read/single write operation capability
- Programmable burst length : 1/2/4/8/full page
- 2 variations of burst sequence
  - Sequential (BL = 1/2/4/8/full page)
  - interleave (BL = 1/2/4/8)

Preliminary: The specification of this device are subject to change without notice. Please contact your nearest Hitachi's Sales Dept. regarding specification.



**Front side**
**Back side**

Pin No.	Signal name	Pin No.	Signal name	Pin No.	Signal name	Pin No.	Signal name
1	V <sub>SS</sub>	73	NC	2	V <sub>SS</sub>	74	CK1
3	DQ0	75	V <sub>SS</sub>	4	DQ32	76	V <sub>SS</sub>
5	DQ1	77	NC	6	DQ33	78	NC
7	DQ2	79	NC	8	DQ34	80	NC
9	DQ3	81	V <sub>CC</sub>	10	DQ35	82	V <sub>CC</sub>
11	V <sub>CC</sub>	83	DQ16	12	V <sub>CC</sub>	84	DQ48
13	DQ4	85	DQ17	14	DQ36	86	DQ49
15	DQ5	87	DQ18	16	DQ37	88	DQ50
17	DQ6	89	DQ19	18	DQ38	90	DQ51
19	DQ7	91	V <sub>SS</sub>	20	DQ39	92	V <sub>SS</sub>
21	V <sub>SS</sub>	93	DQ20	22	V <sub>SS</sub>	94	DQ52
23	DQMB0	95	DQ21	24	DQMB4	96	DQ53
25	DQMB1	97	DQ22	26	DQMB5	98	DQ54
27	V <sub>CC</sub>	99	DQ23	28	V <sub>CC</sub>	100	DQ55
29	A0	101	V <sub>CC</sub>	30	A3	102	V <sub>CC</sub>
31	A1	103	A6	32	A4	104	A7
33	A2	105	A8	34	A5	106	A13 (BA0)
35	V <sub>SS</sub>	107	V <sub>SS</sub>	36	V <sub>SS</sub>	108	V <sub>SS</sub>
37	DQ8	109	A9	38	DQ40	110	A12 (BA1)
39	DQ9	111	A10 (AP)	40	DQ41	112	A11
41	DQ10	113	V <sub>CC</sub>	42	DQ42	114	V <sub>CC</sub>
43	DQ11	115	DQMB2	44	DQ43	116	DQMB6
45	V <sub>CC</sub>	117	DQMB3	46	V <sub>CC</sub>	118	DQMB7
47	DQ12	119	V <sub>SS</sub>	48	DQ44	120	V <sub>SS</sub>
49	DQ13	121	DQ24	50	DQ45	122	DQ56
51	DQ14	123	DQ25	52	DQ46	124	DQ57
53	DQ15	125	DQ26	54	DQ47	126	DQ58
55	V <sub>SS</sub>	127	DQ27	56	V <sub>SS</sub>	128	DQ59
57	NC	129	V <sub>CC</sub>	58	NC	130	V <sub>CC</sub>
59	NC	131	DQ28	60	NC	132	DQ60

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## Front side

## Back side

Pin No.	Signal name	Pin No.	Signal name	Pin No.	Signal name	Pin No.	Signal name
61	CK0	133	DQ29	62	CKE0	134	DQ61
63	V <sub>CC</sub>	135	DQ30	64	V <sub>CC</sub>	136	DQ62
65	$\overline{RE}$	137	DQ31	66	$\overline{CE}$	138	DQ63
67	$\overline{W}$	139	V <sub>SS</sub>	68	NC	140	V <sub>SS</sub>
69	$\overline{S0}$	141	SDA	70	NC	142	SCL
71	NC	143	V <sub>CC</sub>	72	NC	144	V <sub>CC</sub>

## Pin Description

### Pin name

### Function

A0 to A11

Address input

- Row address A0 to A11
- Column address A0 to A7

A12/A13

Bank select address BA1, BA0

DQ0 to DQ63

Data-input/output

$\overline{S0}$

Chip select

$\overline{RE}$

Row address asserted bank enable

$\overline{CE}$

Column address asserted

$\overline{W}$

Write enable

DQMB0 to DQMB7

Byte input/output mask

CK0/CK1

Clock input

CKE0

Clock enable

SDA

Data-input/output for serial PD

SCL

Clock input for serial PD

V<sub>CC</sub>

Power supply

V<sub>SS</sub>

Ground

NC

No connection

**Serial PD Matrix\*<sup>1</sup>**

Byte No.	Function described	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0	Hex value	Comments
0	Number of bytes used by module manufacturer	1	0	0	0	0	0	0	0	80	128
1	Total SPD memory size	0	0	0	0	1	0	0	0	08	256 byte
2	Memory type	0	0	0	0	0	1	0	0	04	SDRAM
3	Number of row addresses bits	0	0	0	0	1	1	0	0	0C	12
4	Number of column addresses bits	0	0	0	0	1	0	0	0	08	8
5	Number of banks	0	0	0	0	0	0	0	1	01	1
6	Module data width	0	1	0	0	0	0	0	0	40	64
7	Module data width (continued)	0	0	0	0	0	0	0	0	00	0 (+)
8	Module interface signal levels	0	0	0	0	0	0	0	1	01	LVTTTL
9	SDRAM cycle time (highest CE latency) 10 ns	1	0	1	0	0	0	0	0	A0	CL = 3
10	SDRAM access from Clock (highest CE latency) 6 ns	0	1	1	0	0	0	0	0	60	
11	Module configuration type	0	0	0	0	0	0	0	0	00	Non parity
12	Refresh rate/type	1	0	0	0	0	0	0	0	80	Normal (15.625 μs) Self refresh
13	SDRAM width	0	0	0	1	0	0	0	0	10	4M × 16
14	Error checking SDRAM width	0	0	0	0	0	0	0	0	00	—
15	SDRAM device attributes: minimum clock delay for back-to-back random column addresses	0	0	0	0	0	0	0	1	01	1 CLK
16	SDRAM device attributes: Burst lengths supported	1	0	0	0	1	1	1	1	8F	1, 2, 4, 8, full page
17	SDRAM device attributes: number of banks on SDRAM device	0	0	0	0	0	1	0	0	04	4
18	SDRAM device attributes: CE latency	0	0	0	0	0	1	1	0	06	2, 3
19	SDRAM device attributes: S latency	0	0	0	0	0	0	0	1	01	0

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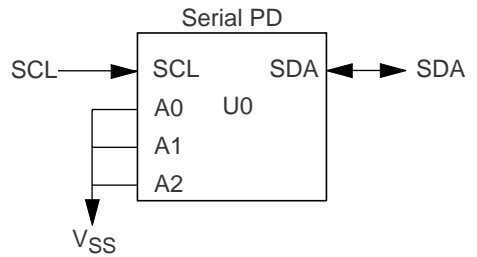
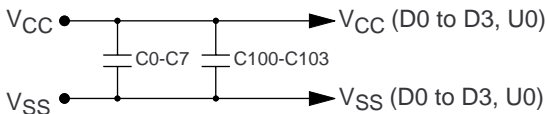
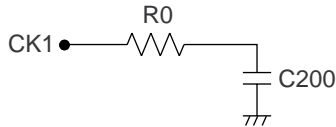
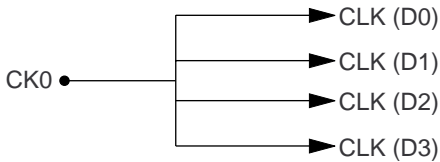
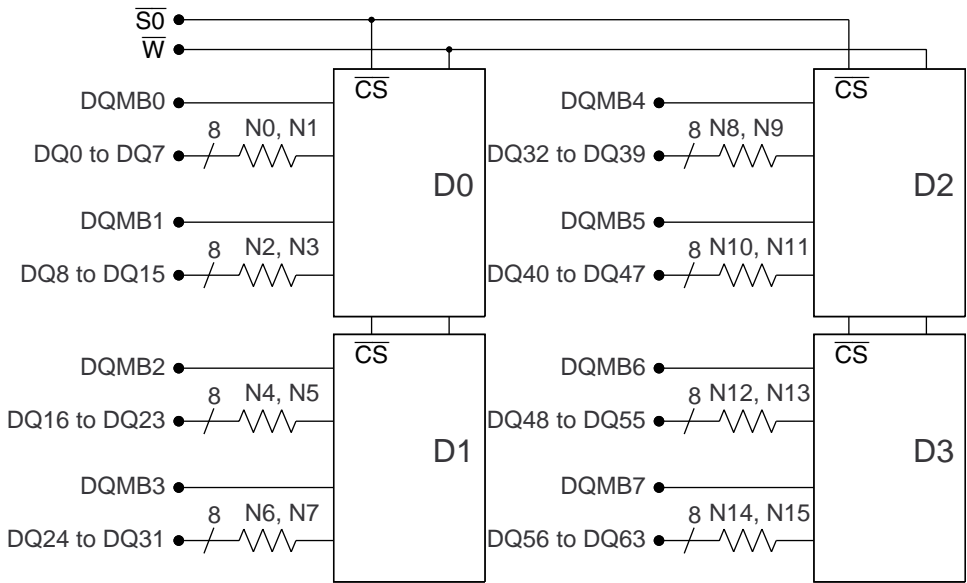
Byte No.	Function described	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0	Hex value	Comments
20	SDRAM device attributes: W latency	0	0	0	0	0	0	0	1	01	0
21	SDRAM module attributes	0	0	0	0	0	0	0	0	00	Unbuffer
22	SDRAM device attributes: General	0	0	0	0	1	1	1	0	0E	$V_{CC} \pm 10\%$
23	SDRAM cycle time (2nd highest $\overline{CE}$ latency) (-A6F/A6FL) 10 ns (-B6F/B6FL) 15 ns	1	0	1	0	0	0	0	0	A0	CL = 2
		1	1	1	1	0	0	0	0	F0	
24	SDRAM access from Clock (2nd highest $\overline{CE}$ latency) (-A6F/A6FL) 6 ns (-B6F/B6FL) 8 ns	0	1	1	0	0	0	0	0	60	
		1	0	0	0	0	0	0	0	80	
25	SDRAM cycle time (3rd highest $\overline{CE}$ latency) Undefined	0	0	0	0	0	0	0	0	00	
26	SDRAM access from Clock (3rd highest $\overline{CE}$ latency) Undefined	0	0	0	0	0	0	0	0	00	
27	Minimum row precharge time	0	0	0	1	0	1	0	0	14	20 ns
28	Row active to row active min	0	0	0	1	0	1	0	0	14	20 ns
29	$\overline{RE}$ to $\overline{CE}$ delay min	0	0	0	1	0	1	0	0	14	20 ns
30	Minimum $\overline{RE}$ pulse width	0	0	1	1	0	0	1	0	32	50 ns
31	Density of each bank on module	0	0	0	0	1	0	0	0	08	32M byte
32	Address and command signal input setup time	0	0	1	0	0	0	0	0	20	2 ns
33	Address and command signal input hold time	0	0	0	1	0	0	0	0	10	1 ns
34	Data signal input setup time	0	0	1	0	0	0	0	0	20	2 ns
35	Data signal input hold time	0	0	0	1	0	0	0	0	10	1 ns
36 to 61	Superset information	0	0	0	0	0	0	0	0	00	Future use
62	SPD data revision code	0	0	0	1	0	0	1	0	12	Rev. 1.2A
63	Checksum for bytes 0 to 62 (-A6F/A6FL) (-B6F/B6FL)	0	0	0	0	0	1	0	0	04	4
		0	1	1	1	0	1	0	0	74	116
64	Manufacturer's JEDEC ID code	0	0	0	0	0	1	1	1	07	HITACHI
65 to 71	Manufacturer's JEDEC ID code	0	0	0	0	0	0	0	0	00	
72	Manufacturing location	x	x	x	x	x	x	x	x	xx	*3 (ASCII-8bit code)

Byte No.	Function described	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0	Hex value	Comments
73	Manufacturer's part number	0	1	0	0	1	0	0	0	48	H
74	Manufacturer's part number	0	1	0	0	0	0	1	0	42	B
75	Manufacturer's part number	0	0	1	1	0	1	0	1	35	5
76	Manufacturer's part number	0	0	1	1	0	0	1	0	32	2
77	Manufacturer's part number	0	1	0	0	0	1	0	0	44	D
78	Manufacturer's part number	0	0	1	1	0	1	0	0	34	4
79	Manufacturer's part number	0	0	1	1	1	0	0	0	38	8
80	Manufacturer's part number	0	1	0	0	0	1	1	1	47	G
81	Manufacturer's part number	0	1	0	0	0	0	1	0	42	B
82	Manufacturer's part number	0	0	1	0	1	1	0	1	2D	—
83	Manufacturer's part number (-A6F/A6FL)	0	1	0	0	0	0	0	1	41	A
	(-B6F/B6FL)	0	1	0	0	0	0	1	0	42	B
84	Manufacturer's part number	0	0	1	1	0	1	1	0	36	6
85	Manufacturer's part number	0	1	0	0	0	1	1	0	46	F
86	Manufacturer's part number (L-version)	0	1	0	0	1	1	0	0	4C	L
	Manufacturer's part number	0	0	1	0	0	0	0	0	20	(Space)
87	Manufacturer's part number	0	0	1	0	0	0	0	0	20	(Space)
88	Manufacturer's part number	0	0	1	0	0	0	0	0	20	(Space)
89	Manufacturer's part number	0	0	1	0	0	0	0	0	20	(Space)
90	Manufacturer's part number	0	0	1	0	0	0	0	0	20	(Space)
91	Revision code	0	0	1	1	0	0	0	0	30	Initial
92	Revision code	0	0	1	0	0	0	0	0	20	(Space)
93	Manufacturing date	×	×	×	×	×	×	×	×	×	Year code (BCD)*4
94	Manufacturing date	×	×	×	×	×	×	×	×	×	Week code (BCD)*4
95 to 98	Assembly serial number	*6									
99 to 125	Manufacturer specific data	—									*5
126	Intel specification frequency	0	1	1	0	0	1	0	0	64	100 MHz
127	Intel specification CE# latency support	1	1	0	0	0	1	1	1	C7	CL = 2, 3
	(-A6F/A6FL)										
	(-B6F/B6FL)	1	1	0	0	0	1	0	1	C5	CL = 3

- Notes:
1. All serial PD data are not protected. 0: Serial data, “driven Low”, 1: Serial data, “driven High”  
These SPD are based on Intel specification (Rev.1.2A).
  2. Regarding byte32 to 35, based on JEDEC Committee Ballot JC42.5-97-119.
  3. Byte72 is manufacturing location code. (ex: In case of Japan, byte72 is 4AH. 4AH shows “J” on ASCII code.)
  4. Regarding byte93 and 94, based on JEDEC Committee Ballot JC42.5-97-135. BCD is “Binary Coded Decimal”.
  5. All bits of 99 through 125 are not defined (“1” or “0”).
  6. Bytes 95 through 98 are assembly serial number.



Block Diagram



Notes :

1. The SDA pull-up resistor is required due to the open-drain/open-collector output.
2. The SCL pull-up resistor is recommended because of the normal SCL line inactive "high" state.

- \* D0 to D3: HM5264165
- U0: 2-kbit EEPROM
- C0 to C7: 0.33  $\mu$ F
- C100 to C103: 0.1  $\mu$ F
- C200: 10 pF
- N0 to N15: Network resistors (10  $\Omega$ )
- R0: Resistor (10  $\Omega$ )

**Absolute Maximum Ratings**

Parameter	Symbol	Value	Unit	Note
Voltage on any pin relative to $V_{SS}$	$V_T$	-0.5 to $V_{CC} + 0.5$ ( $\leq 4.6$ (max))	V	1
Supply voltage relative to $V_{SS}$	$V_{CC}$	-0.5 to +4.6	V	1
Short circuit output current	$I_{out}$	50	mA	
Power dissipation	$P_T$	4.0	W	
Operating temperature	$T_{opr}$	0 to +65	°C	
Storage temperature	$T_{stg}$	-55 to +125	°C	

Note: 1. Respect to  $V_{SS}$ .

**DC Operating Conditions ( $T_a = 0$  to +65°C)**

Parameter	Symbol	Min	Max	Unit	Notes
Supply voltage	$V_{CC}$	3.0	3.6	V	1, 2
	$V_{SS}$	0	0	V	3
Input high voltage	$V_{IH}$	2.0	$V_{CC} + 0.3$	V	1, 4, 5
Input low voltage	$V_{IL}$	-0.3	0.8	V	1, 6

Notes: 1. All voltage referred to  $V_{SS}$

2. The supply voltage with all  $V_{CC}$  pins must be on the same level.

3. The supply voltage with all  $V_{SS}$  pins must be on the same level.

4. CK, CKE,  $\bar{S}$ , DQMB, DQ pins:  $V_{IH}$  (max) =  $V_{CC} + 0.5$  V for pulse width  $\leq 5$  ns at  $V_{CC}$ .

5. Others:  $V_{IH}$  (max) = 4.6 V for pulse width  $\leq 5$  ns at  $V_{CC}$ .

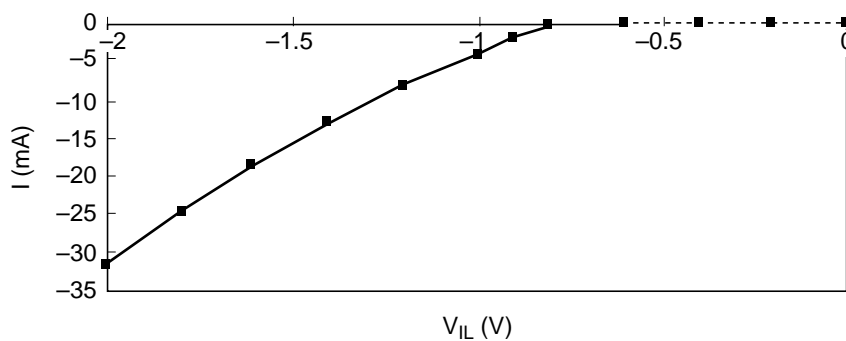
6.  $V_{IL}$  (min) = -1.0 V for pulse width  $\leq 5$  ns at  $V_{SS}$ .

**$V_{IL}/V_{IH}$  Clamp** (Component characteristic)

This SDRAM component has  $V_{IL}$  and  $V_{IH}$  clamp for CK, CKE,  $\bar{S}$ , DQMB and DQ pins.

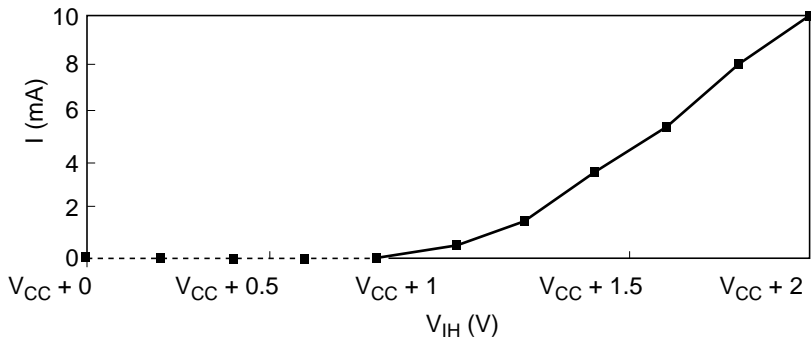
**Minimum  $V_{IL}$  Clamp Current**

$V_{IL}$ (V)	I (mA)
-2	-32
-1.8	-25
-1.6	-19
-1.4	-13
-1.2	-8
-1	-4
-0.9	-2
-0.8	-0.6
-0.6	0
-0.4	0
-0.2	0
0	0



**Minimum  $V_{IH}$  Clamp Current**

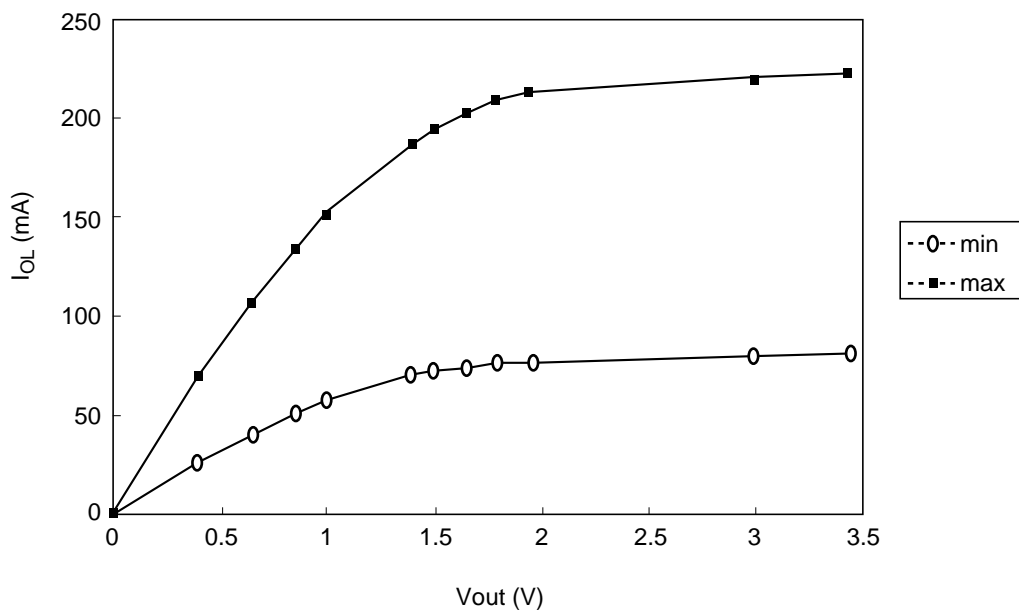
$V_{IH}$ (V)	I (mA)
$V_{CC} + 2$	10
$V_{CC} + 1.8$	8
$V_{CC} + 1.6$	5.5
$V_{CC} + 1.4$	3.5
$V_{CC} + 1.2$	1.5
$V_{CC} + 1$	0.3
$V_{CC} + 0.8$	0
$V_{CC} + 0.6$	0
$V_{CC} + 0.4$	0
$V_{CC} + 0.2$	0
$V_{CC} + 0$	0



**$I_{OL}/I_{OH}$  Characteristics** (Component characteristic)

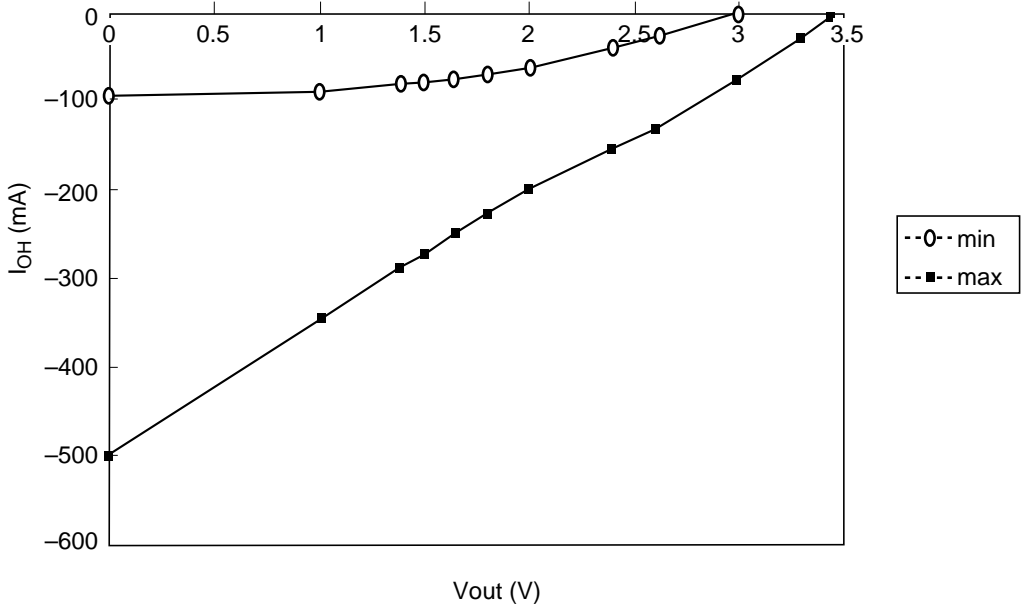
**Output Low Current ( $I_{OL}$ )**

Vout (V)	$I_{OL}$	
	Min (mA)	Max (mA)
0	0	0
0.4	27	71
0.65	41	108
0.85	51	134
1	58	151
1.4	70	188
1.5	72	194
1.65	75	203
1.8	77	209
1.95	77	212
3	80	220
3.45	81	223



Output High Current ( $I_{OH}$ ) ( $T_a = 0$  to  $65^\circ\text{C}$ ,  $V_{CC} = 3.0$  V to  $3.45$  V,  $V_{SS} = 0$  V)

Vout (V)	$I_{OH}$	
	Min (mA)	Max (mA)
3.45	—	-3
3.3	—	-28
3	0	-75
2.6	-21	-130
2.4	-34	-154
2	-59	-197
1.8	-67	-227
1.65	-73	-248
1.5	-78	-270
1.4	-81	-285
1	-89	-345
0	-93	-503



**DC Characteristics** ( $T_a = 0$  to  $65^\circ\text{C}$ ,  $V_{CC} = 3.3 \text{ V} \pm 0.3 \text{ V}$ ,  $V_{SS} = 0 \text{ V}$ )

Parameter	Symbol	HB52D48GB		Unit	Test conditions	Notes
		Min	Max			
Operating current	$I_{CC1}$	—	260	mA	Burst length = 1 $t_{RC} = \text{min}$	1, 2, 3
Standby current in power down	$I_{CC2P}$	—	6	mA	$\text{CKE0} = V_{IL}$ , $t_{CK} = 12 \text{ ns}$	6
Standby current in power down (input signal stable)	$I_{CC2PS}$	—	4	mA	$\text{CKE0} = V_{IL}$ , $t_{CK} = \infty$	7
Standby current in non power down	$I_{CC2N}$	—	40	mA	$\text{CKE0}$ , $\bar{S} = V_{IH}$ , $t_{CK} = 12 \text{ ns}$	4
Active standby current in power down	$I_{CC3P}$	—	16	mA	$\text{CKE0}$ , $\bar{S} = V_{IH}$ , $t_{CK} = 12 \text{ ns}$	1, 2, 6
Active standby current in non power down	$I_{CC3N}$	—	72	mA	$\text{CKE0}$ , $\bar{S} = V_{IH}$ , $t_{CK} = 12 \text{ ns}$	1, 2, 4
Burst operating current	$I_{CC4}$	—	260	mA	$t_{CK} = 12 \text{ ns}$ , $\text{BL} = 4$	1, 2, 5
Refresh current	$I_{CC5}$	—	440	mA	$t_{RC} = \text{min}$	3
Self refresh current	$I_{CC6}$	—	4	mA	$V_{IH} \geq V_{CC} - 0.2 \text{ V}$ $V_{IL} \leq 0.2 \text{ V}$	8
Self refresh current (L-version)	$I_{CC6}$	—	1.6	mA		
Input leakage current	$I_{LI}$	-10	10	$\mu\text{A}$	$0 \leq V_{in} \leq V_{CC}$	
Output leakage current	$I_{LO}$	-10	10	$\mu\text{A}$	$0 \leq V_{out} \leq V_{CC}$ DQ = disable	
Output high voltage	$V_{OH}$	2.4	—	V	$I_{OH} = -4 \text{ mA}$	
Output low voltage	$V_{OL}$	—	0.4	V	$I_{OL} = 4 \text{ mA}$	

Notes: 1.  $I_{CC}$  depends on output load condition when the device is selected.  $I_{CC}$  (max) is specified at the output open condition.

2. One bank operation.
3. Input signals are changed once per one clock.
4. Input signals are changed once per two clocks.
5. Input signals are changed once per four clocks.
6. After power down mode, CK0/CK1 operating current.
7. After power down mode, no CK0/CK1 operating current.
8. After self refresh mode set, self refresh current.

**Capacitance** ( $T_a = 25^\circ\text{C}$ ,  $V_{CC} = 3.3\text{ V} \pm 0.3\text{ V}$ )

<b>Parameter</b>	<b>Symbol</b>	<b>Max</b>	<b>Unit</b>	<b>Notes</b>
Input capacitance (Address)	$C_{IN}$	40	pF	1, 2, 4
Input capacitance ( $\overline{RE}$ , $\overline{CE}$ , $\overline{W}$ , CK0/CK1, CKE0)	$C_{IN}$	40	pF	1, 2, 4
Input capacitance ( $\overline{S0}$ )	$C_{IN}$	40	pF	1, 2, 4
Input capacitance (DQMB0 to DQMB7)	$C_{IN}$	20	pF	1, 2, 4
Input/Output capacitance (DQ0 to DQ63)	$C_{I/O}$	20	pF	1, 2, 3, 4

- Notes:
1. Capacitance measured with Boonton Meter or effective capacitance measuring method.
  2. Measurement condition:  $f = 1\text{ MHz}$ , 1.4 V bias, 200 mV swing.
  3. DQMB =  $V_{IH}$  to disable Data-out.
  4. This parameter is sampled and not 100% tested.



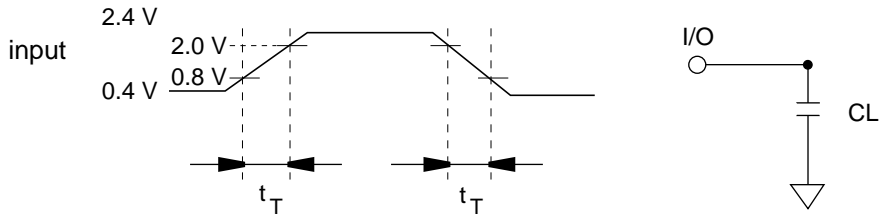
**AC Characteristics** ( $T_a = 0$  to  $65^\circ\text{C}$ ,  $V_{CC} = 3.3\text{ V} \pm 0.3\text{ V}$ ,  $V_{SS} = 0\text{ V}$ )

Parameter	HITACHI PC100 Symbol Symbol		HB52D48GB				Unit	Notes
			-A6F/A6FL		-B6F/B6FL			
			Min	Max	Min	Max		
System clock cycle time ( $\overline{\text{CE}}$ latency = 2)	$t_{\text{CK}}$	Tclk	10	—	15	—	ns	1
( $\overline{\text{CE}}$ latency = 3)	$t_{\text{CK}}$	Tclk	10	—	10	—	ns	
CK high pulse width	$t_{\text{CKH}}$	Tch	3	—	3	—	ns	1
CK low pulse width	$t_{\text{CKL}}$	Tcl	3	—	3	—	ns	1
Access time from CK ( $\overline{\text{CE}}$ latency = 2)	$t_{\text{AC}}$	Tac	—	6	—	8	ns	1, 2
( $\overline{\text{CE}}$ latency = 3)	$t_{\text{AC}}$	Tac	—	6	—	6	ns	
Data-out hold time	$t_{\text{OH}}$	Toh	3	—	3	—	ns	1, 2
CK to Data-out low impedance	$t_{\text{LZ}}$		2	—	2	—	ns	1, 2, 3
CK to Data-out high impedance	$t_{\text{HZ}}$		—	6	—	6	ns	1, 4
Data-in setup time	$t_{\text{AS}}, t_{\text{CS}},$ $t_{\text{DS}}, t_{\text{CES}}$	Tsi	2	—	2	—	ns	1, 5, 6
CKE setup time for power down exit	$t_{\text{CESP}}$	Tpde	2	—	2	—	ns	1
Data-in hold time	$t_{\text{AH}}, t_{\text{CH}},$ $t_{\text{DH}}, t_{\text{CEH}}$	Thi	1	—	1	—	ns	1, 5
Ref/Active to Ref/Active command period	$t_{\text{RC}}$	Trc	70	—	70	—	ns	1
Active to Precharge command period	$t_{\text{RAS}}$	Tras	50	120000	50	120000	ns	1
Active command to column command (same bank)	$t_{\text{RCD}}$	Trcd	20	—	20	—	ns	1
Precharge to active command period	$t_{\text{RP}}$	Trp	20	—	20	—	ns	1
Write recovery or data-in to precharge lead time	$t_{\text{DPL}}$	Tdpl	10	—	10	—	ns	1
Active (a) to Active (b) command period	$t_{\text{RRD}}$	Trrd	20	—	20	—	ns	1
Transition time (rise and fall)	$t_{\text{T}}$		1	5	1	5	ns	
Refresh period	$t_{\text{REF}}$		—	64	—	64	ms	

- Notes:
1. AC measurement assumes  $t_T = 1$  ns. Reference level for timing of input signals is 1.5 V.
  2. Access time is measured at 1.5 V. Load condition is  $CL = 50$  pF.
  3.  $t_{LZ}$  (min) defines the time at which the outputs achieves the low impedance state.
  4.  $t_{HZ}$  (max) defines the time at which the outputs achieves the high impedance state.
  5.  $t_{CES}$  define CKE setup time to CK rising edge except power down exit command.
  6.  $t_{AS}/t_{AH}$ : Address,  $t_{CS}/t_{CH}$ :  $\overline{S}$ ,  $\overline{RE}$ ,  $\overline{CE}$ ,  $\overline{W}$ , DQMB  
 $t_{DS}/t_{DH}$ : Data-in,  $t_{CES}/t_{CEH}$ : CKE

## Test Conditions

- Input and output timing reference levels: 1.5 V
- Input waveform and output load: See following figures



**Relationship Between Frequency and Minimum Latency**

Parameter	HB52D48GB			
	-A6F/A6FL/B6F/B6FL			
Frequency (MHz)	100			
$t_{CK}$ (ns)	HITACHI Symbol	PC100 Symbol	10	Notes
Active command to column command (same bank)	$I_{RCD}$		2	1
Active command to active command (same bank)	$I_{RC}$		7	= [ $I_{RAS} + I_{RP}$ ] 1
Active command to precharge command (same bank)	$I_{RAS}$		5	1
Precharge command to active command (same bank)	$I_{RP}$		2	1
Write recovery or data-in to precharge command (same bank)	$I_{DPL}$	$T_{dpl}$	1	1
Active command to active command (different bank)	$I_{RRD}$		2	1
Self refresh exit time	$I_{SREX}$	$T_{srx}$	1	2
Last data in to active command (Auto precharge, same bank)	$I_{APW}$	$T_{dal}$	4	= [ $I_{DPL} + I_{RP}$ ]
Self refresh exit to command input	$I_{SEC}$		7	= [ $I_{RC}$ ] 3
Precharge command to high impedance (CE latency = 2)	$I_{HZP}$	$T_{roh}$	2	
( $\overline{CE}$ latency = 3)	$I_{HZP}$	$T_{roh}$	3	
Last data out to active command (auto precharge) (same bank)	$I_{APR}$		1	
Last data out to precharge (early precharge) ( $\overline{CE}$ latency = 2)	$I_{EP}$		-1	
( $\overline{CE}$ latency = 3)	$I_{EP}$		-2	
Column command to column command	$I_{CCD}$	$T_{ccd}$	1	
Write command to data in latency	$I_{WCD}$	$T_{dwd}$	0	
DQMB to data in	$I_{DID}$	$T_{dqm}$	0	
DQMB to data out	$I_{DOD}$	$T_{dqz}$	2	
CKE to CK disable	$I_{CLE}$	$T_{cke}$	1	
Register set to active command	$I_{RSA}$	$T_{mrd}$	1	

Parameter	HB52D48GB			Notes
	-A6F/A6FL/B6F/B6FL			
Frequency (MHz)	100			
$t_{CK}$ (ns)	HITACHI Symbol	PC100 Symbol	10	
$\overline{S}$ to command disable	$I_{CDD}$		0	
Power down exit to command input	$I_{PEC}$		1	
Burst stop to output valid data hold ( $\overline{CE}$ latency = 2)	$I_{BSR}$		1	
	$I_{BSR}$		2	
Burst stop to output high impedance ( $\overline{CE}$ latency = 2)	$I_{BSH}$		2	
	$I_{BSH}$		3	
Burst stop to write data ignore	$I_{BSW}$		0	

- Notes: 1.  $I_{RCD}$  to  $I_{RRD}$  are recommended value.  
 2. Be valid [DSEL] or [NOP] at next command of self refresh exit.  
 3. Except [DSEL] and [NOP].

## Pin Functions

**CK0/CK1 (input pin):** CK is the master clock input to this pin. The other input signals are referred at CK rising edge.

**$\overline{S0}$  (input pin):** When  $\overline{S}$  is Low, the command input cycle becomes valid. When  $\overline{S}$  is High, all inputs are ignored. However, internal operations (bank active, burst operations, etc.) are held.

**$\overline{RE}$ ,  $\overline{CE}$  and  $\overline{W}$  (input pins):** Although these pin names are the same as those of conventional DRAM modules, they function in a different way. These pins define operation commands (read, write, etc.) depending on the combination of their voltage levels. For details, refer to the command operation section.

**A0 to A11 (input pins):** Row address (AX0 to AX11) is determined by A0 to A11 level at the bank active command cycle CK rising edge. Column address (AY0 to AY7) is determined by A0 to A7 level at the read or write command cycle CK rising edge. And this column address becomes burst access start address. A10 defines the precharge mode. When A10 = High at the precharge command cycle, both banks are precharged. But when A10 = Low at the precharge command cycle, only the bank that is selected by A12/A13 (BA) is precharged.

**A12/A13 (input pin):** A12/A13 is a bank select signal (BA). The memory array is divided into bank0, bank1, bank2 and bank3. If A12 is Low and A13 is Low, bank0 is selected. If A12 is High and A13 is Low, bank1 is selected. If A12 is Low and A13 is High, bank2 is selected. If A12 is High and A13 is High, bank3 is selected.

**CKE0 (input pin):** This pin determines whether or not the next CK is valid. If CKE is High, the next CK rising edge is valid. If CKE is Low, the next CK rising edge is invalid. This pin is used for power-down mode, clock suspend mode and self refresh mode.

**DQMB0 to DQMB7 (input pins):** Read operation: If DQMB is High, the output buffer becomes High-Z. If the DQMB is Low, the output buffer becomes Low-Z (The latency of DQMB during reading is 2 clocks).

Write operation: If DQMB is High, the previous data is held (the new data is not written). If DQMB is Low, the data is written (The latency of DQMB during writing is 0 clock).

**DQ0 to DQ63 (DQ pins):** Data is input to and output from these pins.

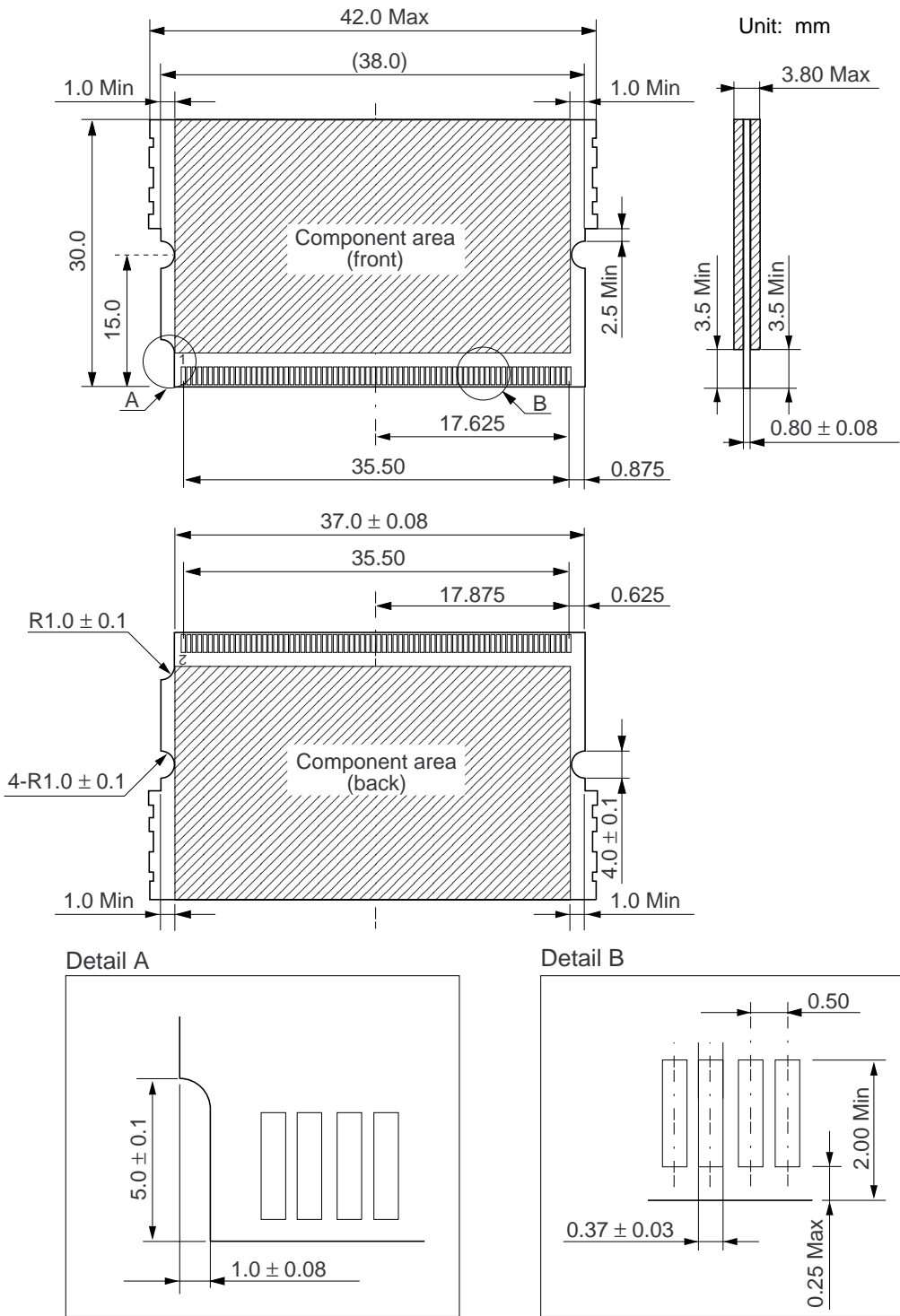
**V<sub>CC</sub> (power supply pins):** 3.3 V is applied.

**V<sub>SS</sub> (power supply pins):** Ground is connected.

## Detailed Operation Part

Refer to the HM5264165F/HM5264805F/HM5264405F-75/A60/B60 datasheet.

**Physical Outline**



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0.0	Jan. 13, 2000	Initial issue (referred to HM5264165F/HM5264805F/HM5264405F- 75/A60/B60 rev 1.0)		

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