FINAL

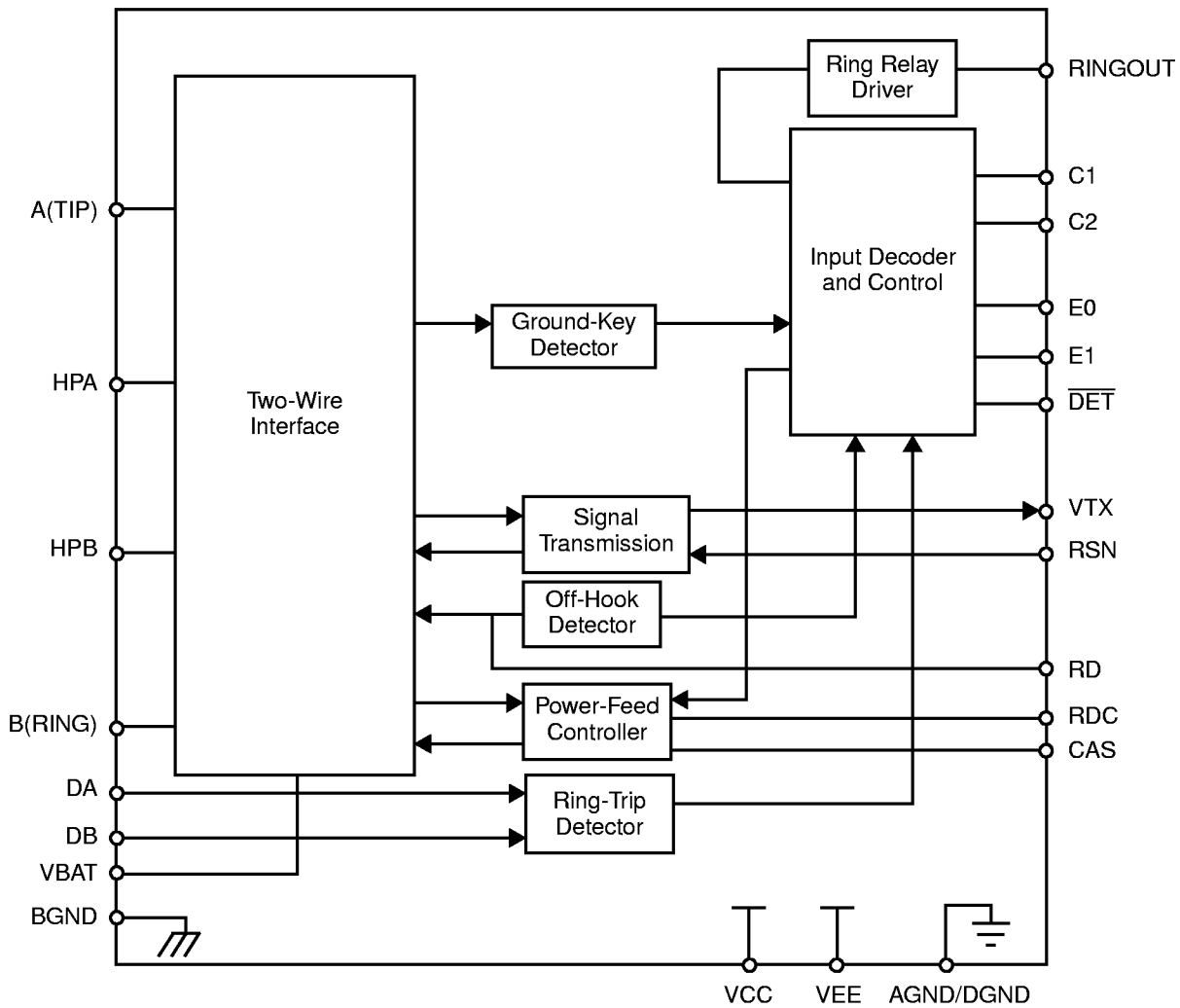
Am79467

Subscriber Line Interface Circuit

DISTINCTIVE CHARACTERISTICS

- Optimized for long-loop operation
- Programmable constant-current feed
- Programmable loop-current detector
- Programmable ground-key detector
- Low standby power
- On-hook transmission
- –24 V to –58 V battery operation
- On-chip relay driver
- Two-wire impedance set by single external impedance

BLOCK DIAGRAM



Publication# **18508** Rev: **C** Amendment: **/0**
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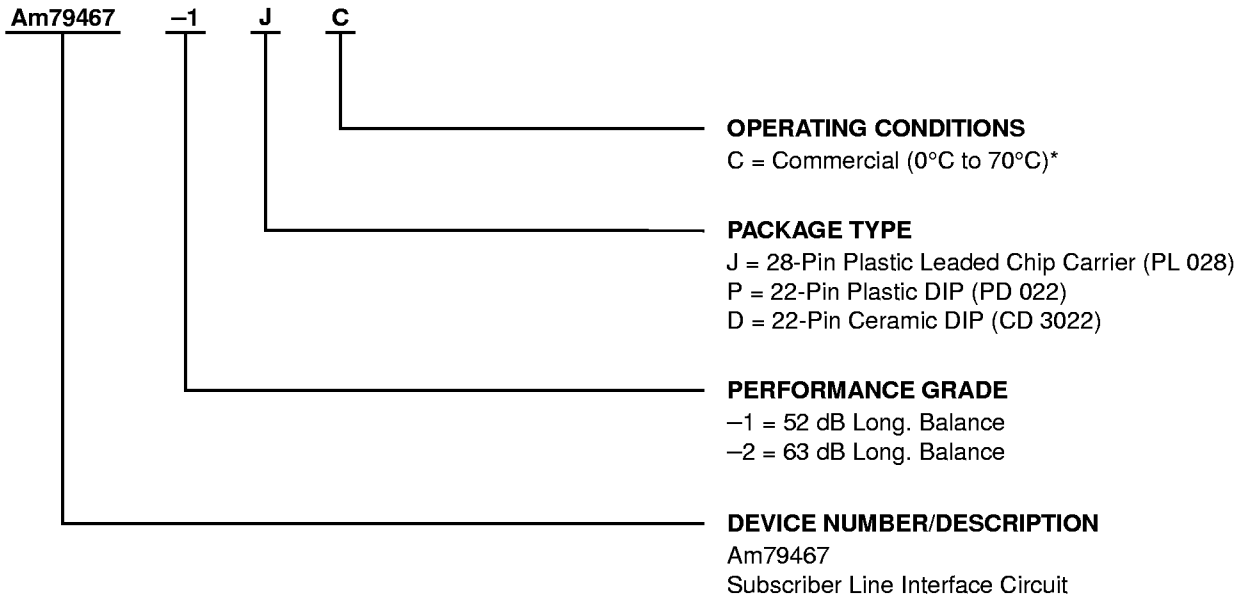
ORDERING INFORMATION

Standard Products

AMD standard products are available in several packages and operating ranges. The order number (Valid Combination) is formed by a combination of the elements below.



Valid Combinations		
Am79467	–1 –2	JC PC DC

Valid Combinations

Valid Combinations list configurations planned to be supported in volume for this device. Consult the local AMD sales office to confirm availability of specific valid combinations, to check on newly released combinations, and to obtain additional data on AMD's standard military grade products.

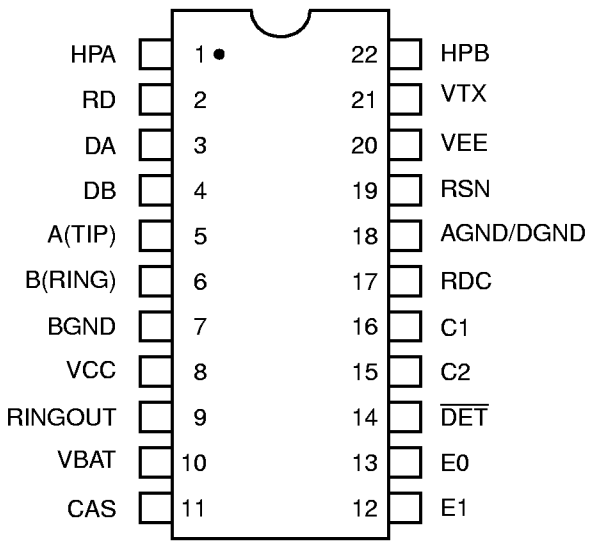
Note:

** Functionality of the device from 0°C to +70°C is guaranteed by production testing. Performance from –40°C to +85°C is guaranteed by characterization and periodic sampling of production units.*

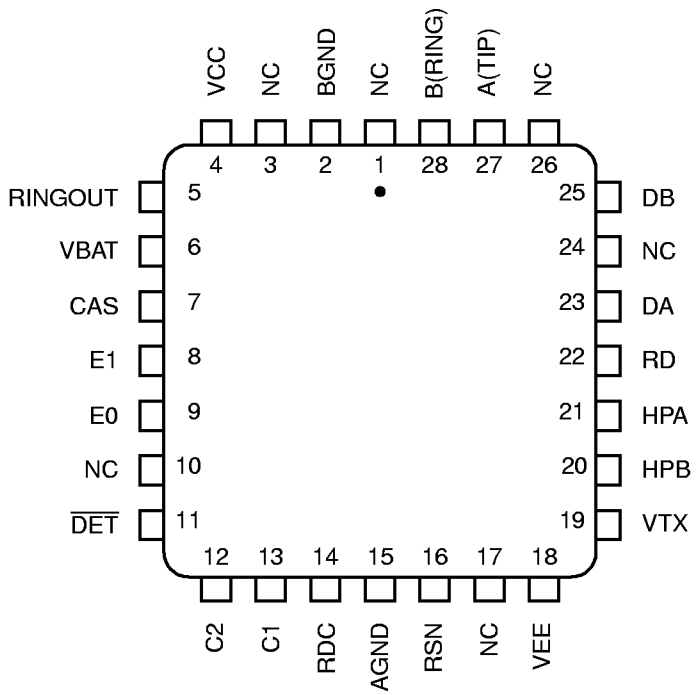
CONNECTION DIAGRAMS

Top View

22-Pin DIP



28-Pin PLCC



Notes:

1. *Pin 1 is marked for orientation.*
2. *NC = No connect*

PIN DESCRIPTIONS

Pin Names	Type	Description
AGND/DGND	Gnd	Analog and Digital ground.
A(TIP)	Output	Output of A(TIP) power amplifier.
BGND	Gnd	Battery (power) ground.
B(RING)	Output	Output of B(RING) power amplifier.
C3–C1	Input	Decoder. TTL compatible. C3 is MSB and C1 is LSB.
CAS	Capacitor	Anti-saturation pin for capacitor to filter reference voltage when operating in anti-saturation region.
DA	Input	Ring-trip negative. Negative input to ring-trip comparator.
DB	Input	Ring-trip positive. Positive input to ring-trip comparator.
$\overline{\text{DET}}$	Output	Switchhook detector. When enabled, a logic Low indicates the selected detector is tripped. The detector is selected by the logic inputs (C2–C1, E1–E0). The output is open-collector with a built-in 15 kΩ pull-up resistor.
E0	Input	$\overline{\text{DET}}$ Enable. A logic High disables $\overline{\text{DET}}$. A logic Low enables $\overline{\text{DET}}$.
E1	Input	Ground-Key Enable. A logic High selects the off-hook detector. A logic Low selects the ground-key detector. TTL compatible.
HPA	Capacitor	High-Pass Filter Capacitor. A(TIP) side of high-pass filter capacitor.
HPB	Capacitor	High-Pass Filter Capacitor. B(RING) side of high-pass filter capacitor.
NC	—	No connect. This pin not internally connected.
RD	Resistor	Detector resistor. Detector threshold set and filter pin.
RDC	Resistor	DC feed resistor. Connection point for the DC feed current programming network. The other end of the network connects to the receiver summing node (RSN). Connection point for the DC feed current programming network. The other end of the network connects to the receiver summing node (RSN). V_{RDC} is negative for normal polarity and positive for reverse polarity.
RINGOUT	Output	Ring Relay Driver. Open-collector driver with emitter internally connected to BGND.
RSN	Input	Receive Summing Node. The metallic current (AC and DC) between A(TIP) and B(RING) is equal to 1000 times the current into this pin. The networks that program receive gain, two-wire impedance, and feed current all connect to this node.
VBAT	Battery	Battery supply and connection to substrate.
VCC	Power	+5 V power supply.
VEE	Power	–5 V power supply.
VTX	Output	Transmit Audio. This output is a unity gain version of the A(TIP) and B(RING) metallic voltage. VTX also sources the two-wire input impedance programming network.

ABSOLUTE MAXIMUM RATINGS

Storage temperature . . . . . –60°C to +150°C

V_{CC} with respect to AGND/DGND . . . . . 0.5 V to +7 V

V_{EE} with respect to AGND/DGND . . . . . 0.5 V to –7 V

V_{BAT} with respect to AGND/DGND . . . 0.5 V to –70 V

BGND with respect to AGND/DGND . . . +3 V to –3 V

A(TIP) or B(RING) to BGND:

- Continuous . . . . . V_{BAT} to +2 V
- 10 ms (f = 0.1 Hz) . . . . . V_{BAT} – 20 V to +5 V
- 1 µs (f = 0.1 Hz) . . . . . V_{BAT} – 40 V to +10 V
- 250 ns (f = 0.1 Hz) . . . . . V_{BAT} – 70 V to +15 V

Current from A(TIP) or B(RING). . . . . 70 mA

Current through relay driver . . . . . 50 mA

Ring relay supply voltage . . . . . 0 V to V_{BAT} + 75 V

DA and DB inputs:

- Voltage on ring-trip inputs . . . . . V_{BAT} to 0 V
- Current into ring-trip inputs . . . . . ±5 mA

C2–C1, E0, E1, $\overline{DET}$

- Input voltage . . . . . 0 V to V_{CC}
- Output voltage ($\overline{DET}$ not active) . . . . . 0 V to V_{CC}
- Output current ($\overline{DET}$) . . . . . 5 mA

Power Dissipation ($T_A \leq 70°C$):

- Continuous . . . . . 1.5 W
- Peak (t < 100 ms, t_{REP} > 1 s). . . . . 4 W

Note: *Thermal limiting circuitry on chip will shut down the circuit at a junction temperature of about 165°C. The device should never be exposed to this temperature. Operation above 145°C junction temperature may degrade device reliability. See the SLIC Packaging Considerations for more information.*

Stresses above those listed under Absolute Maximum Ratings may cause permanent device failure. Functionality at or above these limits is not implied. Exposure to Absolute Maximum Ratings for extended periods may affect device reliability.

OPERATING RANGES

Commercial (C) Devices

Ambient temperature . . . . . 0°C to +70°C*

V_{CC} . . . . . 4.75 V to 5.25 V

V_{EE} . . . . . –4.75 V to –5.25 V

V_{BAT} . . . . . –24 V to –58 V

AGND/DGND . . . . . 0 V

BGND with respect to AGND/DGND . . . . . –100 mV to +100 mV

Operating Ranges define those limits between which device functionality is guaranteed.

** Functionality of the device from 0°C to +70°C is guaranteed by production testing. Performance from –40°C to +85°C is guaranteed by characterization and periodic sampling of production units.*

ELECTRICAL CHARACTERISTICS

Description	Test Conditions (See Note 1)	Min	Typ	Max	Unit	Note
Transmission Performance						
2-wire return loss	200 Hz to 500 Hz 500 Hz to 1 kHz 1.0 kHz to 3.4 kHz	25 27 23			dB	1, 4
Z_{VTX}, Analog output impedance			3	20	Ω	4
V_{VTX}, Analog output offset voltage	0°C to +70°C –40°C to +85°C	–35 –40		+35 +40	mV	— 4
Overload level, 2-wire and 4-wire	R_L = 600 Ω	3.1			Vpk	2
Overload level	Load impedance > 20 kΩ	3.1				
THD, Total harmonic distortion	1.0 kHz, 0 dBm		–65	–54	dB	5
THD, on-hook	0 dBm, R_L = 900 Ω, Battery = –51 V			–35.5		
Longitudinal Performance						
Longitudinal to metallic L-T, L-4 balance	200 Hz to 3.4 kHz –1 parts*	52			dB	
Longitudinal to metallic L-T, L-4 balance	200 Hz to 1 kHz: –2 parts* 0°C to +70°C –40°C to +85°C	 63 55				— 4
	1 kHz to 3.4 kHz: –2 parts* 0°C to +70°C –40°C to +85°C	 58 55				— 4
Longitudinal signal generation 4-L	200 Hz to 4 kHz, normal polarity	45	55			
Longitudinal current per pin (A or B)	Active state	25	35		mArms	
Longitudinal impedance (A or B)	0 Hz to 100 Hz		20	35	Ω/pin	
Idle Channel Noise						
C-message weighted noise	2-wire: 0°C to +70°C –40°C to +85°C		+7	+10 +12	dBrnC	— 4
	4-wire: 0°C to +70°C –40°C to +85°C		+7	+10 +12		— 4
Psophometric weighted noise	2-wire: 0°C to +70°C –40°C to +85°C		–83	–80 –78	dBmp	4
	4-wire: 0°C to +70°C –40°C to +85°C		–83	–80 –78		
Receive Summing Node (RSN)						
RSN DC voltage	I_{RSN} = 0 mA		0		V	4
RSN impedance	200 Hz to 3.4 kHz		10	20	Ω	
RSN current to metallic loop-current gain	300 Hz to 3.4 kHz 0°C to +70°C –40°C to +85°C	988 980	1000 1000	1012 1020		

Note:
** Performance Grade*

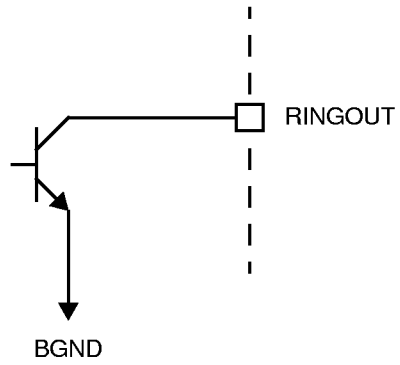
ELECTRICAL CHARACTERISTICS (continued)

Description	Test Conditions (See Note 1)	Min	Typ	Max	Unit	Note
Insertion Loss and Balance Return Signal (2-Wire to 4-Wire, 4-Wire to 2-Wire, and 4-Wire to 4-Wire, See Test Circuits A and B)						
Gain accuracy over temperature	0 dBm, 1 kHz 0°C to +70°C −40°C to +85°C	−0.15 −0.20	0 0	+0.15 +0.20	dB	3 4
Gain accuracy over frequency	300 Hz to 3.4 kHz (relative to 1 kHz): 0°C to +70°C −40°C to +85°C	−0.10 −0.15		+0.10 +0.15	dB	3 4
Gain tracking	+3 dBm to −55 dBm (relative to 0 dBm): 0°C to +70°C −40°C to +85°C	−0.10 −0.15		+0.10 +0.15	dB	3, 4 4
Group delay	0 dBm, 1 kHz		5.3		µs	5
Line Characteristics						
Long loops, Active state	BAT = −50 V, R_{LDC} = 2000 Ω	21			mA	4
I_L, Loop current accuracy	I_L in constant-current region	$0.915I_L$	I_L	$1.085I_L$	mA	
I_L, Accuracy, Standby state	$I_L = \frac{\lvert V_{BAT}\rvert - 3\ V}{R_L + 1800}$ T_A = 25°C	$0.8I_L$	I_L	$1.2I_L$	mA	
I_L, Loop current	Disconnect, R_L = 0			100	µA	
VAB, Open Circuit voltage	V_{BAT} = −50 V	42.8			V	
Power Supply Rejection Ratio (V_{RIPPLE} = 100 mVrms), Active Normal State						
V_{CC} V_{EE} V_{BAT}	50 Hz to 3.4 kHz 50 Hz to 3.4 kHz 50 Hz to 3.4 kHz	30 30 35	40 36 41		dB	5
Effective internal resistance	CAS pin to GND		60		kΩ	4
Off-Hook Detector						
On-threshold	R_D = 33 kΩ	11.3		17.3	mA	
Off-threshold	R_D = 33 kΩ	9.85		14.7	mA	
Hysteresis	R_D = 33 kΩ	0		3.2	mA	
Power Dissipation, Battery = −58 V						
On-hook Open Circuit state			25		mW	
On-hook Standby state			50		mW	
On-hook Active state	R_L = ∞, V_{BAT} = −50 V		145	300	mW	
Off-hook Active state	R_L = 0 Ω R_L = 300 Ω R_L = 600 Ω		1.5 1.4 1.2	1.8 1.6 1.4	W	

ELECTRICAL CHARACTERISTICS (continued)

Description	Test Conditions (See Note 1)	Min	Typ	Max	Unit	Note
Supply Currents, Battery = –58 V						
I_{CC}, on-hook V_{CC} supply current	Open Circuit state Standby state Active state, V_{BAT} = –50 V		1.2 1.7 4.8	2.0 2.5 6.5	mA	
I_{EE}, on-hook V_{EE} supply current	Open Circuit state Standby state Active state, V_{BAT} = –50 V		0.5 0.9 1.9	1.3 1.6 3.0		
I_{BAT}, on-hook V_{BAT} supply current	Open Circuit state Standby state Active state, V_{BAT} = –50 V		0.3 0.7 2.6	1.2 1.6 4.5		
Ground-Key Detector Thresholds						
I_A and I_B delta to trigger the ground-key detector		8	12	17	mA	
I_A and I_B delta to clear the triggered ground-key detector		3	7	12		
Hysteresis		3	5	8		
Ring-Trip Detector Input						
Bias current		–500	–100		nA	
Offset voltage	Source resistance = 0 to 2 MΩ	–50	0	+50	mV	
Input resistance	Unbalanced Balanced	1 3			MΩ	4
Input common mode range		V_{BAT}		–2	V	
Logic Inputs (C2–C1, E0, E1)						
V_{IH}, Input High voltage		2.0			V	
V_{IL}, Input Low voltage				0.8		
I_{IH}, Input High current	All inputs except E1	–75		40	µA	
Input High current	Input E1	–75		45		
I_{IL}, Input Low current		–500				
Logic Output ($\overline{DET}$)						
V_{OH}, Output Low voltage	I_{OUT} = 0.8 mA, 15 kΩ to V_{CC}			0.40	V	
V_{OL}, Output High voltage	I_{OUT} = –0.1 mA, 15 kΩ to V_{CC}	2.4				
Internal pull-up resistor		8		25	kΩ	
Relay Driver Output (RINGOUT)						
On voltage	I_{OL} = 25 mA		+0.2	+0.75	V	
Off leakage	V_{OH} = +12 V			10	µA	

RELAY DRIVER SCHEMATIC

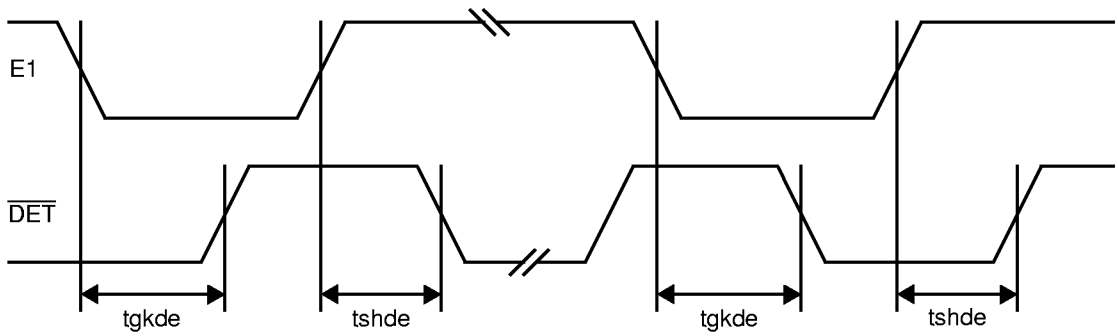


SWITCHING CHARACTERISTICS

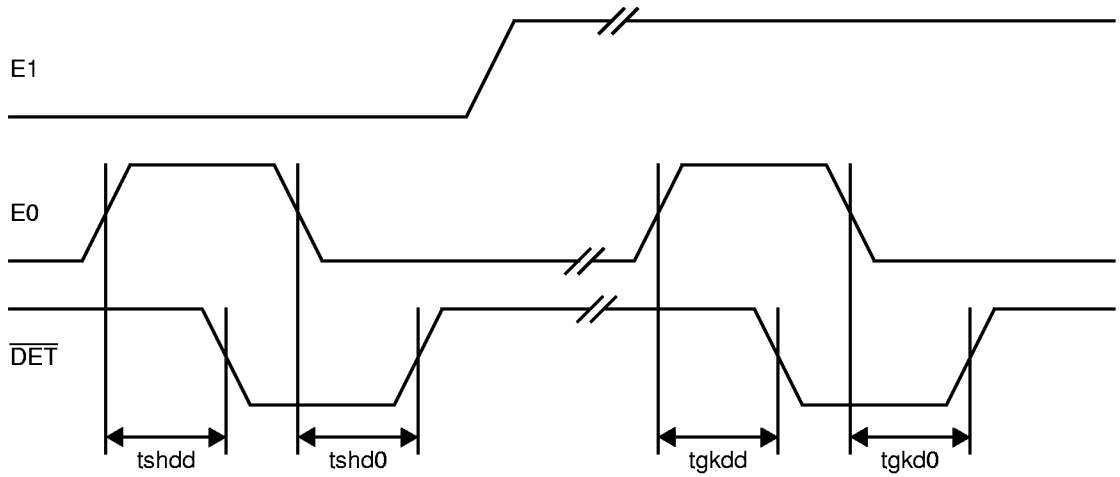
Symbol	Parameter	Test Conditions	Temperature Ranges	Min	Typ	Max	Unit	Note
tgkde	E1 Low to $\overline{DET}$ High (E0 = 1)	Ground-Key Detect state R_L open, R_G connected (See Figures E and F)	0°C to +70°C −40°C to +85°C			3.8 4.0	µs	4
	E1 Low to $\overline{DET}$ Low (E0 = 1)		0°C to +70°C −40°C to +85°C			1.1 1.6		
tgkdd	E0 High to $\overline{DET}$ Low (E1 = 0)		0°C to +70°C −40°C to +85°C			1.1 1.6		
tgkd0	E0 Low to $\overline{DET}$ High (E1 = 0)		0°C to +70°C −40°C to +85°C			3.8 4.0		
tshde	E1 High to $\overline{DET}$ Low (E0 = 1)	Switchhook Detect state R_L = 600 Ω, R_G open (See Figures E and F)	0°C to +70°C −40°C to +85°C			1.2 1.7		
	E1 High to $\overline{DET}$ High (E0 = 1)		0°C to +70°C −40°C to +85°C			3.8 4.0		
tshdd	E0 High to $\overline{DET}$ Low (E1 = 1)		0°C to +70°C −40°C to +85°C			1.1 1.6		
tshd0	E0 Low to $\overline{DET}$ High (E1 = 1)		0°C to +70°C −40°C to +85°C			3.8 4.0		

SWITCHING WAVEFORMS

E1 to $\overline{\text{DET}}$



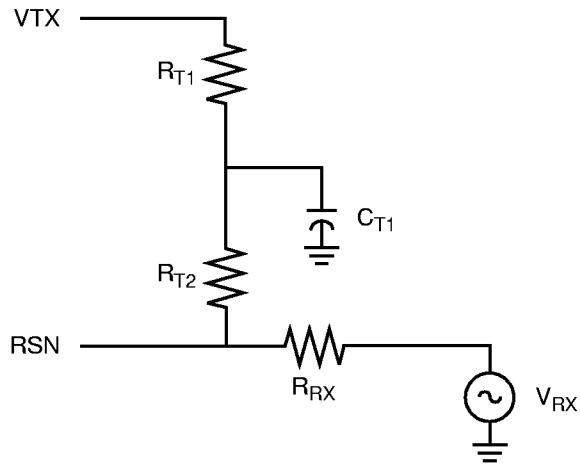
E0 to $\overline{\text{DET}}$



Note:
All delays measured at 1.4 V level.

Notes:

1. *Unless otherwise noted, test conditions are BAT = –52 V, V_{CC} = +5 V, V_{EE} = –5 V, R_L = 600 Ω, C_{HP} = 18 nF, R_{DC1} = R_{DC2} = 52.3 kΩ, C_{DC} = 0.68 µF, R_D = 33 kΩ, no fuse resistors, D_1 = 1N400x, two-wire AC input impedance is a 600 Ω resistance synthesized by the programming network shown below.*



Where: R_{T1} = R_{T2} = R_{RX} = 300 kΩ, C_{T1} = 150 pF*

* C_{T1} is not required when 23 dB two-wire return loss at higher voice frequencies is acceptable. If C_{T1} is not used, R_{T1} and R_{T2} can be combined into one resistor. If this SLIC is used with a DSLAC™ device, C_{T1} is not required.

2. *Overload level is defined when THD = 1%.*
3. *Balance return signal is the signal generated at V_{TX} by V_{RX}. This specification assumes the two-wire AC load impedance matches the programmed impedance.*
4. *Not tested in production. This parameter is guaranteed by characterization or correlation to other tests.*
5. *This parameter is tested at 1 kHz in production. Performance at other frequencies is guaranteed by characterization.*

Table 1. SLIC Decoding

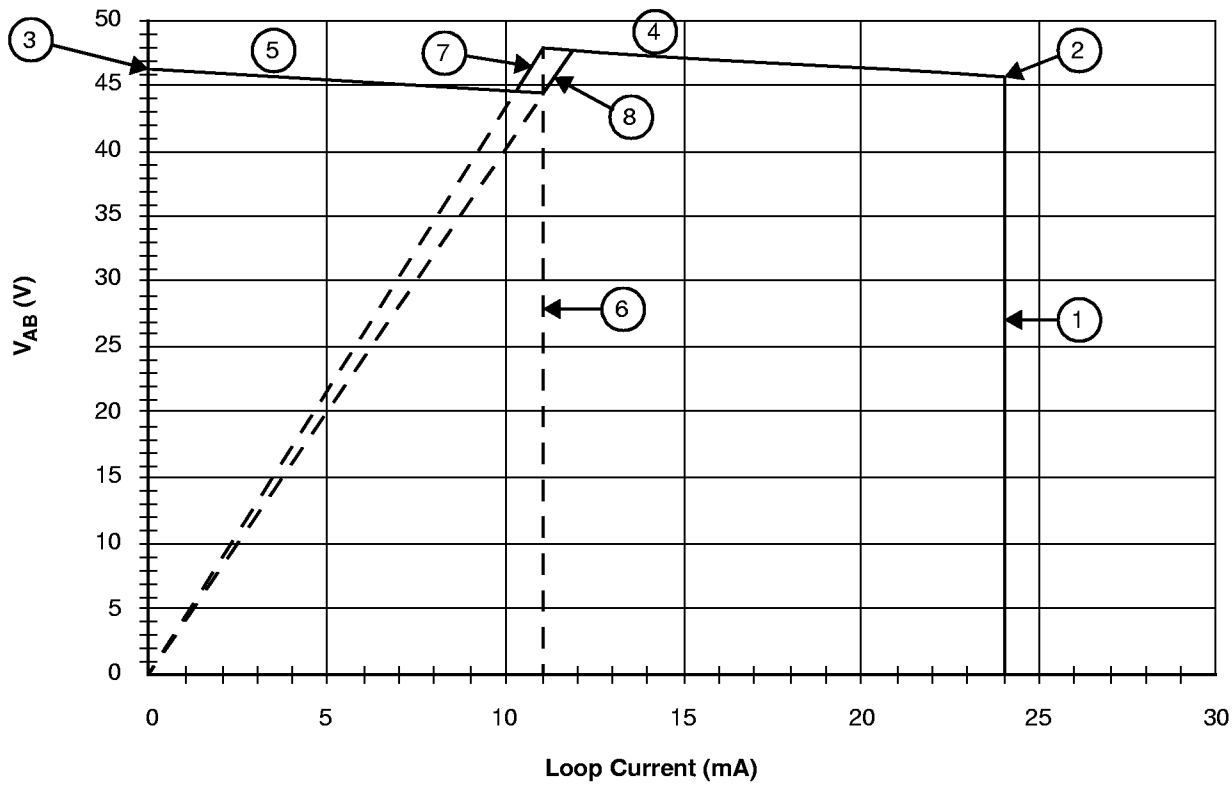
State	E1	C1	C2	Two-Wire Status	Detector Mode	$\overline{\text{DET}}$ Output
0	0	0	0	Open Circuit	No active detector	Logic level High
1	0	0	1	Active	Ground-key detector	Ground key
2	0	1	0	Ringing	No active detector	Logic level High
3	0	1	1	Standby	Ground-key detector	Ground key
4	1	0	0	Open Circuit	No active detector	Logic level High
5	1	0	1	Active	Loop-current detector	Loop-current status
6	1	1	0	Ringing	Ring-trip detector	Ring-trip status
7	1	1	1	Standby	Loop-current detector	Loop-current status

Note:
E0 = 1. For E0 = 0, $\overline{DET}$ = logic level High.

Table 2. User-Programmable Components

$Z_T = 1000(Z_{2WIN} - 2R_F)$	Where Z_T is connected between the VTX and RSN pins. The fuse resistors are R_F, and Z_{2WIN} is the desired 2-wire AC input impedance. When computing Z_T, the internal current amplifier pole and any external stray capacitance between VTX and RSN must be taken into account.
$Z_{RX} = \frac{Z_T}{2}$	Where Z_{RX} is connected from V_{RX} to the RSN pin and Z_T is defined above. This equation sets the receive gain to 0 dB when the SLIC is terminated with an impedance equal to Z_{2WIN}.
$R_{DC1} + R_{DC2} = \frac{2500\ V}{I_{LOOP}}$ $C_{DC} = 30\ ms\left(\frac{1}{R_{DC1}} + \frac{1}{R_{DC2}}\right)$	Where R_{DC1}, R_{DC2}, and C_{DC} form the network connected to the RDC pin. R_{DC1} and R_{DC2} are approximately equal. I_{LOOP} is the desired loop current in the constant-current region.
$R_D = \frac{365}{I_T}$, $C_D = \frac{0.5\ ms}{R_D}$	Where R_D and C_D form the network connected from RD to –5 V and I_T is the threshold current between on hook and off hook.
$C_{CAS} = \frac{1}{(1.2 \bullet 10^5) f_c}$	Where C_{CAS} is the regulator filter capacitor and f_c is the desired filter cut-off frequency.

DC FEED CHARACTERISTICS



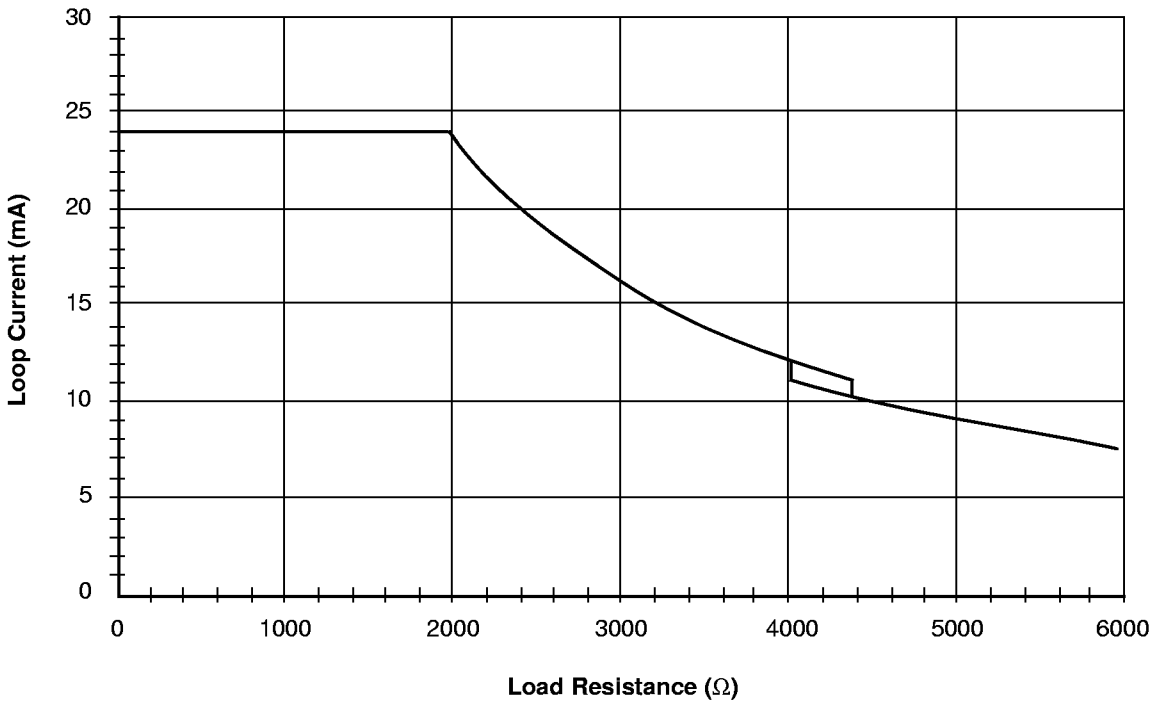
R_{DC} = 104.6 kΩ
V_{BAT} = 51.3 V
R_D = 33 kΩ

Notes:

1. *Constant-current region:* $I_L = \frac{2500}{R_{DC}}$
2. *Anti-sat (battery tracking) turn-on:* $V_{AB} = 0.96|V_{BAT}| - 3.65$
3. *Open Circuit voltage:* $V_{AB} = 1.025|V_{BAT}| - 6.23$
4. *Anti-sat region ($I_L > I_{DET}$):* $V_{AB} = 0.96|V_{BAT}| - 3.65 + \frac{2500}{600} - I_L\left(\frac{R_{DC}}{600}\right)$
5. *Anti-sat region ($I_L < I_{DET}$):* $V_{AB} = 1.025|V_{BAT}| - 6.23 - I_L\left(\frac{R_{DC}}{600}\right)$
6. *Loop-detect (I_{DET}) threshold:* $I_{DET} = \frac{365}{R_D}$
7. *Anti-sat transition region, off-hook to on-hook*
8. *Anti-sat transition region, on-hook to off-hook*

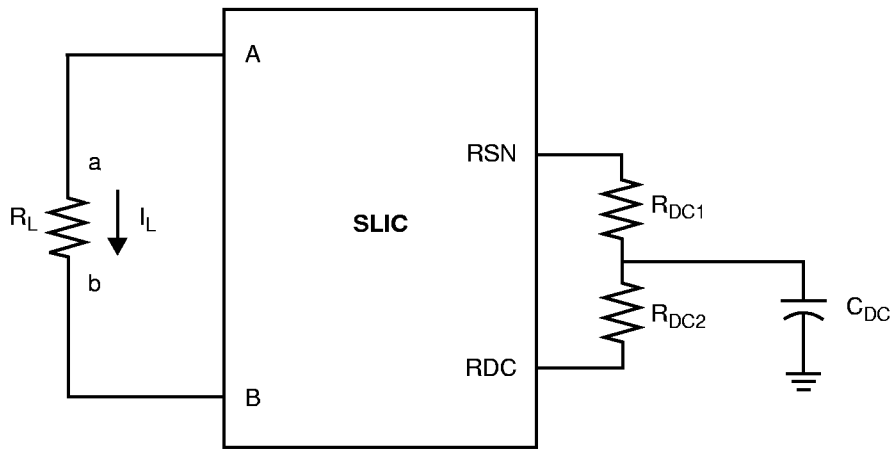
a. V_A–V_B (V_{AB}) Voltage vs. Loop Current (Typical)

DC FEED CHARACTERISTICS (continued)



R_{DC} = 104.6 kΩ
V_{BAT} = 51.3 V
R_D = 33 kΩ

b. Loop Current vs. Load Resistance (Typical)

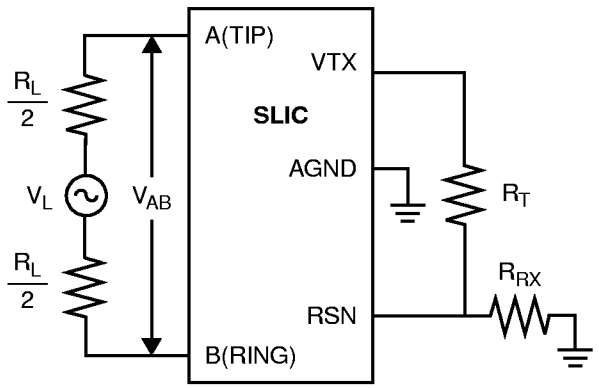


Feed current programmed by R_{DC1} and R_{DC2}

c. Feed Programming

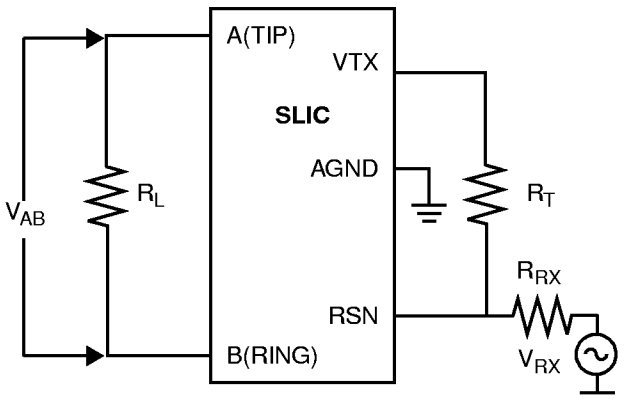
Figure 1. DC Feed Characteristics

TEST CIRCUITS



$I_{L2-4} = 20 \log (V_{TX} / V_{AB})$

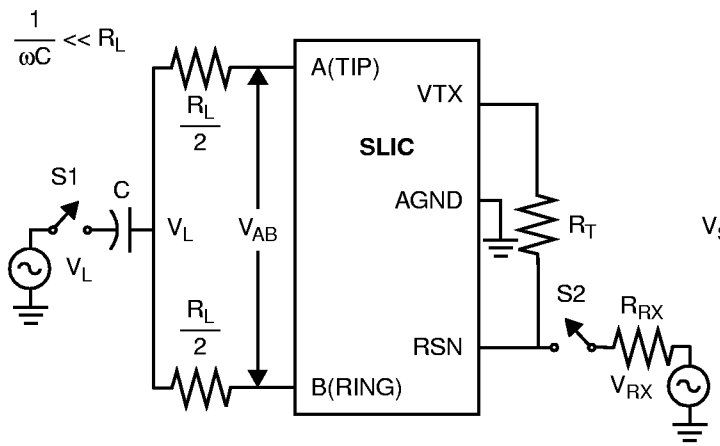
A. Two- to Four-Wire Insertion Loss



$I_{L4-2} = 20 \log (V_{AB} / V_{RX})$

$BRS = 20 \log (V_{TX} / V_{RX})$

B. Four- to Two-Wire Insertion Loss and Balance Return Signal



S2 Open, S1 Closed:

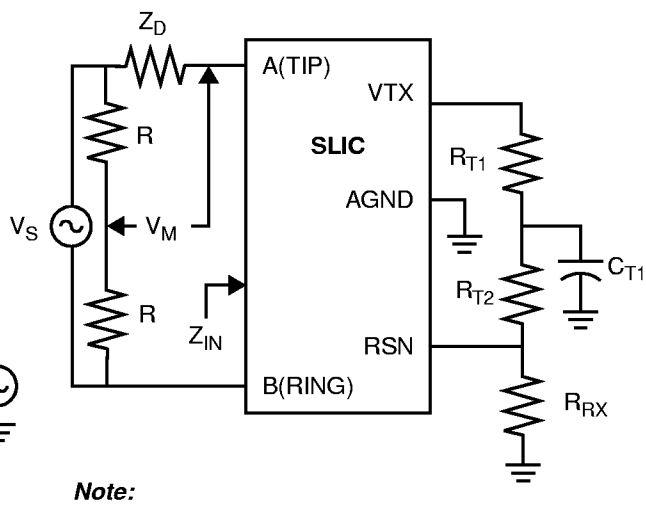
L-T Long. Bal. = 20 log (V_{AB} / V_L)

L-4 Long. Bal. = 20 log (V_{TX} / V_L)

S2 Closed, S1 Open:

4-L Long. Sig. Gen. = 20 log (V_L / V_{RX})

C. Longitudinal Balance



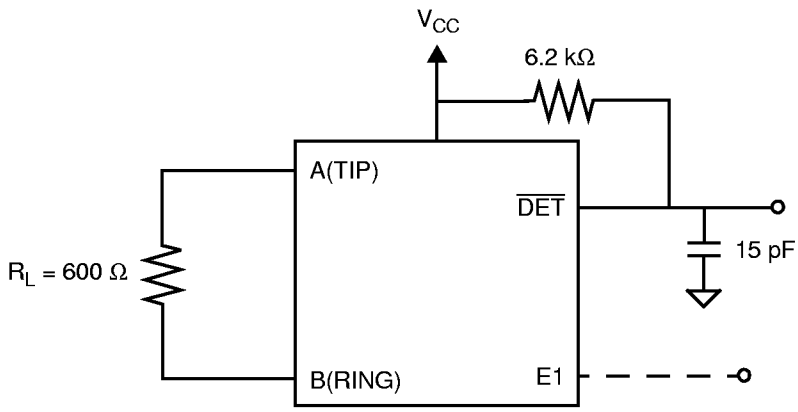
Note:

Z_D is the desired impedance (e.g., the characteristic impedance of the line).

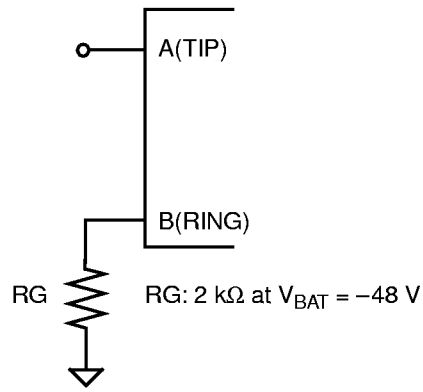
$R_L = 20 \log (2 V_M / V_S)$

D. Two-Wire Return Loss Test Circuit

TEST CIRCUITS (continued)

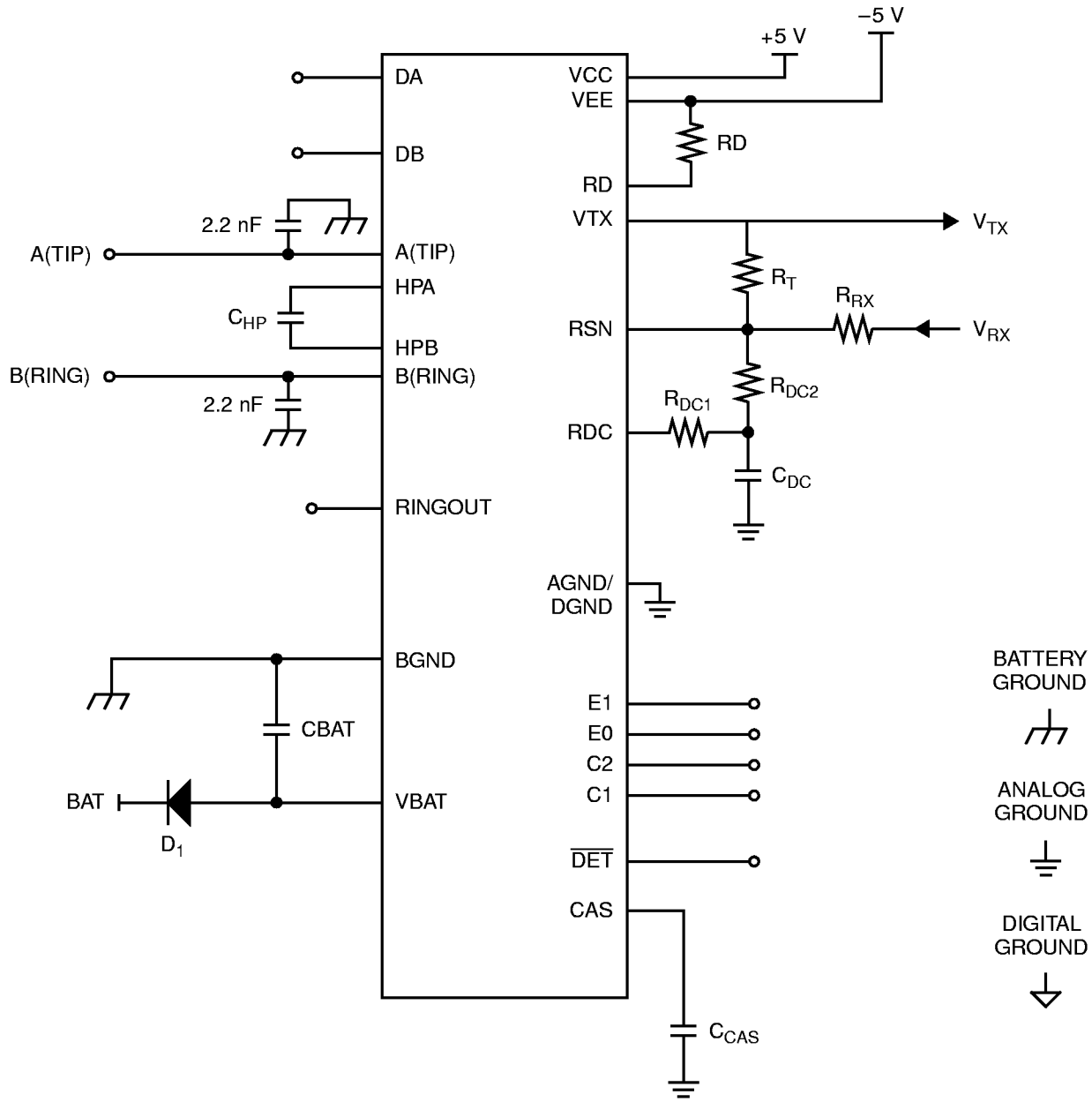


E. Loop-Detector Switching



F. Ground-Key Switching

TEST CIRCUITS (continued)



G. Am79467 Test Circuit

REVISION SUMMARY

Revision A to Revision B

- Minor changes to the data sheet style and format were made to conform to AMD standards.
- Electrical Characteristics—Under Longitudinal Performance, the specifications for Longitudinal to Metallic moved from the Typ column to the Min column.
- Table 2—The equation on the second row was revised.

Revision B to Revision C

- Minor changes to the data sheet style and format were made to conform to AMD standards.

MC

The Maximum Count bit is set whenever the timer reaches its final maximum count value. If the timer is configured in dual MAX COUNT register mode, this bit will be set each time the value in MAX COUNT register A is reached, and each time the value in MAX COUNT register B is reached. This bit is set regardless of the timer's interrupt-enable bit. The MC bit gives the user the ability to monitor timer status through software instead of through interrupts.

Programmers' intervention is required to clear this bit.

RTG

Retrigger bit is only active for internal clocking (EXT = 0). In this case it determines the control function provided by the input pin.

If RTG = 0, the input level gates the internal clock on and off. If the input pin is High, the timer will count; if the input pin is Low, the timer will hold its value. As indicated previously, the input signal may be asynchronous with respect to the 80C186 clock.

When RTG = 1, the input pin detects Low-to-High transitions. The first such transition starts the timer running, clearing the timer value to 0 on the first clock, and then incrementing thereafter. Further transitions on the input pin will again reset the timer to 0, from which it will start counting up again. If CONT = 0, when the timer has reached maximum count, the EN bit will be cleared, inhibiting further timer activity.

P

The Prescaler bit is ignored unless internal clocking has been selected (EXT = 0). If the P bit is a 0, the timer will count at one-fourth the internal CPU clock rate. If the P bit is a 1, the output of Timer 2 will be used as a clock for the timer. Note that the user must initialize and start Timer 2 to obtain the prescaled clock.

EXT

The External bit selects between internal and external clocking for the timer. The external signal may be asynchronous with respect to the 80C186 clock.

If this bit is set, the timer will count Low-to-High transitions on the input pin. If cleared, it will count an internal clock while using the input pin for control. In this mode, the function of the external pin is defined by the RTG bit. The maximum input to output transition latency time may be as much as six clocks. However, clock inputs may be pipelined as closely together as every four clocks without losing clock pulses.

ALT

The ALT bit determines which of two MAX COUNT registers is used for count comparison. If ALT = 0, register A for that timer is always used, while if ALT = 1, the comparison will alternate between register A and register B when each maximum count is reached. This alternation allows the user to change one MAX COUNT register while the other is being used, and thus provides a method of generating non-repetitive waveforms. Square waves and pulse outputs of any duty cycle are a subset of available signals obtained by not changing the final count registers. The ALT bit also determines the function of the timer output pin. If ALT is 0, the output pin will go Low for one clock, the clock after the maximum count is reached. If ALT is 1, the output pin will reflect the current MAX COUNT register being used (0/1 for B/A).

CONT

Setting the CONT bit causes the associated timer to run continuously, while resetting it causes the timer to halt upon maximum count. If CONT = 0 and ALT = 1, the timer will count to the MAX COUNT register A value, reset, count to the register B value, reset, and halt.

Not all mode bits are provided for Timer 2. Certain bits are hardwired as indicated below:

ALT = 0, EXT = 0, P = 0, RTG = 0, RIU = 0

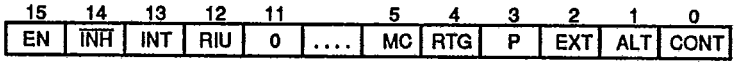
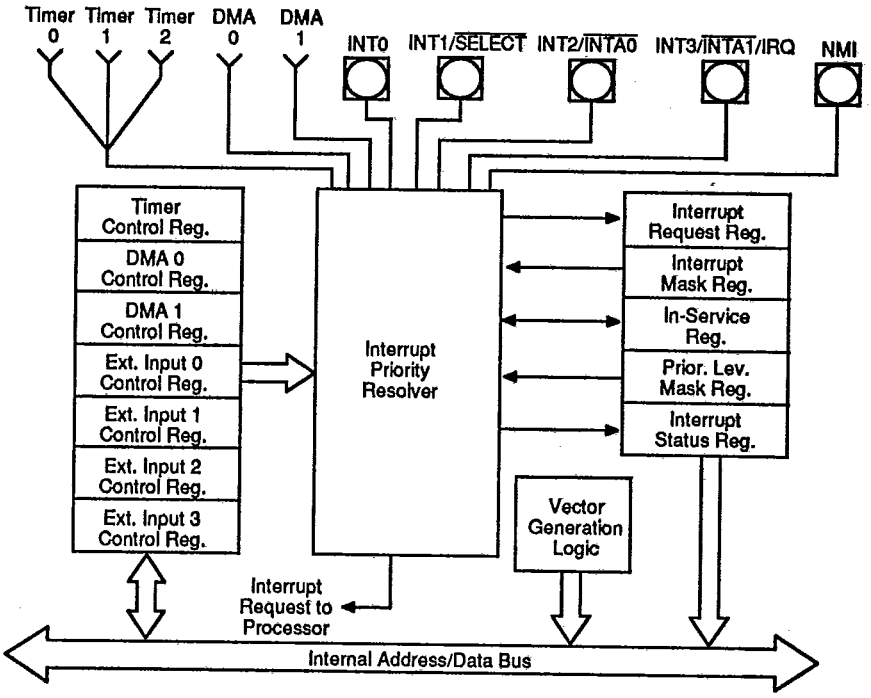


Figure 18. Timer Mode/Control Register 13087D-019



13087D-020

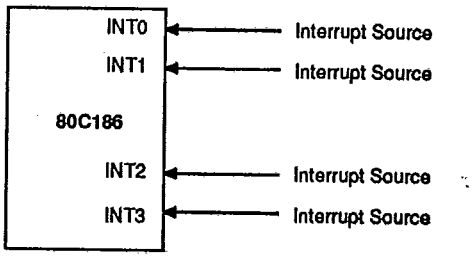
Figure 19. Interrupt Controller Block Diagram

Master Mode Features

Programmable Priority

The user can program the interrupt sources into any of eight different priority levels. The programming is done by placing a 3-bit priority level (0–7) in the control register of each interrupt source. (A source with a priority level of 4 has higher priority over all priority levels from 5 to 7. Priority registers containing values lower than 4 have greater priority.) All interrupt sources have preprogrammed default priority levels (see Table 3).

If two requests with the same programmed priority level are pending at once, the priority ordering scheme shown in Table 3 is used. If the serviced interrupt routine reenables interrupts, it allows other interrupt requests to be serviced.



13087D-021

Figure 20. Fully Nested (Direct) Mode Interrupt Controller Connections

SWITCHING CHARACTERISTICS (continued) T-49-17-15

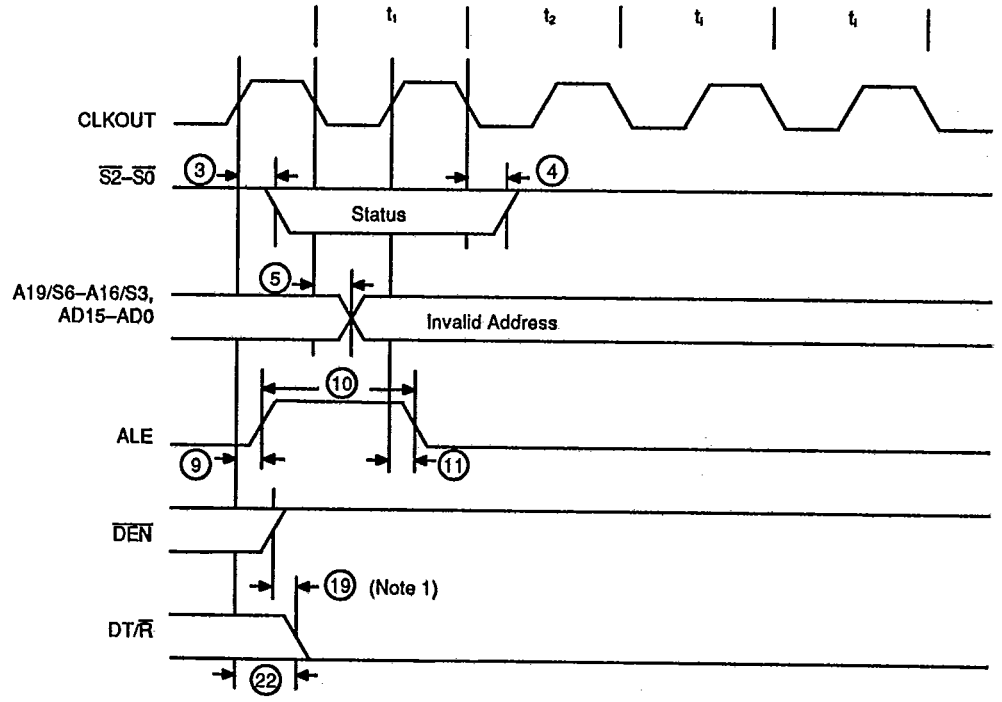
Software Halt Cycle Timings

T_A = 0°C to +70°C, V_{CC} = 5 V ±10% except V_{CC} = 5 V ±5% at f > 12.5 MHz

No	Symbol	Parameter	Preliminary								Unit
			80C186		80C186-12		80C186-16		80C186-20		
			Min	Max	Min	Max	Min	Max	Min	Max	
80C186 General Timing Responses (Listed More Than Once)											
3	t_{CHSV}	Status Active Delay	5	45	5	35	5	31	5	25	ns
4	t_{CLSH}	Status Inactive Delay	5	46	5	35	5	30	5	25	ns
5	t_{CLAV}	Address Valid Delay	5	44	5	36	5	33	5	30	ns
9	t_{CHLH}	ALE Active Delay		30		25		20		20	ns
10	t_{LHLL}	ALE Width	$t_{CLCL}-15$		$t_{CLCL}-15$		$t_{CLCL}-15$		$t_{CLCL}-15$		ns
11	t_{CHLL}	ALE Inactive Delay		30		25		20		20	ns
19	t_{OXDL}	$\overline{DEN}$ Inactive to DT/$\overline{R}$ Low*		0		0		0	0	0	ns
22	t_{CHCTV}	Control Active Delay 2	5	44	5	37	5	31	5	27	ns

All timings are measured at 1.5 V and 100 pF loading on CLKOUT unless otherwise noted.
All output test conditions are with C_L = 50–200 pF (10 MHz) and C_L = 50–100 pF (12.5–20 MHz).
For AC tests, input V_{IL} = 0.45 V and V_{IH} = 2.4 V except at X_1 where V_{IH} = V_{CC} − 0.5 V.
*Equal Loading

Software Halt Cycle Waveforms



Note: 1. For write cycle followed by halt cycle.

SWITCHING CHARACTERISTICS (continued)

Clock Timings

T_A = 0°C to +70°C, V_{CC} = 5 V ±10% except V_{CC} = 5 V ±5% at f > 12.5 MHz

No	Symbol	Parameter	Preliminary 80C186 Min	80C186 Max	80C186-12 Min	80C186-12 Max	80C186-16 Min	80C186-16 Max	80C186-20 Min	80C186-20 Max	Unit
80C186 CLKIN Requirements Measurements taken with following conditions. External clock input to X1 and X2 not connected (float).											
36	t_{CKIN}	CLKIN Period	50		40		31.25		25		ns
37	t_{CLCK}	CLKIN Low Time 1.5 V[2]	20		16		13		7		ns
38	t_{CHCK}	CLKIN High Time 1.5 V[2]	20		16		13		8		ns
39	t_{CKHL}	CLKIN Fall Time 3.5 to 1.0 V		5		5		5		5	ns
40	t_{CKLH}	CLKIN Rise Time 1.0 to 3.5 V		5		5		5		5	ns
80C186 CLKOUT Timing											
41	t_{CICO}	CLKIN to CLKOUT Skew		25		21		17		13	ns
42	t_{CLCL}	CLKOUT Period	100		80		62.5		50		ns
43	t_{CLCH}	CLKOUT Low Time									
		C_L = 100 pF[2]	0.5 t_{CLCL}−8		0.5 t_{CLCL}−7		0.5 t_{CLCL}−7		0.5 t_{CLCL}−7		ns
		C_L = 50 pF[3]	0.5 t_{CLCL}−6		0.5 t_{CLCL}−5		0.5 t_{CLCL}−5		0.5 t_{CLCL}−5		ns
44	t_{CHCL}	CLKOUT High Time									
		C_L = 100 pF[4]	0.5 t_{CLCL}−8		0.5 t_{CLCL}−7		0.5 t_{CLCL}−7		0.5 t_{CLCL}−7		ns
		C_L = 50 pF[3]	0.5 t_{CLCL}−6		0.5 t_{CLCL}−5		0.5 t_{CLCL}−5		0.5 t_{CLCL}−5		ns
45	t_{CH1CH2}	CLKOUT Rise Time 1.0 to 3.5 V		10		10		10		10	ns
46	t_{CL2CL1}	CLKOUT Fall Time 3.5 to 1.0 V		10		10		10		10	ns

All timings are measured at 1.5 V and 100 pF loading on CLKOUT unless otherwise noted.
All output test conditions are with C_L = 50–200 pF (10 MHz) and C_L = 50–100 pF (12.5–20 MHz).
For AC tests, input V_{IL} = 0.45 V and V_{IH} = 2.4 V except at X_1 where V_{IH} = V_{CC} − 0.5 V.

Notes: 1. t_{CLCK} and t_{CHCK} (CLKIN Low and High times) should not have a duration less than 40% of t_{CKIN}.
2. Tested under worst case conditions: V_{CC} = 5.5 V (5.25 V @ 20 MHz), T_A = 70°C.
3. Not tested.
4. Tested under worst case conditions: V_{CC} = 4.5 V (4.75 V @ 20 MHz), T_A = 0°C.

Clock Waveforms