MOS INTEGRATED CIRCUIT
μPD9324

COLOR DEMODULATION LSI (CDU) FOR IMPROVED DEFINITION TV

DESCRIPTION

The μPD9324 is a color demodulation LSI (CDU) for improved definition TV (IDTV). This LSI demodulates color by multiplying the color subcarrier and the color signal being processed for YC process.

In combination with five LSIs (YCS, YCP, YCI, MDP, and CKG), this LSI can be used to configure an IDTV signal processing system.

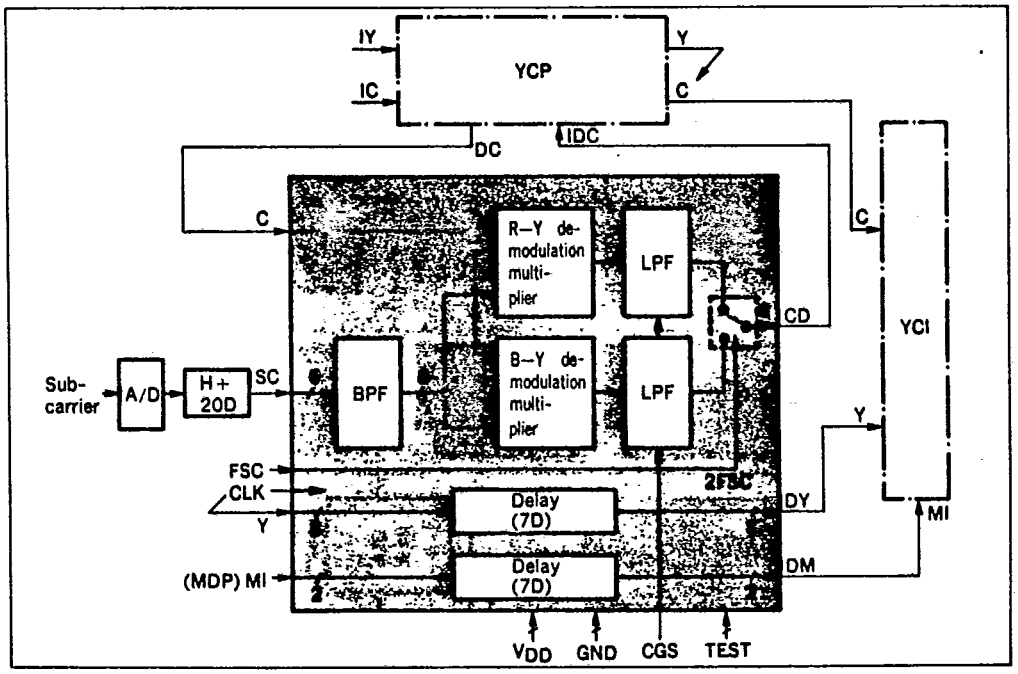
CHARACTERISTICS

- Capable of color demodulation based on the line lock clock.
- Has two built-in multiplier circuits for color demodulation.
- R-Y/B-Y sequential output.
- +5 volt single power supply.
- Low power consumption due to CMOS circuitry.

ORDERING INFORMATION

Part Number	Package
μPD9324GF-3B8	64 PIN PLSTIC QFP (14 x 20)

BLOCK DIAGRAM



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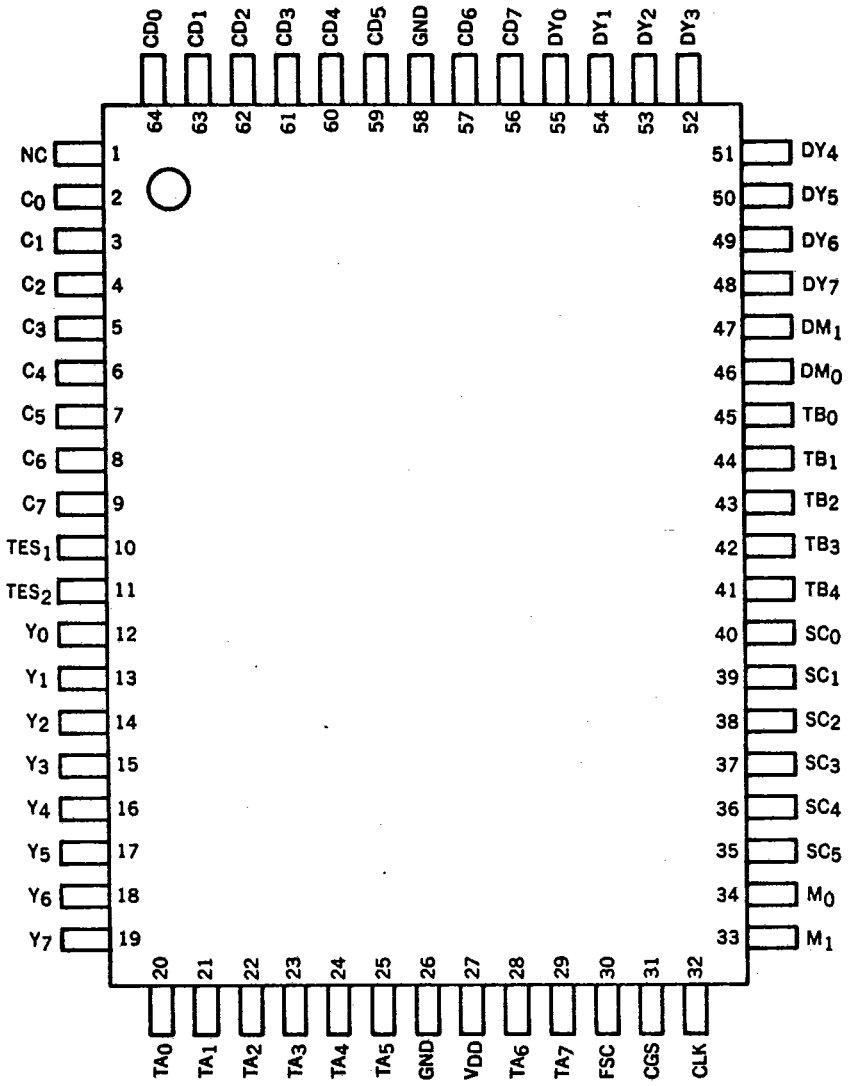
CONNECTION DIAGRAM (Top View)



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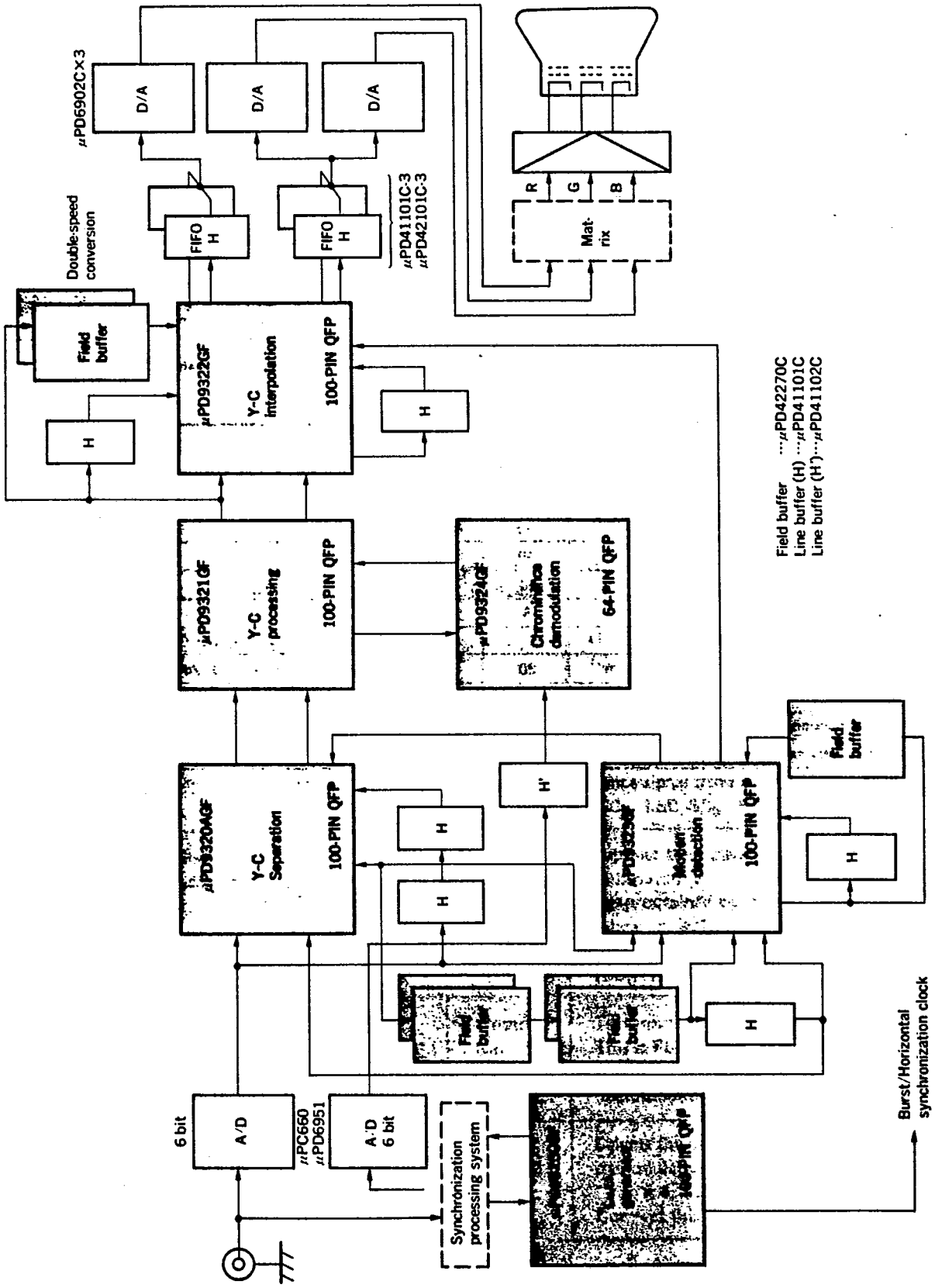
LSI SYSTEM CONFIGURATION FOR THE IDTV



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ABSOLUTE MAXIMUM RATINGS (T_a = 25 °C)

Source Voltage	V_{DD}	−0.5 to 7.0	V
Input Voltage	V_{IN}	−0.5 to V_{DD} +0.5	V
Output Current	I_{OUT}	20	mA
Package Allowable Dissipation	P_D	400	mW
Operating Temperature	T_{opt}	−20 to +75	°C
Storage Temperature	T_{stg}	−65 to +150	°C

RECOMMENDED OPERATING CONDITIONS (T_a = −20 to +75 °C)

CHARACTERISTIC	SYMBOL	MIN.	TYP.	MAX.	UNIT	TEST CONDITIONS
Source Voltage	V_{DD}	4.5	5.0	5.5	V	
Low-Level Input Voltage	V_{IL}	0		0.3 V_{DD}	V	Input terminals: Y, M, C, FSC, CGS, and CLK (CMOS input)
High-Level Input Voltage	V_{IH}	0.7 V_{DD}			V	
Low-Level Input Voltage	V_{IL}	0		0.8	V	Input terminals: SC (TTL input)
High-Level Input Voltage	V_{IH}	2.4			V	
Clock Frequency	F_{CLK}		14.3		MHz	

ELECTRICAL CHARACTERISTICS (V_{DD} = 5 V ±10 %, T_a = −20 to +75 °C)

CHARACTERISTIC	SYMBOL	MIN.	TYP.	MAX.	UNIT	TEST CONDITIONS
Supply Current	I_{DD}		40		mA	
Low-Level Output Current	I_{OL}	4	11		mA	V_{OL} = 0.4 V
High-Level Output Current	$-I_{OH}$	4	8		mA	V_{OH} = V_{DD} −0.4 V
Input Current	$\pm I_I$			10	μA	V_I = V_{DD} or GND
Input Current	$-I_I$	25	80	260	μA	V_I = GND: Pull-up resistor input
Output Delay Time	T_d		18		ns	
Input Terminal Capacitance	C_{IN}			10	pF	V_{DD} = V_I = 0 f = 1 MHz
Output Terminal Capacitance	C_{OUT}			15	pF	

TERMINAL DESCRIPTION

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TERMINAL SYMBOL	TERMINAL NAME	TERMINAL NUMBER	FUNCTIONS	
Y_0 to Y_7	Luminance input	12 to 19	Input (CMOS)	Inputs the luminance signal output from the YCP. This input process is used to delay the main line signal of the luminance signal by seven clocks. (Y_0: LBS, Y_7: MSB)
DY_0 to DY_7	Delayed luminance output	55 to 48	Output (CMOS)	This output is supplied to the YCI. Outputs the Y input delayed by seven clocks. (DY_0: LBS, DY_7: MSB)
M_0 M_1	Motion signal input	34 33	Input (CMOS)	Inputs the Y interpolation motion signal output, MI, from the MDP. This input process is used to delay the motion signal supplied to the YCI by seven clocks. (M_0: LSB, M_1: MSB)
DM_0 DM_1	Delayed motion signal output	46 47	Output (CMOS)	Outputs the signal to the YCI. Outputs the Y interpolation motion signal delayed by seven clocks. (DM_0: LSB, DM_1: MSB)
C_0 to C_7	Chrominance input	2 to 9	Input (CMOS)	Inputs the chrominance signal output from the YCP. This input signal is used to demodulate the chrominance signal coming through the ACC. (C_0: LSB, C_7: MSB)
SC_0 to SC_5	Subcarrier A/D input	40 to 35	Input (TTL)	Inputs the six-bit signal obtained from the subcarrier waveform through A/D conversion. This signal is the reference signal for chrominance signal demodulation. (SC_0: LSB, SC_5: MSB)
CD_0 to CD_7	Chrominance demodulation output	64 to 59 57 to 56	Output (CMOS)	Supplies the output to the YCP. This output is the demodulated chrominance input obtained by multiplication by the subcarrier A/D. Alternately outputs the R-Y and B-Y signals. (CD_0: LSB, CD_7: MSB)
FSC	Subcarrier input	30	Input (CMOS)	The input is supplied by the CKG. This is FSC (3.58 MHz) signal used for determining the phase of the chrominance demodulation output.
CGS	Chrominance gain selection	31	Input (CMOS) Pull-up R	Selects the gain in the chrominance demodulation output. (0 ... x 4, 1 ... x 2) Connect this terminal to the V_{DD}.

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TERMINAL SYMBOL	TERMINAL NAME	TERMINAL NUMBER	FUNCTIONS	
CLK	Clock	32	Input (CMOS)	This input is supplied by the CKG. This clock is the 4 F_{SC} (14.3 MHz) system clock.
TES1 TES2	Test input	10 11	Input Pull-up R	Test input terminal. Connect this terminal to V_{DD}.
TA_0 to TA_7	Test output A	20 to 25 28 to 29	Output	Test output terminal.
TB_0 to TB_4	Test output B	45 to 41	Output	Test output terminal.
V_{DD}	Power terminal	26		Supply input terminal. Apply +5 volts to this terminal.
GND	Grounding terminal	27 58		This is a grounding terminal.

DESCRIPTION OF FUNCTIONS

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The μPD9324 color-demodulates the chrominance signal from the μPD9321 (YCP).

1. Color Demodulation Circuit

This circuit performs color demodulation multiplication, using the subcarrier A/D signal (SC), which is the reference color phase signal, on the 8-bit chrominance signal provided through ACC process by the μPD9321 (YCP), and returns its output to the YCP as the sequential R-Y/B-Y signal.

1-1 Chrominance Input

The chrominance input is supplied from the μPD9321 (YCP). This input is the eight-bit signal obtained through the ACC (Automatic color gain control) process of the 12-bit chrominance input from the μPD9320A (YCS).

1-2 Subcarrier A/D Input

This circuit is able to use its own clock as the reference color phase to demodulate the color signal using the burst lock system clock.

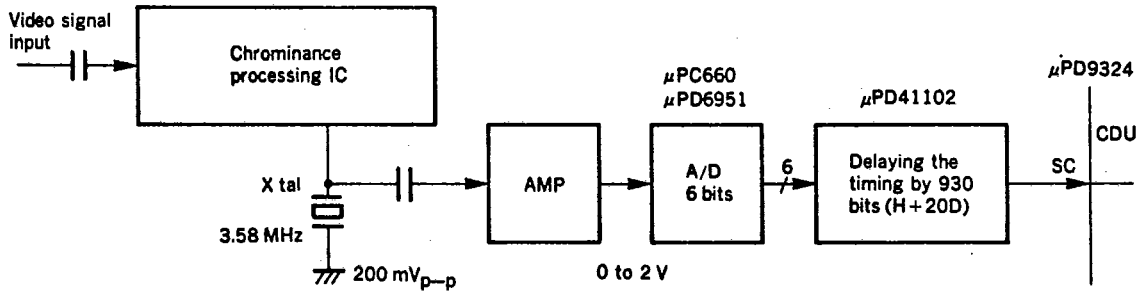
In color demodulation using the line lock system clock, however, this circuit cannot use its own clock as the reference color phase. Thus, the reference color phase signal must be supplied externally.

The subcarrier A/D signal (SC) serves this purpose. This signal is obtained by digitizing the sine wave output of a crystal oscillator having a frequency of 3.58 MHz (F_{SC}) that is phase-locked to the synchronization signal processing burst signal, using the six-bit A/D converter.

To make the color demodulation delay time conform with the main line color signal phase, the above signal is delayed by 930 bits by the μPD41102 line buffer.

Note: Invert the MSB (SC5) of the SC input with the inverter.

Fig. 1 Subcarrier A/D Input

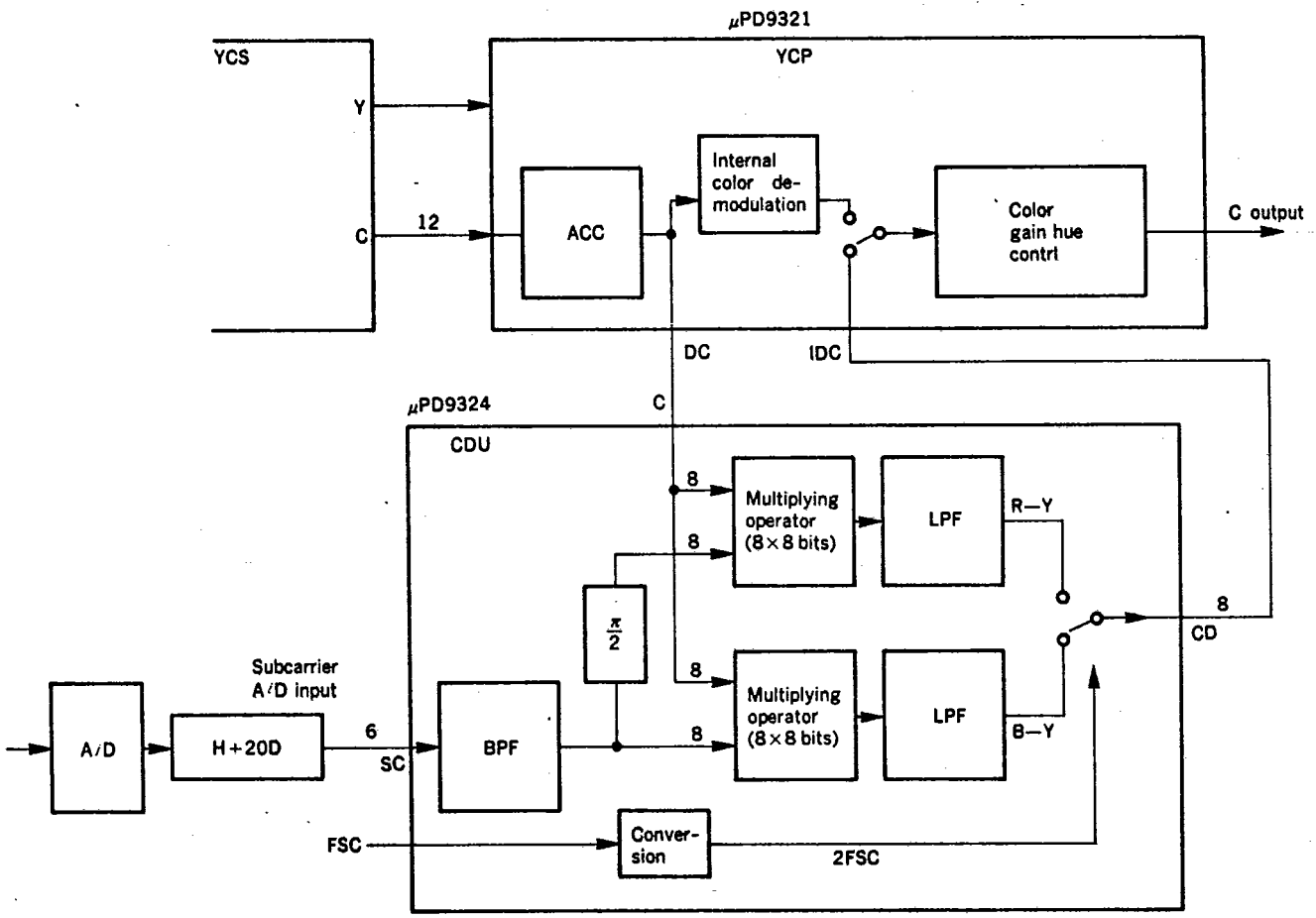


1-3 Color Demodulation

Two 8 x 8 bit multipliers are used for color demodulation. The R-Y and B-Y signals are demodulated from the chrominance signal.

To make the six-bit subcarrier A/D signal conform with the eight-bit chrominance signal, the former is converted into an eight-bit signal with the BPF. These two signals are then multiplied to perform color demodulation of the B-Y signal. The R-Y signal is demodulated by multiplying the subcarrier signal shifted by 90 degrees with the chrominance signal.

Fig. 2 Block Diagram of Color Demodulation



1-4 LPF and Sequential Conversion

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The color-demodulated R-Y and B-Y signals remove the 7 MHz folded signal using the LPF.

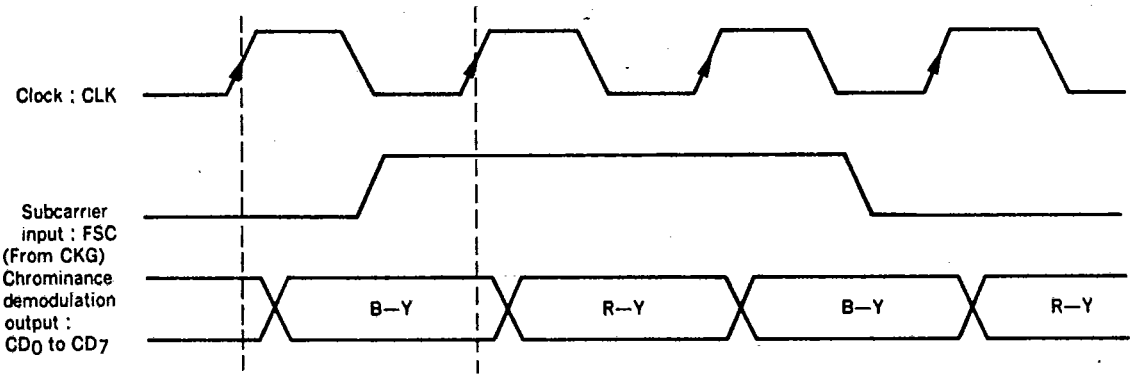
The phases of the LPF-processed R-Y/B-Y signals are synchronized with that of the FSC signal (3.58 MHz) input from the μPD9325 then converted into sequential signals that output R-Y and B-Y signal alternately at every 4 F_{SC} clock and returned to the μPD9321 (YCP).

In the above process, the output gain can be controlled by the chrominance gain selection terminal (CGS). In the standard operation, this terminal is connected to V_{DD}. (x 2).

CGS = "1": x 2 gain
= "0": x 4 gain

Note: In the "x 2" gain, the over-all gain in the color demodulation is unity (x 1).

Fig. 3 Chrominance Demodulation Output Timing Chart



2. Y Signal Delaying Circuit

This circuit delays the luminance signal by seven clocks.

This circuit delays the luminance output from the μPD9321 (YCP) by seven clocks and outputs it to the μPD9322 (YCI).

3. Motion Signal Delaying Circuit

This circuit delays the Y interpolation signal by seven clocks.

This circuit delays the Y interpolation motion signal output from the μPD9323 (MDP) by seven clocks and outputs it to the μPD9322 (YCI).

APPLICATION CIRCUIT: EXAMPLE

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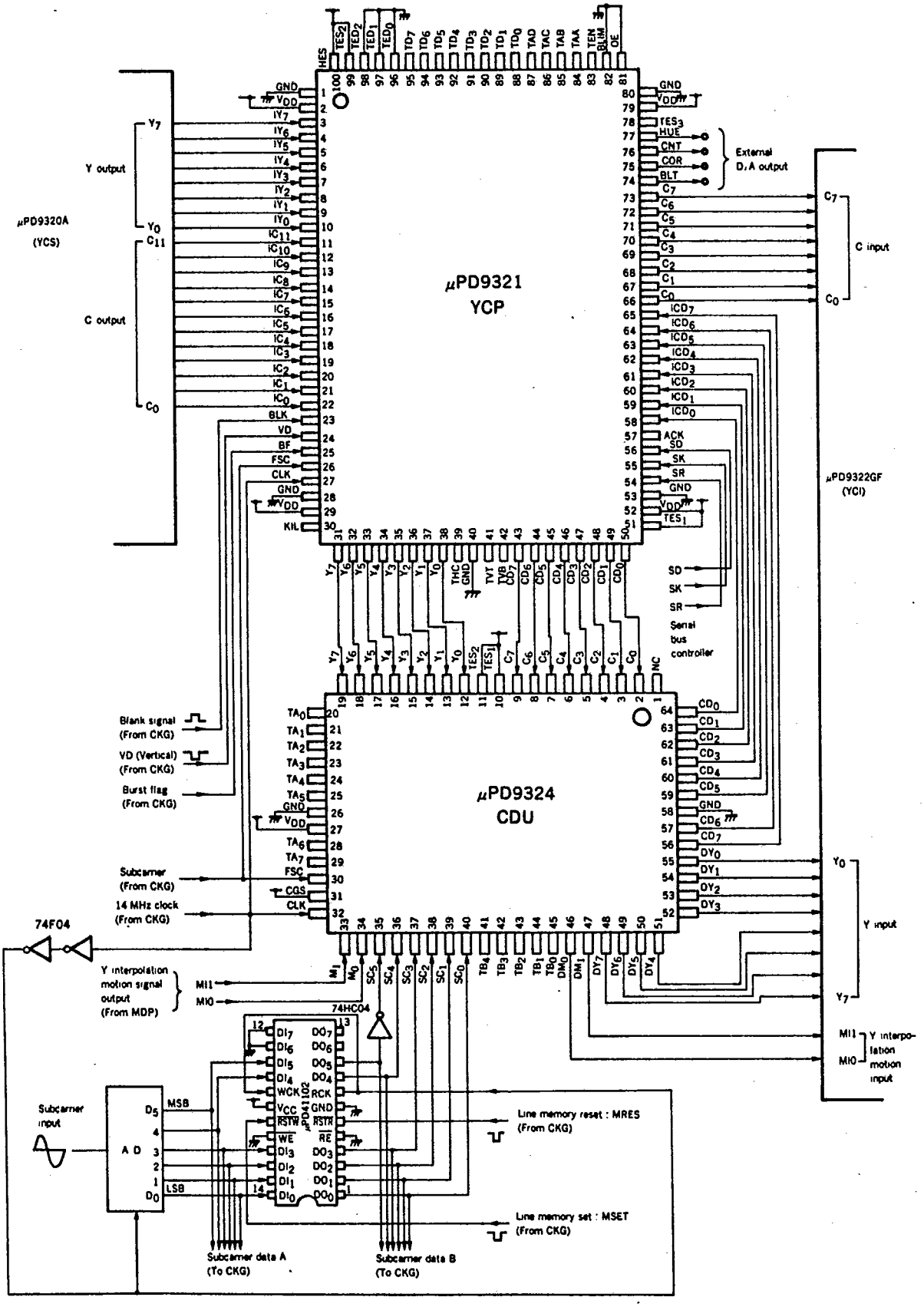

64-PIN PLASTIC QFP (14 x 20)

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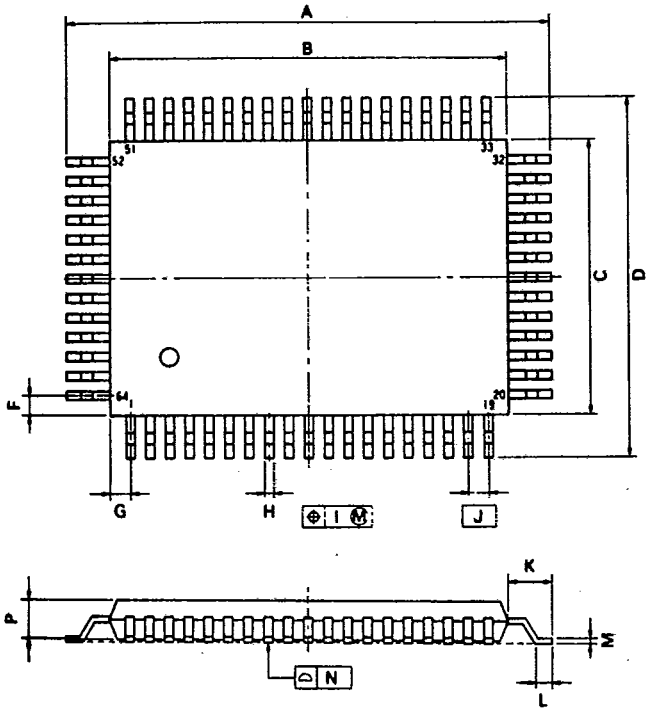

P64GF-100-3B8,3BE-1

NOTE

Each lead centerline is located within 0.20 mm (0.008 inch) of its true position (T.P.) at maximum material condition.

ITEM	MILLIMETERS	INCHES
A	$23.6^{+0.4}$	$0.929^{+0.016}$
B	$20.0^{+0.2}$	$0.795^{+0.009}_{-0.008}$
C	$14.0^{+0.2}$	$0.551^{+0.009}_{-0.008}$
D	$17.6^{+0.4}$	$0.693^{+0.016}$
F	1.0	0.039
G	1.0	0.039
H	$0.40^{+0.10}$	$0.016^{+0.004}_{-0.005}$
I	0.20	0.008
J	1.0 (T.P.)	0.039 (T.P.)
K	$1.8^{+0.2}$	$0.071^{+0.008}_{-0.009}$
L	$0.8^{+0.2}$	$0.031^{+0.008}_{-0.009}$
M	$0.15^{+0.10}_{-0.05}$	$0.006^{+0.004}_{-0.003}$
N	0.15	0.006
P	2.7	0.106
Q	$0.1^{\pm0.1}$	$0.004^{\pm0.004}$
R	$0.1^{\pm0.1}$	$0.004^{\pm0.004}$
S	3.0 MAX.	0.119 MAX.