TOSHIBA Bipolar Linear Integrated Circuit Silicon Monolithic

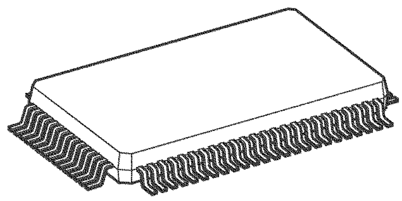
TA1360AFG

YCbCr/YPbPr Signal and Sync Processor for Digital TV, Progressive Scan TV and Double Scan TV

The TA1360AFG integrates an analog component signal (YCbCr/YPbPr) processor and sync processor in a 80-pin QFP plastic package. The IC is ideal for digital TVs, progressive TVs, and double scan TVs.

The luminance block and the color difference block incorporate the high performance signal processing circuits. The sync processor block supports 525I/60, 625I/50, 525P/60, 625P/50, 1125I/50, 1125I/60, 750P/60, (750P/50), PAL100 Hz, NTSC120 Hz, and SVGA/60(VESA).

The TA1360AFG incorporates the I²C bus. The device can control various functions via the bus line.



QFP80-P-1420-0.80F

Weight: 1.6 g (typ.)

Features

Luminance Block

- Black stretch circuit and DC restoration rate correction circuit
- Dynamic γ correction circuit (gray scale correction)
- SRT (LTI)
- Y group delay correction (shoot balance correction)
- High-bright color circuit
- Color detail enhancer (CDE)
- White pulse limiter (WPL)
- VSM output

Color difference Block

- Fresh color correction
- Dynamic Y/C correction circuit
- Color SRT (CTI)
- Color γ circuit
- Green stretch
- Blue stretch

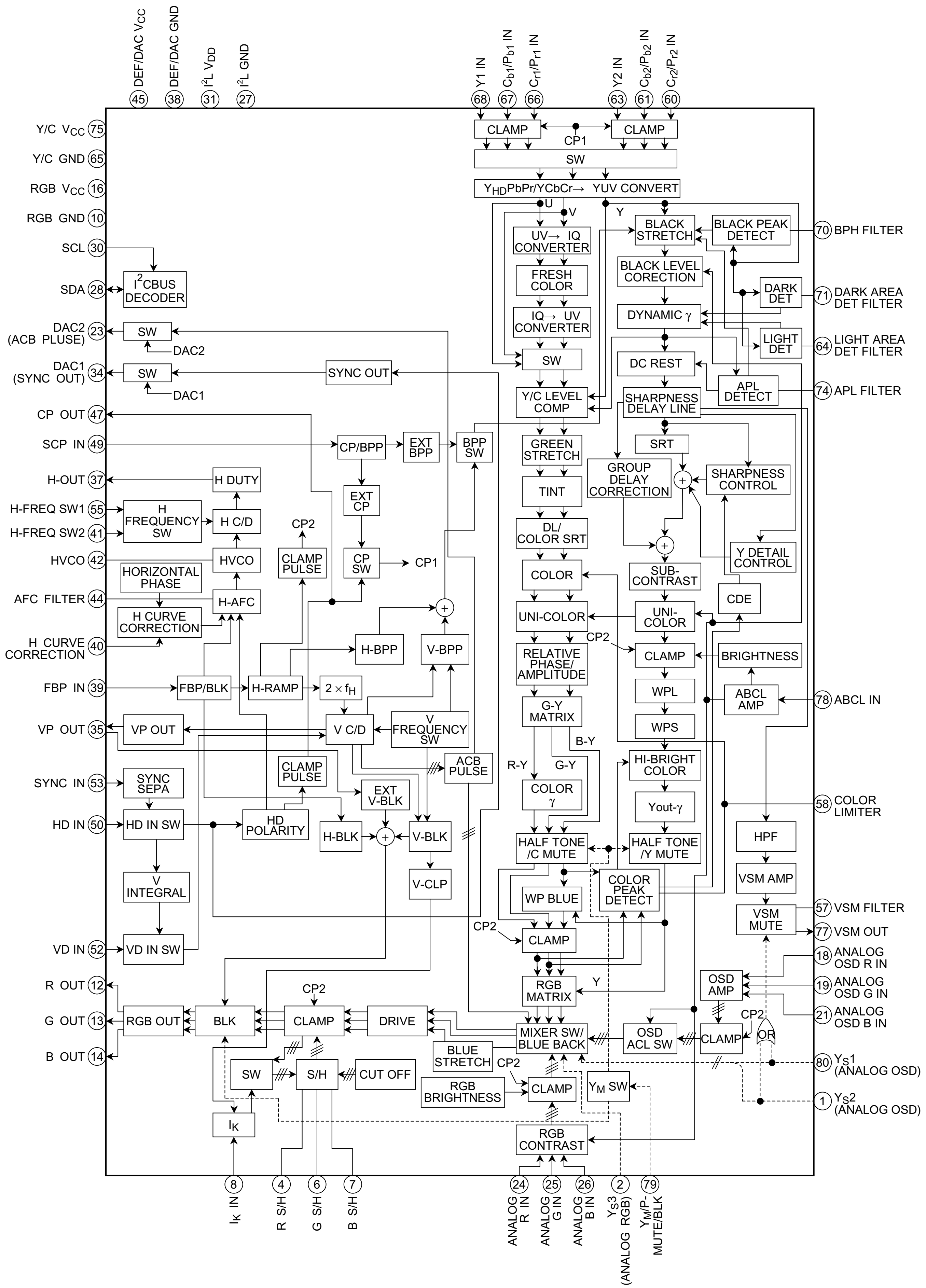
Text Block

- OSD blending SW
- ACB (only black level)
- Two analog RGB inputs

Synchronization Block

- Horizontal sync (15.75 k, 28.125 k, 31.5 k, 33.75 k, 37.9 k, 45 kHz)
- Vertical sync (525I/P, 625I/P, 750P, 1125I/P, PAL 100 Hz/NTSC 120 Hz
- 2- and 3-level sync separator circuit
- HD/VD input (positive and negative polarities)
- Copy guard
- Vertical blanking

Block Diagram



Pin Assignment

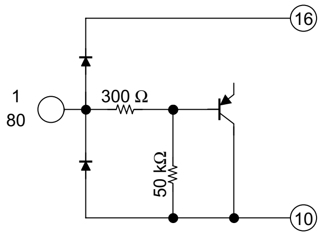
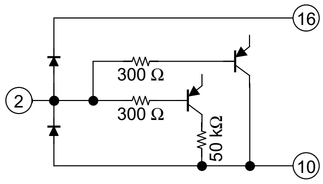
TA1360AFG

1	Y_S2 (ANALOG OSD)	41	H-FREQUENCY SW2
2	Y_S3 (ANALOG RGB)	42	HVCO
3	NC	43	NC
4	R S/H	44	AFC FILTER
5	NC	45	DEF/DAC V_{CC}
6	G S/H	46	NC
7	B S/H	47	CP OUT
8	I_K IN	48	NC
9	NC	49	SCP IN
10	RGB GND	50	HD IN
11	NC	51	NC
12	R OUT	52	VD IN
13	G OUT	53	SYNC IN
14	B OUT	54	NC
15	NC	55	H-FREQ SW1
16	RGB V_{CC}	56	NC
17	NC	57	VSM FILTER
18	ANALOG OSD R IN	58	COLOR LIMITER
19	ANALOG OSD G IN	59	NC
20	NC	60	C_{r2}/P_{r2} IN
21	ANALOG OSD B IN	61	C_{b2}/P_{b2} IN
22	NC	62	NC
23	DAC2 (ACB PULSE)	63	Y2 IN
24	ANALOG R IN	64	LIGHT AREA DET FILTER
25	ANALOG G IN	65	Y/C GND
26	ANALOG B IN	66	C_{r1}/P_{r1} IN
27	I^2L GND	67	C_{b1}/P_{b1} IN
28	SDA	68	Y1 IN
29	NC	69	NC
30	SCL	70	BPH FILTER
31	I^2L V_{DD}	71	DARK AREA DET FILTER
32	NC	72	NC
33	NC	73	NC
34	DAC1 (SYNC OUT)	74	APL FILTER
35	VP OUT	75	Y/C V_{CC}
36	NC	76	NC
37	H-OUT	77	VSM OUT
38	DEF/DAC GND	78	ABCL IN
39	FBP IN	79	Y_M/P-MUTE/BLK
40	H COURVE CORRECTION	80	Y_S1 (ANALOG OSD)

Pin Functions

<table>
<tr><th>Pin No.</th><th>Pin Name</th><th>Function</th><th>Interface Circuit</th><th>Input Signal/Output Signal</th></tr>
<tr><td>1

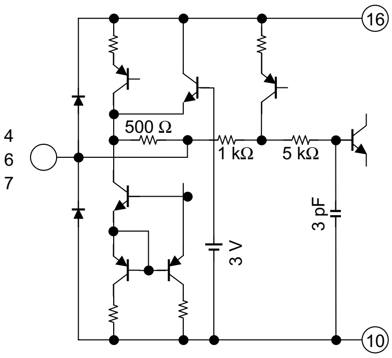
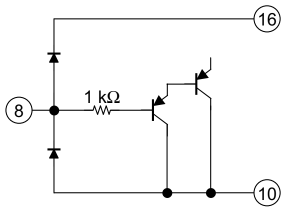
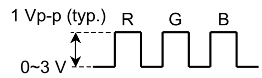
80</td><td>Y_S2 (analog OSD)

Y_S1 (analog OSD)</td><td>Switches internal RGB and OSD input signals.
The blend ratio of internal RGB and OSD signals can be adjusted according to applying voltage to pins Y_S1 and Y_S2.
VSM output is muted when Y_S1 or Y_S2 pin is set to High.
<table>
<tr><th>Y_S2</th><th>Y_S1</th><th>Blend ratio Int RGB: OSD RGB</th></tr>
<tr><td>L</td><td>L</td><td>10:0</td></tr>
<tr><td>H</td><td>L</td><td>7:3</td></tr>
<tr><td>L</td><td>H</td><td>5:5</td></tr>
<tr><td>H</td><td>H</td><td>0:10</td></tr>
</table></td><td>
</td><td>0 to 0.5 V : Internal
1.1 V to 1.7 V : VSM Mute
2.9 V to 9 V : OSD, VSM Mute</td></tr>
<tr><td>2</td><td>Y_S3 (analog RGB)</td><td>Switches internal RGB and external analog RGB input.
VSM output is muted when analog RGB is selected.</td><td>
</td><td>0 to 0.5 V : Internal
1.5 V to 9 V : Analog RGB, VSM Mute</td></tr>
<tr><td>3</td><td>NC</td><td>This pin is not used.
Connect to GND.</td><td>—</td><td>—</td></tr>
<tr><td>4

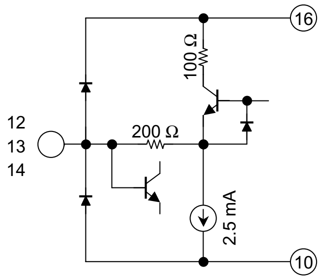
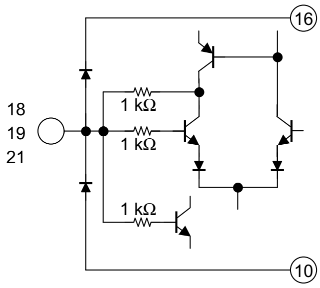
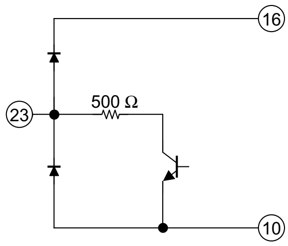
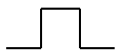
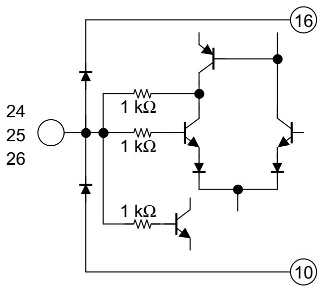
6

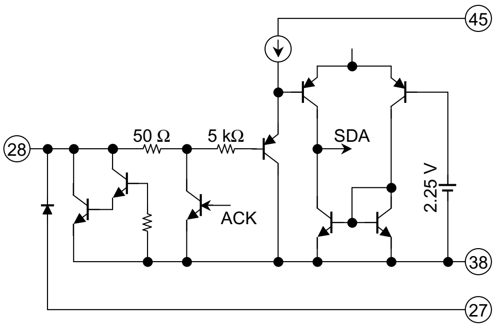
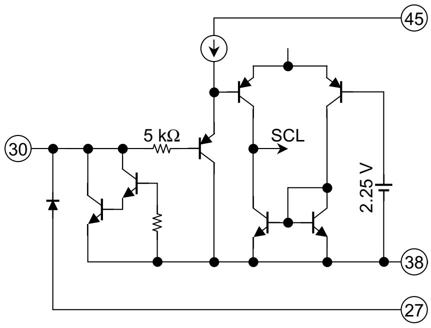
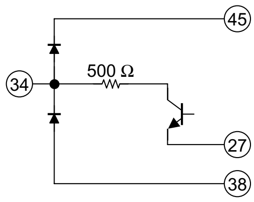
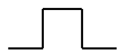
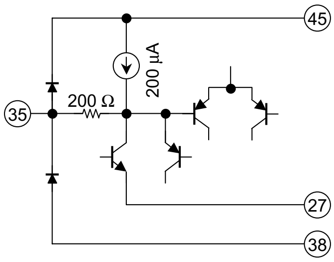
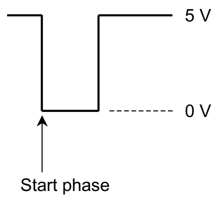
7</td><td>R S/H

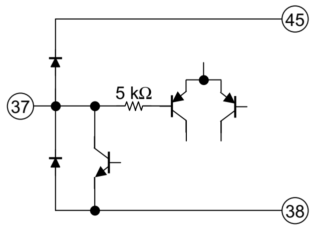
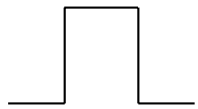
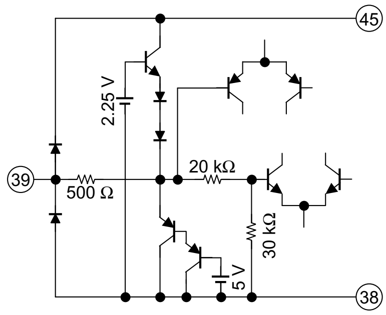
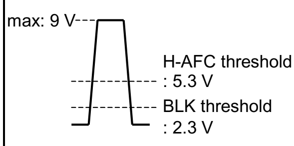
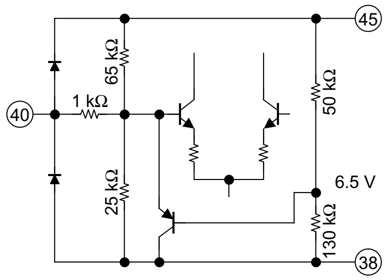
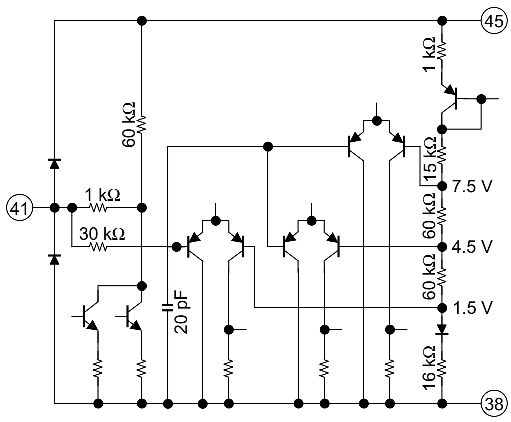
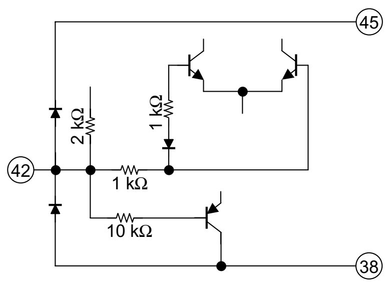
G S/H

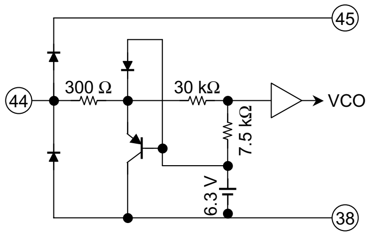
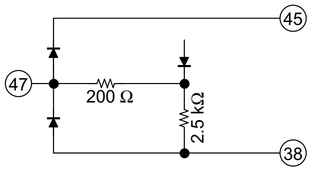
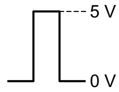
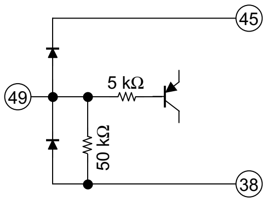
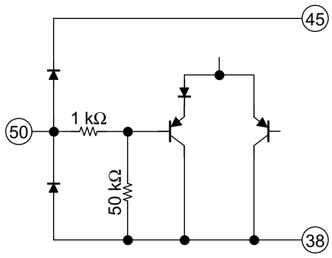
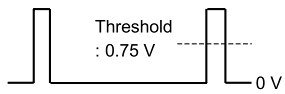
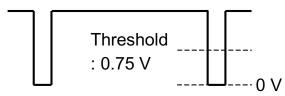
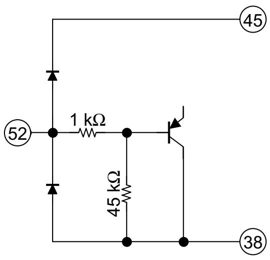
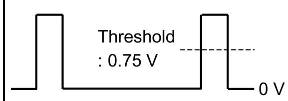
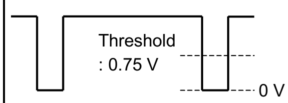
B S/H</td><td>S/H (sample-and-hold) pin.
In ACB Mode, connect 2.2-µF capacitor. In CUT-OFF Mode, connect 0.01-µF capacitor.</td><td>
</td><td>DC</td></tr>
<tr><td>5</td><td>NC</td><td>This pin is not used.
Connect to GND.</td><td>—</td><td>—</td></tr>
<tr><td>8</td><td>I_K IN</td><td>Inputs feedback signal from CRT. (BLK level should be 0 to 3 V.)
When ACB function is not used, connect this pin to RGB V_{CC} pin.</td><td>
</td><td>

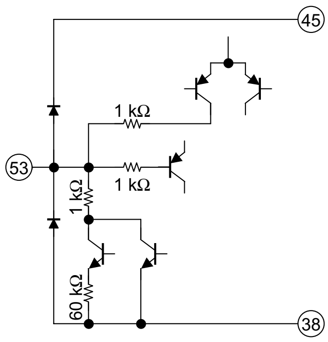
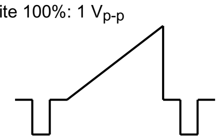
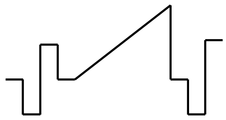
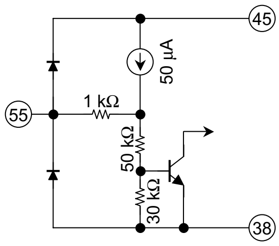
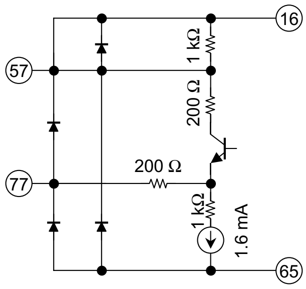
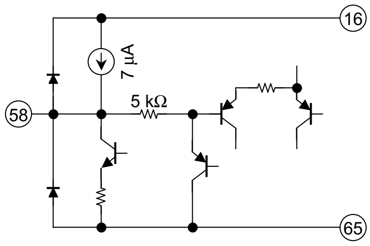
or RGB V_{CC}</td></tr>
<tr><td>9</td><td>NC</td><td>This pin is not used.
Connect to GND.</td><td>—</td><td>—</td></tr>
<tr><td>10</td><td>RGB GND</td><td>GND pin for text/RGB block</td><td>—</td><td>—</td></tr>
<tr><td>11</td><td>NC</td><td>This pin is not used.
Connect to GND.</td><td>—</td><td>—</td></tr>
</table>

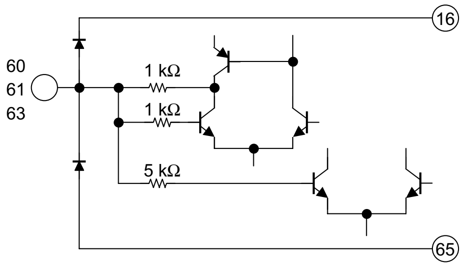
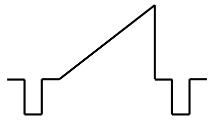
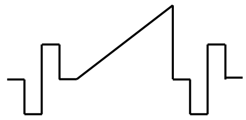
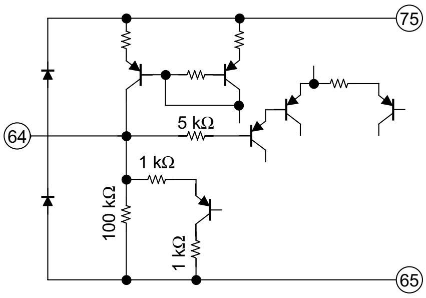
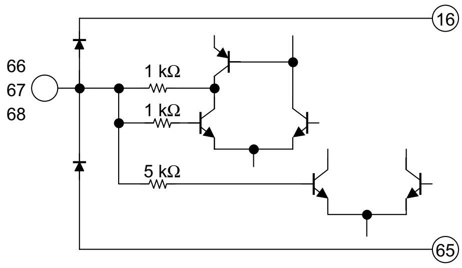
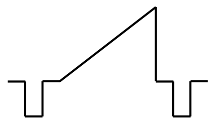
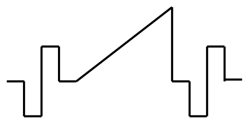
Pin No.	Pin Name	Function	Interface Circuit	Input Signal/Output Signal
12 13 14	R OUT G OUT B OUT	Outputs R/G/B signal. Recommended output amplitude: 100 IRE = 2.3 Vp-p		100 IRE: 2.3 Vp-p Conditions: UNI-COLOR = max SUB-CONT = Cent Y IN = 0.7 Vp-p
15	NC	This pin is not used. Connect to GND.	—	—
16	RGB V_{CC}	V_{CC} pin for text/RGB block. See “Maximum Ratings” about the supply voltage.	—	—
17	NC	This pin is not used. Connect to GND.	—	—
18 19 21	ANALOG OSD R IN ANALOG OSD G IN ANALOG OSD B IN	Inputs analog OSD signal via clamp capacitor.		100 IRE: 0.7 Vp-p (not including sync)
20 22	NC	This pin is not used. Connect to GND.	—	—
23	DAC2 (ACB pulse)	Outputs 1-bit DAC or pulse over ACB period. Open-collector output.		DC or ACB PULSE 
24 25 26	ANALOG R IN ANALOG G IN ANALOG B IN	Inputs analog R/G/B signal via clamp capacitor.		100 IRE: 0.7 Vp-p (not including sync)
27	I^2L GND	GND pin for I^2L block	—	—

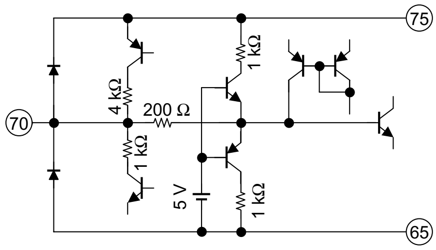
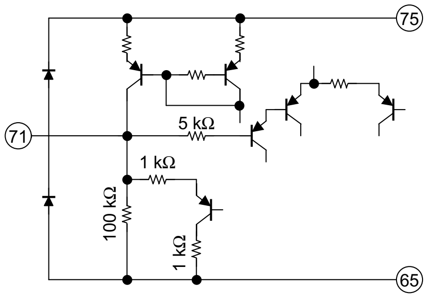
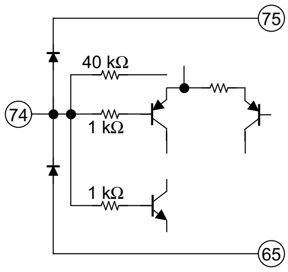
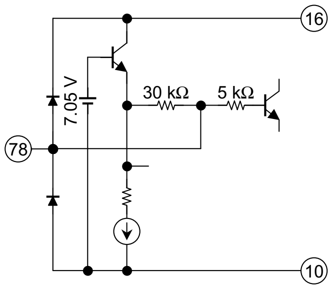
Pin No.	Pin Name	Function	Interface Circuit	Input Signal/Output Signal
28	SDA	SDA pin for I^2C BUS		—
29	NC	This pin is not used. Connect to GND.	—	—
30	SCL	SCL pin for I^2C BUS		—
31	I^2L V_{DD}	V_{DD} pin for I^2L block. Connects 2 V (typ.). Supply power via zener diode through resistor from pin 45. (See “Application Circuit”)	—	—
32 33	NC	This pin is not used. Connect to GND.	—	—
34	DAC1 (SYNC OUT)	Outputs 1-bit DAC or separated SYNC. Open-collector output.		DC or SYNC OUT 
35	VP OUT	Outputs vertical pulse. Applying current to this pin, performs external blanking by OR-ing with internal blanking. Note: Changing H-position varies VP output width. Use the start phase only for VP output.		VP output:  V-BLK input current: 780 µA to 1 mA
36	NC	This pin is not used. Connect to GND.	—	—

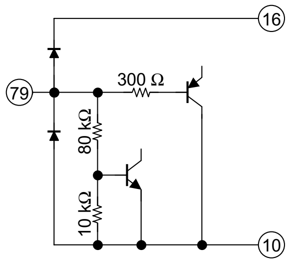
Pin No.	Pin Name	Function	Interface Circuit	Input Signal/Output Signal
37	H-OUT	Horizontal output pin. Open-collector output.		
38	DEF/DAC GND	GND pin for DEF/DAC block	—	—
39	FBP IN	Inputs FBP for horizontal AFC. Sets H-BLK width.		
40	H CURVE CORRECTION	Adjusts screen curve at high voltage fluctuation. Input AC component of high voltage fluctuation. When not used, connect 0.01-μF capacitor between this pin and GND.		DC
41	H-FREQ SW2	Switches horizontal frequency (Switch 2). Leave this pin open when horizontal frequency is switched by Bus controlling. Controlling this pin prevails over Bus control. (Refer to Table 1: Bus control function.) When this IC is used for CRT, frequency of horizontal output (pin 37) is controlled according to voltage of this pin. DC voltage that is generated by dividing resistor of DEF V_{CC} (pin 45) should be used to control this pin.		At BUS control (horizontal frequency) : output voltage value 28 k/15 kHz : DC 9 V 31 kHz : DC 6 V 33 kHz : DC 3 V 37 k/45 kHz : DC 0 V At pin 22 control, horizontal frequency and input voltage value 0 to 1.0 V : 37 k/45 kHz 2.0 V to 4.0 V : 33 kHz 5.0 V to 7.0 V : 31 kHz 8.0 V to 9.0 V : 28 k/15 kHz
42	HVCO	Connects ceramic oscillator for horizontal oscillation. Use Murata "CSBLA503KECZF30".		—
43	NC	This pin is not used. Connect to GND.	—	—

Pin No.	Pin Name	Function	Interface Circuit	Input Signal/Output Signal
44	AFC FILTER	Connects filter for detecting AFC.		DC
45	DEF/DAC V_{CC}	V_{CC} pin for DEF/DAC block. See “Maximum Ratings” about the supply voltage.	—	—
46	NC	This pin is not used. Connect to GND.	—	—
47	CP OUT	Outputs internal clamp pulse (CP).		
48	NC	This pin is not used. Connect to GND.	—	—
49	SCP IN	Inputs SCP from up converter. Input signals are clamp pulse (CP) and black peak detection stop pulse (BPP).		2.2 V to 2.8 V : BPP 4.2 V to 9 V : CP
50	HD IN	Inputs horizontal sync HD signal. Inputs positive- or negative-polarity signals.		 or 
51	NC	This pin is not used. Connect to GND.	—	—
52	VD IN	Inputs vertical sync VD signal. Inputs positive- or negative-polarity signals.		 or 

Pin No.	Pin Name	Function	Interface Circuit	Input Signal/Output Signal
53	SYNC IN	Inputs Y signal with sync signal via clamp capacitor.		White 100%: 1 V_{p-p}  or 
54	NC	This pin is not used. Connect to GND.	—	—
55	H-FREQ SW1	Switches horizontal frequency (Switch 1). Leave this pin open when horizontal frequency is switched by Bus controlling. Controlling this pin prevails over Bus control. (Refer to Table 1: Bus control function.) When this IC is used for CRT, connect this pin to DEF V_{CC} (pin 45) or DEF GND (pin 38). If it is not necessary to control this pin on CRT, connect this pin directly to DEF VCC or DEF GND on the PCB.		DEF V_{CC} or DEF GND
56	NC	This pin is not used. Connect to GND.	—	—
57	VSM FILTER	Connects VSM output filter. Please connect 0.01-µF capacitor between this pin and GND.		DC
58	COLOR LIMITER	Connects filter for detecting color limit.		DC
59	NC	This pin is not used. Connect to GND.	—	—

Pin No.	Pin Name	Function	Interface Circuit	Input Signal/Output Signal
60	C_{r2}/P_{r2} IN	Inputs C_{r2}/P_{r2} signal via clamp capacitor.		700 mVp-p700 mVp-p at 100% color bar for C_{r1}/P_{r1}
61	C_{b2}/P_{b2} IN	Inputs C_{b2}/P_{b2} signal via clamp capacitor.		700 mVp-p at 100% color bar for C_{b1}/P_{b1}
63	Y2 IN	Inputs Y2 signal via clamp capacitor.		1 Vp-p (including sync) at 100% color bar  or 
62	NC	This pin is not used. Connect to GND.	—	—
64	LIGHT AREA DET FILTER	Connects filter for detecting light area. Voltage of this pin controls dynamic γ circuit gain for light area.		DC
65	Y/C GND	GND pin for Y/C block	—	—
66	C_{r1}/P_{r1} IN	Inputs C_{r1}/P_{r1} signal via clamp capacitor.		700 mVp-p700 mVp-p at 100% color bar for C_{r1}/P_{r1}
67	C_{b1}/P_{b1} IN	Inputs C_{b1}/P_{b1} signal via clamp capacitor.		700 mVp-p at 100% color bar for C_{b1}/P_{b1}
68	Y1 IN	Inputs Y1 signal via clamp capacitor.		1 Vp-p (including sync) at 100% color bar  or 
69	NC	This pin is not used. Connect to GND.	—	—

Pin No.	Pin Name	Function	Interface Circuit	Input Signal/Output Signal
70	BPH FILTER	Connects filter for detecting black peak. Voltage of this pin controls black stretch gain. Leaving Y open and setting the test circuit SW 2 = C enable to monitor H/V-BPP (black-stretch-stop pulse) width.		DC
71	DARK AREA DET FILTER	Connects filter for detecting dark area. Voltage of this pin controls dynamic γ circuit gain for dark area.		DC
72 73	NC	This pin is not used. Connect to GND.	—	—
74	APL FILTER	Connects filter for correcting DC restoration rate. Leaving this pin open enables to monitor Y signal after black stretch and dynamic γ.		—
75	Y/C V_{CC}	V_{CC} pin for Y/C block. See "Maximum Ratings" about the supply voltage.	—	—
76	NC	This pin is not used. Connect to GND.	—	—
77	VSM OUT	Outputs Y signal for VSM that passed through HPF circuit (first differential circuit). Output signals are muted according to pins 1, 2, and 80.	See pin 57.	—
78	ABCL IN	Inputs ABL and ACL signals. Sets gain and start point of ABL and dynamic ABL signal according to bus controlling.		DC

Pin No.	Pin Name	Function	Interface Circuit	Input Signal/Output Signal
79	Y_M/P-MUTE/BLK	High-speed halftone switch for internal RGB signal. Enables picture mute and blanking.		0 to 0.5 V : Internal 1.2 V to 1.8 V : Half Tone 2.7 V to 4.0 V : P-Mute 7 V to 9 V : Blanking

Bus Control Map

Write Data

Slave Address: 88H

Sub-Add	D7	D6	D5	D4	D3	D2	D1	D0	Preset
00	H-FREQ1		H-DUTY	YUV-SW	DAC1	DAC2	SYNC-SW	H-FREQ2	1000 0000
01	HORIZONTAL POSITION							CLP-PHS	1000 0000
02	ACB-MODE		SCP-SW	HBP-PHS1	SYNC SEP-LEVEL		TEST		1000 0000
03	V-BLK PHASE					VERTICAL FREQUENCY			1000 0000
04	COMPRESSION-BLK PHASE-1				COMPRESSION-BLK PHASE-2				1000 0000
05	P-MODE1	UNI-COLOR							1000 0000
06	BRIGHTNESS								1000 0000
07	OSD-ACL	COLOR							1000 0000
08	TINT							HBP-PHS2	1000 0000
09	PICTURE SHARPNESS							BLS γ	1000 0000
0A	RGB BRIGHTNESS							DCRR-SW	1000 0000
0B	HI BRT	RGB CONTRAST							1000 0000
0C	SUB CONTRAST					WPS	YUV MODE	Y-OUT γ	1000 0000
0D	DRIVE GAIN1							DR-R	1000 0000
0E	DRIVE GAIN2							DR-B/G	1000 0000
0F	R CUT OFF								1000 0000
10	G CUT OFF								1000 0000
11	B CUT OFF								1000 0000
12	R-Y/B-Y GAIN				R-Y/B-Y PHASE				1000 0000
13	G-Y/B-Y GAIN				G-Y/B-Y PHASE				1000 0000
14	COLOR SRT TRAN		C FREQ	GREEN STRETCH		COLOR γ		CLT	1000 0000
15	C.D.E.		Y/C GAIN COMP		BL STRETCH GAIN		FLESH	H-SHIFT	1000 0000
16	VSM PHASE			VSM GAIN			APACON PEAK FREQ		1000 0000
17	DC REST POINT			DC REST RATE			DC REST LIMIT		1000 0000
18	BLACK STRETCH POINT			APL VS BSP		B.L.C.	B.D.L	BS-AREA	1000 0000
19	SRT-GAIN					WPL-LEVEL			1000 0000
1A	D-ABL POINT		D-ABL GAIN		BL STRETCH POINT		P-MODE2		1000 0000
1B	ABL POINT			ABL GAIN			RGB OUT MODE		1000 0000
1C	DYNC γ GAIN		BS-CHAR1	STATIC γ GAIN-1			STATIC γ GAIN-2		1000 0000
1D	OSD BRIGHT		OSD CONTRAST		Y/C-DL1	DYNC γ AREA			1000 0000
1E	Y DETAIL CONTROL				BS-CHAR2	WP BLUE POINT			1000 0000
1F	Y GROUP DELAY CORRECTION				Y/C-DL2	WP BLUE GAIN			1000 0000

Read Data

Slave Address: 89H

	D7	D6	D5	D4	D3	D2	D1	D0
0	POR	IK-IN	RGB-OUT	YUV-IN	H-OUT	VP-OUT	RGB-IN	SYNC-IN

Bus Control Features

Write Mode

Resister Name	Description	Preset Value
H-FREQ1/2	Switches horizontal oscillation frequency. (See the appendix 1)	33.75 kHz
H-DUTY	Switches horizontal output duty. 0: 41% 1: 47%	41%
YUV-SW	Switches YUV input. 0: INPUT-1 (Y1/C_{b1}/C_{r1}) 1: INPUT-2 (Y2/C_{b2}/C_{r2})	INPUT-1
DAC 1	Switches DAC controlling output. 0: OPEN (high) 1: ON (low) Controls 1-bit DAC of open-collector when TEST is 00. Outputs H/C-SYNC from pin 34 when TEST is 01.	OPEN
DAC 2	Switches DAC controlling output. 0: ON (low), 1: OPEN (high) Controls 1-bit DAC of open-collector when TEST is 00. Outputs ACB reference pulse from pin 23 when TEST is 01.	ON
SYNC-SW	Switches sync input. 0: Selects HD/VD input. 1: Selects SYNC input.	HD/VD
HORIZONTAL POSITION	Adjusts horizontal picture position (phase). 0000000: −12.5% 1111111: +12.5% Note: VP output width (pin 35) varies with a change of horizontal position.	CENTER
CLP-PHS	Switches clamp pulse phase. 0: 0.7-µs (2.5%) width, 1.1-µs (3.8%) delay from HD stop phase. 1: 0.7-µs (2.4%) width, 0.2-µs (0.7%) delay from HD stop phase when no signal, 0.8-µs (2.7%) width that is 1.2-µs (4.2%) delay from FBP start phase. Also switches CP phase of CP-OUT (pin 47).	1.1-µs delay
ACB MODE	Sets ACB mode; Sets converged reference level. 00: ACB OFF (cutoff BUS control), 01: ACB ON (5 IRE), 10: ACB ON (10 IRE) 11: ACB ON (20 IRE)	ACB ON (10 IRE)
SCP-SW	SCP (sand castle pulse) Switches modes. 0: Internal Mode 1: External input Mode	Internal Mode
HBP-PHS1/2	Switches phase of black-stretch-detection stop pulse. HBP-PHS1 = 0 and HBP-PHS2 = 0: FBP ± 3% HBP-PHS1 = 0 and HBP-PHS2 = 1: FBP ± 8% HBP-PHS1 = 1 and HBP-PHS2 = 0: FBP ± 13% HBP-PHS1 = 1 and HBP-PHS2 = 1: FBP ± 18% Leaving Y open and setting the test circuit SW2 to C enable to monitor H/V-BPP (black-stretch-detection stop pulse) width through pin 70.	±3%
SYNC SEP-LEVEL	Switches Sync SEP-level. 00: 16% 01: 24% 10: 32% 11: 40% (At 1125I/60)	16%
TEST	Test Mode: Controls 1-bit DAC of open-collector when TEST is 00. Outputs H/C-SYNC from pin 34, and ACB reference pulse from pin 23 when TEST is 01. Do not set TEST to 10/11 for that is shipment TEST Mode.	00

Resister Name	Description	Preset Value
V-BLK PHASE	Switches vertical BLK stop phase. 00000: 16 H~ 11110: 46 H (1 H/STEP) 11111: Internal H/V-BLK OFF Please set ACB Mode to OFF when internal H/V-BLK is OFF (11111).	32 H
V-FREQUENCY	Vertical free-run frequency: Sets V pull-in range. (See Appendix 2.)	1281 H
COMPRESSION-BLK PHASE-1/2	Compression BLK phase: Sets BLK for upper and lower parts of screen. (See Appendix 3.)	CENTER, OFF
P-MODE1/2	Picture Mode: Sets picture mute, halftone, blue background, and Y mute. (See Appendix 4.)	P-MUTE 1
UNI-COLOR	Unicolor adjustment: 0000000: −16dB~ 1111111: 0dB	min
BRIGHTNESS	Brightness adjustment: 00000000: −40 IRE 11111111: +40 IRE	CENTER
OSD-ACL	OSD-ACL; 0: OFF 1: ON	ON
COLOR	Color adjustment: 0000000: COLOR MUTE, 0000001: −20dB or more 1111111: +4dB	C-MUTE
TINT	Tint adjustment: 0000000: −32 deg~ 1111111: +32 deg	±0 deg
PICTURE-SHARPNESS	Sharpness adjustment: 0000000: −10dB or more 1000000: +10dB 1111111: +17.5dB (at peak FREQ)	CENTER
BLSγ	Blue stretch γ correction: B-axis correction 0: OFF 1: ON	OFF
RGB-BRIGHTNESS	RGB brightness: 0000000; −20 IRE~ 1111111; +20 IRE	CENTER
DCRR-SW	Switches DC restoration rate. 0: 100% or higher 1: 100%or lower	100% or higher
HI BRT	High-bright color: 0: OFF 1: ON	ON
RGB-CONTRAST	RGB contrast: 0000000: −16.5dB 1111111: 0dB	min
SUB-CONTRAST	Sub-contrast: 00000: −3.3dB 11111: +2.5dB	CENTER
WPS	WPS level: 0: 110 IRE 1: 130 IRE	110 IRE
YUV MODE	Y/color-difference input Mode: 0: Y/Cb/Cr, 1: Y/Pb/Pr (Remarks) Y/Cb/Cr: ITU-R BT 601 Y/Pb/Pr: ITU-R BT 709 (1125/60/2:1)	Y/Cb/Cr
Y-outγ	**Y** -out gamma control: 0: OFF 1: ON	OFF
DRIVE GAIN1/2	Drive gain 1/2; 0000000: −5dB 1111111: +3dB	CENTER
DR-R DR-B/G	Switches RGB drive gain base. (See Appendix 5.)	R

Resister Name	Description	Preset Value
R/G/B CUT OFF	R/G/B cutoff: 1) At ACB-OFF RGB-OUT 00000000: 1.9 V 11111111: 2.9 V 2) At ACB-ON SENS-IN 00000000: 0.5 Vp-p 11111111: 1.5 Vp-p	CENTER
R-Y/B-Y GAIN	Switches R-Y/B-Y relative amplitude: 0000: min (0.45) 1111: max (0.9)	CENTER
R-Y/B-Y PHASE	Switches R-Y/B-Y relative phase: 0000: min (90 deg) 1111: max (111.5 deg)	min
G-Y/B-Y GAIN	Switches G-Y/B-Y relative amplitude: 0000: min (0.25) 1111: max (0.48)	CENTER
G-Y/B-Y PHASE	Switches G-Y/B-Y relative phase: 0000: min (232 deg) 1111: max (254 deg)	min
COLOR SRT TRAN	Color SRT transient: Color-difference transient improvement 00: C-SRT OFF~ 11: max	CENTER
C FREQ	Color SRT peak frequency: 0: 4.5 MHz 1: 5.8 MHz	4.5 MHz
GREEN STRETCH	Green stretch: 00: OFF~ 11: max (+3dB)	OFF
COLOR γ	Color γ correction point 00: OFF, 01: 0.23 Vp-p, 10: 0.40 Vp-p, 11: 0.58 Vp-p	OFF
CLT	Color limiter level: 0: 1.65 Vp-p, 1: 2 Vp-p	1.65 Vp-p
CDE	Color detail enhancer: 00: min 11: max	CENTER
Y/C GAIN COMP	Dynamic Y/C compensation: Operated when luminance level is made up according to dynamic Yγ. 00: OFF~ 11: max	OFF
BL STRETCH GAIN	Blue stretch gain: B-axis correction 00: OFF 11: max (+6.4dB)	OFF
FLESH	Flesh color: Skin tone color correction 0: OFF 1: ON (Lead-in angle: ±33.7 deg)	OFF
H-SHIFT	Shifts a center of horizontal picture position (phase): 0: OFF 1: ON（FBP shifts 6.7% against HD）	OFF
VSM-PHASE	VSM phase: 000: −37.5 ns 101: normal 111: +15 ns	CENTER
VSM GAIN	VSM gain: 000: OFF 001: 0 dB~ 111: +16dB (VSM gain is limitted 1.4 Vp-p)	OFF
APACON PEAK f_0	APACON peak frequency: 00: 13.5 MHz 01: 9.5 MHz 10: 7.2 MHz 11: 4.5 MHz	13.5 MHz
DC REST POINT	DC restoration rate correction point: 000: 0% 111: 49%	CENTER
DC REST RATE	DC restoration correction rate: 000: 100% 111: 135% (70%)	min
DC REST LIMIT	DC restoration rate correction limit point: 00: 67% 01: 77% 10: 80% 11: 80%	min

Resister Name	Description	Preset Value
BLACK STRETCH POINT	Black stretch start point 1: 000: OFF 001: 25 IRE~ 111: 55 IRE	CENTER
APL VS BSP	Black stretch start point 2: 00: 0 IRE 11: 46 IRE up (at APL 100%)	0 IRE
B.L.C	Black level automatic correction: Up to 6.5 IRE. (Black stretch takes priority.) 0: OFF 1: ON	OFF
B.D.L.	Switches black detection level: 0: 3 IRE 1: 0 IRE	3 IRE
BS-AREA	Black stretch area reinforcement: 0: ON 1: OFF	ON
SRT-GAIN	SRT gain; Y transient improvement (LTI) 00000: min 11111: max	CENTER
WPL-LEVEL	White letters improvement amplitude; 000: min (21 IRE) ~ 110: max (102 IRE) 111: OFF	min
D-ABL POINT	Dynamic ABL detection voltage 00: min 11: max	CENTER
D-ABL GAIN	Dynamic ABL sensitivity 00: min 11: max	min
BL STRETCH POINT	Blue stretch point; B-axis correction 00: min (28 IRE) 11: max (60 IRE)	min
ABL POINT	ABL detection voltage 000: min 111: max	CENTER
ABL GAIN	ABL sensitivity 000: min 111: max	min
RGB-OUT MODE	RGB output mode; RGB output mode SW for test and adjustment 00: Normal 01: R only 10: G only 11: B only	Normal
DYNCγ GAIN	Dynamic Yγ gain vs dark area; dynamic γ-correction according to dark area. 00:min~ 11: max (Maximum gain is +6dB included Static Yγ gain for dark area.)	CENTER
BS-CHAR1/2	Black stretch characteristic swich BS-CHAR1 = 0 and BS-CHAR2 = 0: OFF BS-CHAR1 = 0 and BS-CHAR2 = 1: min BS-CHAR1 = 1 and BS-CHAR2 = 0: mid BS-CHAR1 = 1 and BS-CHAR2 = 1: max	OFF
STATICγ GAIN-1	Static Yγ dark area gain; γ correction for dark area 000: OFF 001: min (–5dB) ~ 11: max (+2.4dB) Note: When STATIC γ GAIN-1 is 000(OFF), set DYNC γ GAIN to min (00), STATIC γ GAIN-2 to OFF (11), and DYNC γ AREA to min (000).	OFF
STATICγ GAIN-2	Static Yγ light area gain; γ correction for light area 00: max (–8.8dB)~ 11: OFF When 00~10 is set, light area static Yγ and light dynamic Yγ according to light area is operated.	max
OSD BRIGHT	OSD brightness: 00: 5 IRE 01: 0 IRE 10: –5 IRE 11: –10 IRE	–5 IRE
OSD-CONTRAST	OSD contrast: 00: min (–9.5dB) 11: max (0dB)	min

Resister Name	Description	Preset Value
Y/C DL1/2	Adjusts Y/C phase; adjusts the phase Y before passing through matrix circuit. Y/C DL2 = 0 and Y/C DL1 = 0: −10 ns, Y/C DL2 = 0 and Y/C DL1 = 1: −5 ns Y/C DL2 = 1 and Y/C DL1 = 0: 0 ns, Y/C DL2 = 1 and Y/C DL1 = 1: +5 ns	−10 ns
DYNCγAREA	Dynamic γ dark area detection sensitivity; switches detection sensitivity of dynamic Yγ of dark area. 000: min~ 111: max	min
Y DETAIL CONTROL	Controls Y detail; corrects sharpness of 5.0-MHz peak frequency. 0000:min (trap) 1111: max (+6dB)	CENTER
WP BLUE POINT	White peak blue point; 000: OFF 001: min (42 IRE) ~ 111: max (106 IRE)	OFF
Y-GROUP DELAY CORRECTION	Y group delay correction; shoot balance correction. 0000: Pre-shoot gain is lowered. (Overshoot gain is raised.) 1111: Overshoot gain is lowered. (Pre-shoot gain is raised.)	CENTER
WP BLUE GAIN	White peak blue gain. 000: min (+3dB) 111: max (+10dB)	min

Appendix 1: Horizontal Frequency

Pin Voltages (V)		Bus Data			H-Frequency (kHz)
Pin 55	Pin 41	00-D0	00-D7	00-D6	
DEF GND (0~1.0)	DEF V_{CC} (8.0~9.0)	0	0	0	28.125
	6.0 (5.0~7.0)	0	0	1	31.5
	3.0 (2.0~4.0)	0	1	0	33.75
	DEF GND (0~1.0)	0	1	1	37.9
DEF V_{CC} (8.0~9.0)	DEF V_{CC} (8.0~9.0)	1	0	0	15.75
	6.0 (5.0~7.0)	1	0	1	31.5
	3.0 (2.0~4.0)	1	1	0	33.75
	DEF GND (0~1.0)	1	1	1	45

Note 1: Controlling pins prevails over BUS control. When the TA1360F is used for CRT, control horizontal oscillation frequency by pins 41 and 55. (See the pin descriptions for details.)

Note 2: Horizontal output frequency may not be switched at once but may takes two steps if switching pins 41 and 55 is controlled at the same time. Switching horizontal output frequency may cause deterioration of the horizontal transistor. Thus, be sure to take account of applications, included software.

Appendix 2; Vertical Frequency

Data	V Pull-in Range	V-BPP		Example of Format/V (H)-Frequency
		Start Phase	Stop Phase	
000	48~1281 H	1100 H	V-BLK P. (C.BLK P.) +20 H	1125P/30 Hz (33.75 kHz)
001	48~849 H	730 H		750P/60 Hz (45 kHz) (750P/50Hz(37.5 kHz))
010	48~725 H	600 H		625P/50 Hz (31.5 kHz) SVGA/60 Hz(37.9 kHz)
011	48~660 H	545 H		1125I/50 Hz (28.125 kHz) 1125I/60 Hz (33.75 kHz)
100	48~613 H	500 H		525P/60 Hz (31.5 kHz)
101	48~363 H	290 H		PAL/SECAM/50 Hz (15.625 kHz), 100 Hz (31.5 kHz)
110	48~307 H	240 H		NTSC/60 Hz (15.734 kHz), 120 Hz (31.5 kHz)
111	VP-OUT HI	—	—	—

Appendix 3; Compression-BLK Phase

V-Frequency	Phase-1 (start phase) *	Phase-2 (stop phase)
000	1088 H~1116 H	50~78 H (0000: C-BLK2 OFF)
001	720 H~748 H	
010	592 H~620 H	
011	528 H~556 H	
100	488 H~516 H	
101	280 H~308 H	
110	224 H~252 H	
111	C-BLK OFF	

*: C-BLK1 = 1111: C-BLK1 OFF

Appendix 4; P-Mode

05-D7	1A-D1	1A-D0	MODE	Description
0	0	0	NORMAL 1	P-Mute and halftone the main signal by pin Y_M. Insert analog RGB-IN by Ys3, and OSD-IN by Ys1/Ys2. Analog RGB-IN > P-Mute
0	0	1	Y-MUTE	Full-screen-mute process is executed on Y of main signal by BUS. Insert analog RGB-IN by Ys3, and OSD-IN by Ys1/Ys2. Analog RGB-IN > P-Mute
0	1	0	Y_M 1	Full-screen-halftone process is executed on main signal by BUS. Insert P-Mute by pin Y_M, and analog RGB-IN by Ys3. Ys1/Ys2 blends OSD-IN and main halftone signal. Analog RGB-IN > P-Mute
0	1	1	BB	Blue background process is executed on main signal by BUS. Insert P-Mute by pin Y_M, analog RGB-IN by Ys3, and OSD-IN by Ys1/Ys2 Analog RGB-IN > P-Mute
1	0	0	P-MUTE 1	Full-screen-mute process is executed on main signal by BUS. Insert analog RGB-IN by Ys3, and OSD-IN by Ys1/Ys2. Analog RGB-IN > P-Mute
1	0	1	Y_M 2	Full-screen-halftone process is executed on main signal by BUS. Insert P-Mute by pin Y_M, and analog RGB-IN by Ys3. Ys1/Ys2 blends OSD-IN and main halftone signal P-Mute > Analog RGB-IN
1	1	0	P-MUTE 2	Full-screen-mute process is executed on main signal and analog RGB-IN by BUS. Insert OSD-IN by Ys1/Ys2. P-Mute > Analog RGB-IN
1	1	1	NORMAL 2	P-Mute and halftone process is executed on the main signal by pin Y_M. Analog RGB-IN is inserted by Ys3, and OSD-IN by Ys1/Ys2. P-Mute > Analog RGB-IN

Output priority; (000)~(100): Main signal < BB < P-MUTE < RGB-IN < OSD-IN
(101)~(111): Main signal < BB < RGB-IN < P-MUTE < OSD-IN

Appendix 5; DR-R, DR-B/G

DR-R	DR-B/G	Reference Axis	Drive Gain1	Drive Gain2
0	0	R	G	B
0	1	R	G	B
1	0	G	R	B
1	1	B	G	R

Read Function

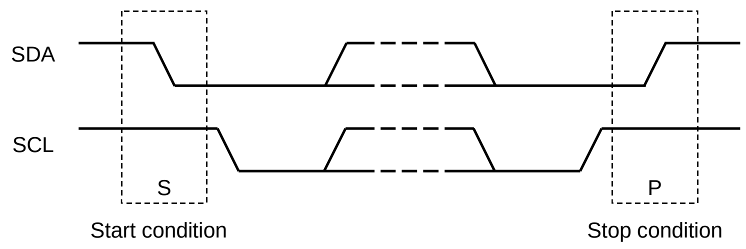
Signal	Function
POR	Power-on reset: 0: RESISTER PRESET 1: Normal After power on, 0 is returned at first read; 1, at second and subsequent reads.
IK-IN	Detects IK input; detects input through pin 8. 0: NG (no signal) 1: OK (signal detected)
RGB-OUT	Detects RGB-OUT self-check; detects output of pins 12, 13, 14. 0: NG (no signal) 1: OK (signal detected) Detects signal when all three outputs hsve signals. Small signals are not detected.
YUV-IN	Detects YUV-IN self-check; detects input of pins 60, 61 63 or pins 66, 67, 68. 0: NG (no signal) 1: OK (signal detected) Detects signal when all three inputs are AC signals. Small signals or signals like DC voltage are not detected.
H-OUT	Detects H-OUT self-check; detects output of pin 37. 0: NG (no signal) 1: OK (signal detected)
VP-OUT	Detects VP-OUT self-check; detects output of pin 35. 0: NG (no signal) 1: OK (signal detected)
RGB-IN	Detects RGB-IN self-check; detects input of pins 24, 25, 26. 0: NG (no signal) 1: OK (signal detected) Detects signal when all three inputs are AC signals. Small signals or signals like DC voltage are not detected.
SYNC-IN	Detects SYNC-IN self-check; detects input of pin 53. 0: NG (no signal), 1: OK (signal detected)

How to Transmit/Receive Via I²C Bus

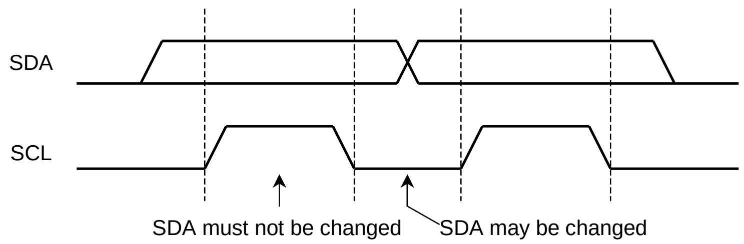
Slave Address: 88H

A6	A5	A4	A3	A2	A1	A0	W/R
1	0	0	0	1	0	0	0/1

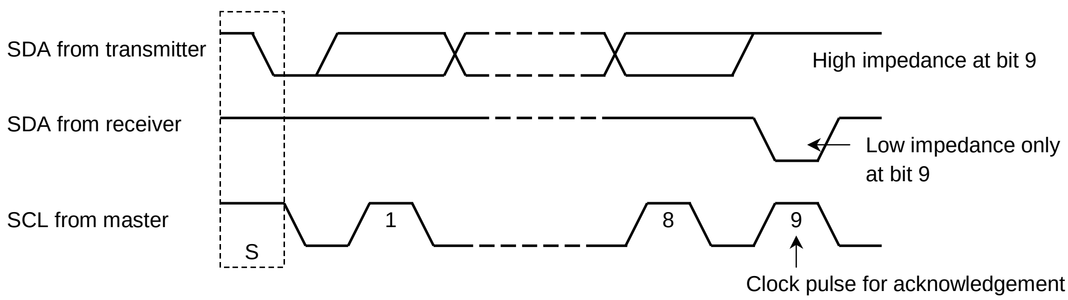
Start and Stop Conditions



Bit Transfer



Acknowledgement



Data Transmit Format 1

S	Slave address	0	A	Sub address	A	Transmit data	A	P

7 bit　8 bit　9 bit

MSB　MSB　MSB

S: Start condition　A: Acknowledgement　P: Stop condition

Data Transmit Format 2

S	Slave address	0	A	Sub address	A	Transmit data 1	A	······

······	Sub address	A	Transmit data n	A	P

Data Receive Format

S	Slave address	1	A	Transmit data 1	A	Receive data 2	A	P

7 bit　8 bit

MSB　MSB

To receive data, the master transmitter changes to the receiver immediately after the first acknowledgement. The slave receiver changes to the transmitter.

The stop condition is always created by the master.

Details are provided in the Philips I^2C specifications.

Optional Data Transmit Format

S	Slave address	0	A	1	Sub address	A	Transmit data 1	····	Transmit data n	A	P

7 bit　7 bit　8 bit　8 bit

MSB　MSB　MSB　MSB

In this way, sub addresses are automatically incremented from the specified sub address and data are set.

Purchase of TOSHIBA I^2C components conveys a license under the Philips I^2C Patent Rights to use these components in an I^2C system, provided that the system conforms to the I^2C Standard Specification as defined by Philips.

Maximum Ratings (Ta = 25°C)

Characteristics	Symbol	Rating		Unit
Supply voltage	V_{CCmax}	12		V
Input pin signal voltage	e_{inmax}	9		Vp-p
Power dissipation	P_D (Note 3)	2604		mW
Power dissipation reduction rate depending on temperature	1/θja	20.8		mW/°C
Operating temperature	T_{opr}	−20 to 65	−20 to 70	°C
Storage temperature	T_{stg}	−55 to 150		°C
Supply voltage (pins 16, 45 and 75)	min	8.7	8.5	V
	typ.	9.0	8.8	
	max	9.3	9.1	

Note 3: See the following Figure A. (With device mounted on a PCB whose dimensions are 114.3 mm × 76.2 mm × 1.6 mm and whose surface is 20% copper. Mount the device on a PCB of at least these dimensions and whose surface is at least 20% copper.)
When using in –25 to 70°C of operating temperature, set the IC's power supply voltage (pins 16, 45, 75) to 8.8 V (±0.3 V).
When designing a set, make sure that the IC can radiate heat because the TA1360AFG has low thermal capacity. Note that the power dissipation varies greatly according to conditions of a board.

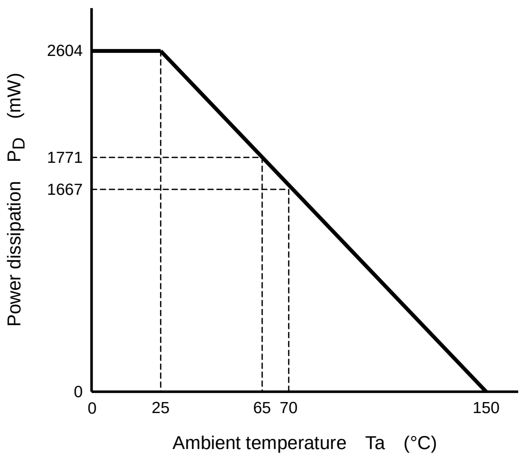


Figure A Power Dissipation Reduction Curve

Note 4: Power supply sequence

At power-on, power should be supplied to the power supply pins according to the following sequence:

1. Pin 31 (I^2L VDD)
2. Pin 45 (DEF/DAC V_{CC})
3. Pins 16 and 75 (YC V_{CC}/RGB V_{CC})

Supply power to pin 37 via zener diode through resistor from pin 45. (See “Application Circuit”.)
BUS preset value is become undefined and caused malfunction of the IC unless supplying power to all supply pins or follow the power supply sequence described above. When the frequency of horizontal output (pin 37) became undefined, horizontal transistor may be damaged. When the TA1360F is used for CRT, control horizontal oscillation frequency by pins 41 and 55.

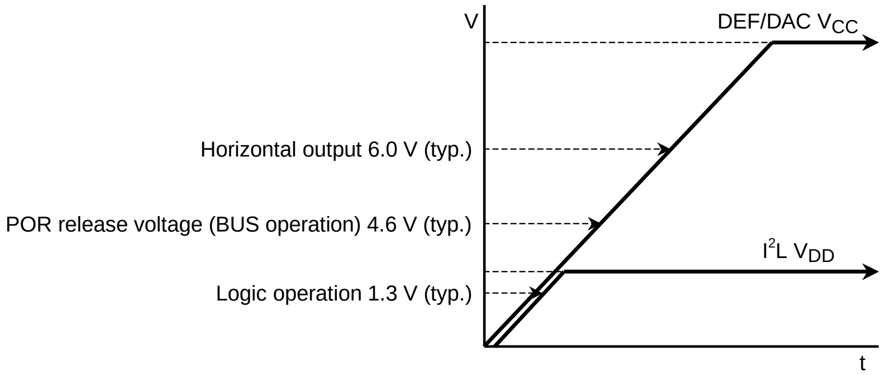


Figure B Timing chart that indicates the timing from power-on till horizontal output. (At Ta = 25 C°)

Operating Conditions

Characteristics	Description		Min	Typ.	Max	Unit
Supply voltage (V_{CC})	Pin 16, 45, 75	T_{opr} = −20 to 65°C (Note 5)	8.7	9.0	9.3	V
		T_{opr} = −20 to 70°C (Note 5)	8.5	8.8	9.1	
	Pin 31		1.8	2.0	2.2	
Y input level	Pins 63, 68: 100% color bar, including sync (Picture period amplitude, 0.7 Vp-p)		—	1.0	—	Vp-p
Color-difference input level	Pins 60, 61 66, 67: 100% color bar, not including sync		—	0.7	—	
HD/VD input level	Pins 50, 52		2.0	5.0	V_{CC}	V
SYNC input level	Pin 53: 100% color bar, including sync		0.9	1.0	1.1	Vp-p
SCP input level	Pin 49	CP	4.2	5.0	V_{CC}	V
		BPP	2.2	2.5	2.8	
Horizontal frequency switching voltage	Pin 55	At 28 k/31 k/33 k/37 kHz	0	0	1.0	
		At 15 k/31 k/33 k/45 kHz	8.0	V_{CC}	V_{CC}	
	Pin 41	28.125 kHz or 15.75 kHz	8.0	V_{CC}	V_{CC}	
		31.5 kHz	5.0	6.0	7.0	
		33.75 kHz	2.0	3.0	4.0	
		37.9 kHz or 45 kHz	0	0	1.0	
FBP input level	Pin 39	H-AFC	6.5	7.0	V_{CC}	
		H-BLK	3.0	3.5	4.0	
FBP input width	Pin 39		0.16	—	0.3	H
H-OUT input current	Pin 37		—	9.0	15.0	mA
DAC input current	Pins 23, 34		—	0.3	1.0	
SCL/SDA pull-up voltage	Pins 28, 30		3.3	5.0	V_{CC}	V
SDA input current	Pin 28		—	—	2	mA
Analog RGB input level	Pins 24, 25, 26: White 100%		—	0.7	—	Vp-p
Analog OSD input level	Pins 18, 19, 21: White 100%		—	0.7	—	
Y_S3 switching voltage	Pin 2		1.5	5.0	V_{CC}	V
Y_S1/2 switching voltage	Pins 1, 80	OSD	2.9	5.0	V_{CC}	
		VSM MUTE	1.1	1.5	1.7	
Y_M switching voltage	Pin 79	BLK	7.0	V_{CC}	V_{CC}	
		P-MUTE	2.7	3.5	4.0	
		HALF TONE	1.2	1.5	1.8	
External V-BLK input current	Pin 35		0.78	—	1	mA

Note 5: See “Maximum Ratings” about T_{opr}.

Electrical Characteristics (unless otherwise specified, V_{CC} = 9 V/2 V, Ta = 25°C)

Current Dissipation

Pin Name	Symbol	Test Circuit	Min	Typ.	Max	Unit
DEF/DAC V_{CC} (9 V)	I_{CC1}	—	19.2	24.0	28.2	mA
RGB V_{CC} (9 V)	I_{CC2}	—	48.8	61.0	67.8	
I^2L V_{DD} (2 V)	I_{CC3}	—	21.3	25.0	29.4	
Y/C V_{CC} (9 V)	I_{CC4}	—	36.8	46.0	51.1	

Pin Voltage

Test Condition

(1) BUS = Preset
(2) SW71 = B, SW70 = B, SW68 = C, SW67 = B, SW66 = B, SW64 = B, SW63 = B, SW60 to 61 = B, SW53 = B, SW44 = ON, SW40 = B, SW39 = A, SW37 = A, SW24 to 26 = A, SW21 = A, SW18~19 = A, SW77 = OFF, SW74 = ON

Pin No.	Pin Name	Symbol	Test Circuit	Min	Typ.	Max	Unit
1	Y_S2	V_1	—	—	0.1	0.2	V
2	Y_S3	V_2	—	—	0.1	0.2	
4	R S/H	V_4	—	4.2	5.2	6.2	
6	G S/H	V_6	—	4.2	5.2	6.2	
7	B S/H	V_7	—	4.2	5.2	6.2	
18	ANALOG OSD R IN	V_{18}	—	3.65	3.95	4.25	
19	ANALOG OSD G IN	V_{19}	—	3.65	3.95	4.25	
21	ANALOG OSD B IN	V_{21}	—	3.65	3.95	4.25	
24	ANALOG R IN	V_{24}	—	3.65	3.95	4.25	
25	ANALOG G IN	V_{25}	—	3.65	3.95	4.25	
26	ANALOG B IN	V_{26}	—	3.65	3.95	4.25	
40	H CURVE CORRECTION	V_{40}	—	2.2	2.5	2.8	
42	HVCO	V_{42}	—	4.4	5.0	5.6	
44	AFC FILTER	V_{44}	—	5.4	6.2	7.0	
49	CP IN	V_{49}	—	—	0	0.3	
50	HD IN	V_{50}	—	—	0	0.3	
52	VD IN	V_{52}	—	—	0	0.3	
53	SYNC IN	V_{53}	—	1.8	2.1	2.4	
57	VSM FILTER	V_{57}	—	7.5	7.7	7.9	
58	COLOR LIMITER	V_{58}	—	6.65	6.9	7.15	
60	Cr/Pr2 IN	V_{60}	—	4.7	5.0	5.3	
61	Cb/Pb2 IN	V_{61}	—	4.7	5.0	5.3	
63	Y2 IN	V_{63}	—	4.7	5.0	5.3	
64	LIGHT AREA DET FILTER	V_{64}	—	—	0.09	0.15	
66	Cr/Pr1 IN	V_{66}	—	4.7	5.0	5.3	
67	Cb/Pb1 IN	V_{67}	—	4.7	5.0	5.3	
68	Y1 IN	V_{68}	—	4.7	5.0	5.3	
70	BPH FILTER	V_{70}	—	5.5	5.8	6.1	
71	DARK AREA DET FILTER	V_{71}	—	—	0.09	0.15	
74	APL FILTER	V_{74}	—	4.8	5.0	5.2	
77	VSM OUT	V_{77}	—	4.1	4.3	4.5	
78	ABCL IN	V_{78}	—	6.1	6.35	6.6	
79	Y_M	V_{79}	—	—	0.1	0.2	
80	Y_S1	V_{80}	—	—	0.1	0.2	

Picture Quality (Sharpness) Block

Characteristics	Symbol	Test Circuit	Test Condition	Min	Typ.	Max	Unit
Y input dynamic range	D_{RY}	—	—	0.7	1.0	1.5	Vp-p
Black detection level shift	V_B	—	(Note P01)	–15	10	15	mV
	V_{B3}	—		35	45	55	
Black stretch amp maximum gain	G_{BS}	—	(Note P02)	2.4	2.8	3.2	dB
Black stretch start point 1	P_{BST1}	—	(Note P03)	20	25	35	IRE
	P_{BST2}	—		50	55	60	
Black stretch start point 2	P_{BS1}	—	(Note P04)	0	5	10	IRE
	P_{BS2}	—		14	21	30	
Black stretch characteristic switch	P_{BSC1}	—	(Note P05)	26	28	30	IRE
	P_{BSC2}	—		–8	–6	–4	
	P_{BSC3}	—		26	28	30	
	P_{BSC4}	—		–5.5	–3	–1	
	P_{BSC5}	—		26	28	30	
	P_{BSC6}	—		–3.5	–2	–0.5	
Black stretch area reinforcement current	IBSA	—	(Note P06)	13	18	23	μA
D.ABL detection voltage	DV_{01}	—	(Note P07)	80	120	160	mV
	DV_{10}	—		240	280	320	
	DV_{11}	—		380	420	460	
D.ABL sensitivity	S_{DAMIN}	—	(Note P08)	—	0.01	0.02	V/V
	S_{DAMAX}	—		0.25	0.28	0.31	
Black level correction	BLC	—	(Note P09)	4.5	6.5	8.5	IRE
Dark area Yγ correction point	P_{DGP}	—	(Note P10)	25	28	33	IRE
Dark area dynamic Yγ gain	G_{DDGMAX}	—	(Note P11)	5.5	6	6.5	dB
Dark area static Yγ gain	G_{DSGMIN}	—	(Note P12)	–6.5	–5	–4	dB
	G_{DSGMAX}	—		2	2.4	2.6	
Light area Yγ correction point	LPG	—	(Note P13)	64	74	80	IRE
Light area dynamic Yγ gain	GLDG	—	(Note P14)	1.1	1.7	2.3	dB
Light area static Yγ gain	G_{LSGMIN}	—	(Note P15)	0.3	0.6	0.9	dB
	G_{LSGMAX}	—		1.4	1.7	2.3	
Dark area detection sensitivity	DAMIN	—	(Note P16)	0.25	0.3	0.37	V
	DACEN	—		0.88	0.98	1.08	
	DAMAX	—		0.95	1.05	1.15	
DC restoration rate	ADT_{100}	—	(Note P17)	0.9	1.1	1.2	times
	ADT_{135}	—		1.2	1.35	1.5	
	ADT_{65}	—		0.55	0.70	0.85	
DC restoration point	V_{DT0}	—	(Note P18)	–5	0	5	%
	V_{DT1}	—		47	49	55	
DC restoration limit	P_{DTL60}	—	(Note P19)	64	67	70	%
	P_{DTL75}	—		74	77	80	
	P_{DTL87}	—		74	80	82	
	P_{DTL100}	—		74	80	82	

Characteristics	Symbol	Test Circuit	Test Condition	Min	Typ.	Max	Unit
Sharpness control peak frequency	F_{AP00}	—	—	10.5	13.5	17	MHz
	F_{AP01}	—		7	9.5	12	
	F_{AP10}	—		5	7.2	7.8	
	F_{AP11}	—		3.5	4.5	6.3	
DC fluctuation at switching sharpness control peak frequency	VRDC	—	(Note P20)	—	0.01	0.02	V
Sharpness control range	G_{MAX00}	—	(Note P21)	15	17.5	19	dB
	G_{MIN00}	—		–4	–0.6	2.5	
	G_{MAX01}	—		15	17.5	19	
	G_{MIN01}	—		–5	–0.3	2.5	
	G_{MAX10}	—		15	17.5	19	
	G_{MIN10}	—		–7	–2.5	1.5	
	G_{MAX11}	—		15	17.5	19	
	G_{MIN11}	—		–12	–5	0	
Sharpness control center characteristic	G_{CEN00}	—	(Note P22)	7	10	13	dB
	G_{CEN01}	—		7	10	13	
	G_{CEN10}	—		7	10	13	
	G_{CEN11}	—		7	10	13	
2T pulse response SRT control	T_{SRT00}	—	(Note P23)	0.9	1.6	2.7	dB
	T_{SRT01}	—		3.5	4.8	7.1	
	T_{SRT10}	—		6.7	8.5	11.3	
	T_{SRT11}	—		11.5	12.5	15.5	
VSM peak frequency	F_{VSM}	—	—	19	19.5	25.5	MHz
VSM gain	G_{V000}	—	(Note P24)	—	–40	–35	dB
	G_{V001}	—		–2	–1.2	–0.4	
	G_{V010}	—		3.7	4.6	5.5	
	G_{V011}	—		7.1	8.2	9.3	
	G_{V100}	—		8.9	10.5	12.1	
	G_{V101}	—		11.4	12.6	13.8	
	G_{V110}	—		13.5	14.4	15.3	
	G_{V111}	—		14.8	15.7	16.6	
VSM mute threshold voltage	V_{SR1}	—	Pins 1, 2, 80	0.62	0.78	0.85	V
	V_{SR2}	—		0.62	0.78	0.85	
	V_{SR580}	—		0.62	0.78	0.85	
VSM limit	V_{LU}	—	(Note P25)	0.55	0.66	0.75	Vp-p
	V_{LD}	—		0.55	0.66	0.75	
Y input to R output delay time	T_{YR}	—	—	110	125	140	ns
Y delay time switch	YDLA	—	(Note P26)	3	5	10	ns
	YDLB	—		7	10	15	
	YDLC	—		10	15	25	
Y group delay correction	G_{AMIN}	—	(Note P27)	–4	–2.5	–1	dB
	G_{BMIN}	—		2.5	3	3.5	
	G_{AMAX}	—		1	1.7	2.4	
	G_{BMAX}	—		–5	–4	–2	

Characteristics	Symbol	Test Circuit	Test Condition	Min	Typ.	Max	Unit
Color detail enhancer	G_{CDE00}	—	(Note P28)	9	10	11	dB
	G_{CDE01}	—		9	10	11	
	G_{CDE10}	—		9	10	11	
	G_{CDE11}	—		9	10	11	
Y detail frequency	F_{YD}	—	—	4	5	6	MHz
Y detail control range	G_{YDMAX}	—	(Note P29)	11	13	15	dB
	G_{YDCEN}	—		8	10	12	
	G_{YDMIN}	—		3	5	7	

Color Difference Block 1: YUV input and matrix

Characteristics	Symbol	Test Circuit	Test Condition	Min	Typ.	Max	Unit
Color difference input dynamic range	D_{RB}	—	—	0.7	0.9	1.0	Vp-p
	D_{RR}	—		0.7	0.9	1.0	
Color difference tint control characteristic	T_{RMAX}	—	—	25	29	33	°
	T_{RMIN}	—		–37	–33	–29	
	T_{BMAX}	—		27	31	35	
	T_{BMIN}	—		–36	–32	–28	
Color SRT peak frequency	F_{B00}	—	—	3.6	4.5	5.4	MHz
	F_{B01}	—		4.6	5.8	7.0	
	F_{R00}	—		3.6	4.5	5.4	
	F_{R01}	—		4.6	5.8	7.0	
Color SRT gain	GS_{B00CEN}	—	(Note S01)	1.5	2.8	4.1	dB
	GS_{B00MAX}	—		2.9	4.2	5.5	
	GS_{B01CEN}	—		2.0	3.3	4.6	
	GS_{B01MAX}	—		3.5	4.8	6.1	
	GS_{R00CEN}	—		3.4	4.7	6.0	
	GS_{R00MAX}	—		5.4	6.7	7.0	
	GS_{R01CEN}	—		3.1	4.4	5.7	
	GS_{R01MAX}	—		5.2	6.5	7.8	
Cb1 input to B output delay time	T_B	—	—	130	155	185	ns
Cr1 input to R output delay time	T_R	—	—	130	155	185	ns
Dynamic Y/C compensation	GC_{BDY1}	—	(Note S02)	1.8	2.25	2.7	dB
	GC_{BDY2}	—		–1.65	–1.2	–0.75	
	GC_{RDY1}	—		1.8	2.25	2.7	
	GC_{RDY2}	—		–1.65	–1.2	–0.75	
YUV gain	G_{Y00}	—	(Note S03)	2.4	3.4	4.4	dB
	G_{Y01}	—		2.4	3.4	4.4	
	G_{CBB}	—		9.5	11.0	12.5	
	G_{PBB}	—		9.9	11.4	12.9	
	G_{PBR}	—		–18.0	–16.0	–14.0	
	G_{CRR}	—		9.5	11.0	12.5	
	G_{PRB}	—		–15.0	–13.5	–12.0	
	G_{PRR}	—		10.0	11.5	13.0	

Characteristics	Symbol	Test Circuit	Test Condition	Min	Typ.	Max	Unit
Green stretch	GrA01	—	(Note S04)	0.98	1	1.02	times
	GrA10	—		0.95	1	1.05	
	GrA11	—		0.93	1	1.07	
	GrB01	—		1.01	1.05	1.10	
	GrB10	—		1.05	1.1	1.15	
	GrB11	—		1.12	1.19	1.26	
	GrC01	—		1.10	1.14	1.18	
	GrC10	—		1.23	1.27	1.31	
	GrC11	—		1.35	1.42	1.49	
	GrD01	—		1.09	1.13	1.17	
	GrD10	—		1.21	1.25	1.29	
	GrD11	—		1.32	1.39	1.46	
	GrE01	—		0.98	1	1.02	
	GrE10	—		0.95	1	1.05	
	GrE11	—		0.93	1	1.07	

Color Difference Block 2

Characteristics	Symbol	Test Circuit	Test Condition	Min	Typ.	Max	Unit
Color difference contrast adjustment characteristic	ΔV_{uCY}	—	(Note A01)	14.5	16.0	17.5	dB
Color adjustment characteristic	Δv_{cCY+}	—	(Note A02)	3.0	4.0	5.0	dB
	ΔvcCY−	—		–35	–22	–17	
R-Y relative phase and amplitude	θ_{RMAX}	—	—	109	111.5	114	°
	θ_{RCNT}	—		98.5	101	103.5	
	θ_{RMIN}	—		88	90	92	
	V_R/V_{BMAX}	—		0.86	0.90	0.94	times
	V_R/V_{BCNT}	—		0.65	0.69	0.73	
	V_R/V_{BMIN}	—		0.42	0.45	0.49	
G-Y relative phase and amplitude	θ_{GMAX}	—	—	251	254	257	°
	θ_{GCNT}	—		244	247	250	
	θ_{GMIN}	—		229	232	235	
	V_G/v_{BMAX}	—		0.43	0.48	0.53	times
	V_G/v_{BCNT}	—		0.33	0.37	0.41	
	V_G/v_{BMIN}	—		0.22	0.25	0.28	
Color difference halftone characteristic	GHT_{RY}	—	(Note A03)	0.47	0.50	0.53	times
	GHT_{GY}	—		0.47	0.50	0.53	
	GHT_{BY}	—		0.47	0.50	0.53	
Color γ characteristic	$V_{\gamma 1}$	—	(Note A04)	0.09	0.23	0.37	Vp-p
	$V_{\gamma 2}$	—		0.26	0.40	0.54	
	$V_{\gamma 3}$	—		0.44	0.58	0.72	
	Δ_{γ}	—		0.60	0.70	0.80	—
Color limiter characteristic	CLT_0	—	(Note A05)	1.45	1.65	1.85	Vp-p
	CLT_1	—		1.80	2.00	2.20	
High-bright color gain	HBC_1	—	(Note A06)	0.02	0.04	0.06	times

Text Block

Characteristics	Symbol	Test Circuit	Test Condition	Min	Typ.	Max	Unit
AC gain (Y1in~R/G/B out)	G_R	—	(Note T01)	3.08	3.45	3.90	times
	G_G	—		3.08	3.45	3.90	
	G_B	—		3.08	3.45	3.90	
AC gain axis difference	$G_{G/R}$	—	—	0.94	1.00	1.06	
	$G_{B/R}$	—		0.94	1.00	1.06	
Frequency characteristic (Y1in~R/G/B out)	G_{fR}	—	At –3dB, sharpness characteristic is flat	30	60	—	MHz
	G_{fG}	—		30	60	—	
	G_{fB}	—		30	60	—	
Frequency characteristic (Cb1/Cr1in~R/G/B out)	G_{fCb}	—	—	10	12.5	—	MHz
	G_{fCr}	—		10	12.5	—	
Unicolor adjustment characteristic	ΔV_u	—	(Note T02)	15.0	16.0	17.0	dB
Brightness adjustment characteristic	V_{brMAX}	—	(Note T03)	4.10	4.45	4.80	V
	V_{brCNT}	—		3.05	3.40	3.75	
	V_{brMIN}	—		1.95	2.30	2.65	
White peak slice level	V_{wps1}	—	(Note T04)	2.20	2.32	2.44	Vp-p
	V_{wps2}	—		2.59	2.74	2.89	
Black peak slice level	V_{bps}	—	(Note T05)	1.15	1.35	1.45	V
RGB output S/N	N_{12}	—	(Note T06)	—	–52	–46	dB
	N_{13}	—		—	–52	–46	
	N_{14}	—		—	–52	–46	
Halftone characteristic	G_{HT1}	—	(Note T07)	0.45	0.50	0.55	times
	G_{HT2}	—		0.45	0.50	0.55	
Halftone on voltage	V_{HT}	—	Pin 79	0.65	0.85	1.05	V
V-BLK pulse output level	V_{VR}	—	—	0.30	0.80	1.30	V
	V_{VG}	—		0.30	0.80	1.30	
	V_{VB}	—		0.30	0.80	1.30	
H-BLK pulse output level	V_{HR}	—	—	0.30	0.80	1.30	V
	V_{HG}	—		0.30	0.80	1.30	
	V_{HB}	—		0.30	0.80	1.30	
BLK pulse delay time	td_{ON}	—	(Note T08)	—	0.00	0.30	μs
	td_{OFF}	—		—	0.08	0.30	
Sub-contrast variable range	Δv_{su+}	—	—	1.95	2.45	2.95	dB
	Δ_{vsu-}	—		–3.8	–3.3	–2.8	
Cut-off voltage variable range	CUT+	—	—	0.42	0.47	0.52	V
	CUT–	—		0.42	0.47	0.52	
RGB output voltage	$\Delta V_{\#12}$	—	—	2.05	2.30	2.55	V
	$\Delta V_{\#13}$	—		2.05	2.30	2.55	
	$\Delta V_{\#14}$	—		2.05	2.30	2.55	
RGB output voltage 3-axis difference	ΔV_{OUT}	—	—	—	0	150	mV

Characteristics	Symbol	Test Circuit	Test Condition	Min	Typ.	Max	Unit
Drive adjustment variable range	DR_{R1+}	—	(Note T09)	2.5	3.0	3.5	dB
	DR_{R1-}	—		–5.5	–5.0	–4.5	
	DR_{R2+}	—		2.5	3.0	3.5	
	DR_{R2-}	—		–5.5	–5.0	–4.5	
	DR_{G1+}	—		2.5	3.0	3.5	
	DR_{G1-}	—		–5.5	–5.0	–4.5	
	DR_{G2+}	—		2.5	3.0	3.5	
	DR_{G2-}	—		–5.5	–5.0	–4.5	
	DR_{G3+}	—		2.5	3.0	3.5	
	DR_{G3-}	—		–5.5	–5.0	–4.5	
	DR_{B1+}	—		2.5	3.0	3.5	
	DR_{B1-}	—		–5.5	–5.0	–4.5	
	DR_{B2+}	—		2.5	3.0	3.5	
	DR_{B2-}	—		–5.5	–5.0	–4.5	
	DR_{B3+}	—		2.5	3.0	3.5	
	DR_{B3-}	—		–5.5	–5.0	–4.5	
Output voltage at P-mute	MU_{RD}	—	—	1.7	1.85	2.0	V
	MU_{GD}	—		1.7	1.85	2.0	
	MU_{BD}	—		1.7	1.85	2.0	
P-mute ON voltage	V_{MUTE}	—	Pin 79	1.90	2.15	2.40	V
Output voltage at blue background	BB_R	—	—	1.0	1.2	1.4	V
	BB_G	—		1.0	1.2	1.4	
	BB_B	—		1.1	1.25	1.4	Vp-p
Input impedance of #78	Zin	—	(Note T10)	24	30	36	kΩ
ACL characteristic	ACL_1	—	(Note T11)	–6.5	–4.5	–2.5	dB
	ACL_2	—		–15.0	–13.5	–11.0	
ABL point	ABL_{P1}	—	(Note T12)	–0.21	–0.16	–0.11	V
	ABL_{P2}	—		–0.28	–0.23	–0.18	
	ABL_{P3}	—		–0.37	–0.32	–0.27	
	ABL_{P4}	—		–0.45	–0.40	–0.35	
	ABL_{P5}	—		–0.54	–0.49	–0.44	
	ABL_{P6}	—		–0.62	–0.57	–0.52	
	ABL_{P7}	—		–0.70	–0.65	–0.60	
	ABL_{P8}	—		–0.75	–0.70	–0.65	
ABL gain	ABL_{G1}	—	(Note T13)	–0.06	–0.02	0.00	V
	ABL_{G2}	—		–0.17	–0.12	–0.07	
	ABL_{G3}	—		–0.34	–0.29	–0.24	
	ABL_{G4}	—		–0.52	–0.47	–0.42	
	ABL_{G5}	—		–0.68	–0.63	–0.59	
	ABL_{G6}	—		–0.85	–0.80	–0.75	
	ABL_{G7}	—		–1.01	–0.96	–0.91	
	ABL_{G8}	—		–1.09	–1.04	–0.99	

Characteristics	Symbol	Test Circuit	Test Condition	Min	Typ.	Max	Unit
RGB output mode	V_{12R}	—	(Note T14)	2.15	2.40	2.65	V
	V_{13R}	—		0.30	0.80	1.30	
	V_{14R}	—		0.30	0.80	1.30	
	V_{12G}	—		0.30	0.80	1.30	
	V_{13G}	—		2.15	2.40	2.65	
	V_{14G}	—		0.30	0.80	1.30	
	V_{12B}	—		0.30	0.80	1.30	
	V_{13B}	—		0.30	0.80	1.30	
	V_{14B}	—		2.15	2.40	2.65	
Y-OUT γ characteristic	γ_1	—	(Note T15)	56	66	76	IRE
	γ_2	—		72	82	92	
	Δ_1	—		0.49	1.24	1.99	dB
	Δ_2	—		–1.67	–0.92	–0.17	
	Δ_3	—		–4.59	–3.84	–3.09	
White-peak blue characteristic	BS_{Pmin}	—	(Note T16)	37	42	47	IRE
	BS_{Pcnt}	—		72	77	82	
	BS_{Pmax}	—		101	106	111	
	BS_{Gmin}	—		2.1	3.1	4.1	dB
	BS_{Gcnt}	—		6.4	7.4	8.4	
	BS_{Gmax}	—		9	10	11	
Forced BLK input threshold voltage	V_{BLKIN}	—	Pin 79	5.1	5.6	6.1	V
ACB insertion pulse phase and amplitude	θ_{ACBR}	—	(Note T17)	—	1	—	H
	θ_{ACBG}	—		—	2	—	
	θ_{ACBB}	—		—	3	—	
	V_{ACB1R}	—		0.15	0.20	0.25	Vp-p
	V_{ACB1G}	—		0.15	0.20	0.25	
	V_{ACB1B}	—		0.15	0.20	0.25	
	V_{ACB2R}	—		0.27	0.32	0.37	
	V_{ACB2G}	—		0.27	0.32	0.37	
	V_{ACB2B}	—		0.27	0.32	0.37	
	V_{ACB3R}	—		0.52	0.57	0.62	
	V_{ACB3G}	—		0.52	0.57	0.62	
	V_{ACB3B}	—		0.52	0.57	0.62	
IK input amplitude	IK_R	—	(Note T18)	0.73	0.93	1.13	Vp-p
	IK_G	—		0.73	0.93	1.13	
	IK_B	—		0.73	0.93	1.13	
IK input cover range	DIK_{in+}	—	(Note T19)	3.00	3.30	3.60	V
	DIK_{in-}	—		–0.50	–0.30	–0.10	

Characteristics	Symbol	Test Circuit	Test Condition	Min	Typ.	Max	Unit
Analog RGB gain	G_{TXR}	—	(Note T20)	3.03	3.40	3.83	times
	G_{TXG}	—		3.03	3.40	3.83	
	G_{TXB}	—		3.03	3.40	3.83	
Analog RGB gain 3-axis difference	$G_{TXG/R}$	—	—	0.94	1.00	1.06	—
	$G_{TXB/R}$	—		0.94	1.00	1.06	
Analog RGB frequency characteristic	Gf_{TXR}	—	At –3dB	30	35	—	MHz
	Gf_{TXG}	—		30	35	—	
	Gf_{TXB}	—		30	35	—	
Analog RGB input dynamic range	DR_{24}	—	—	0.80	1.20	1.50	Vp-p
	DR_{25}	—		0.80	1.20	1.50	
	DR_{26}	—		0.80	1.20	1.50	
Analog RGB white peak slice level	TXV_{WPSR}	—	(Note T21)	2.45	2.70	2.95	Vp-p
	TXV_{WPSG}	—		2.45	2.70	2.95	
	TXV_{WPSB}	—		2.45	2.70	2.95	
Analog RGB black peak limit level	V_{BPSR}	—	(Note T22)	1.15	1.30	1.45	V
	V_{BPSG}	—		1.15	1.30	1.45	
	V_{BPSB}	—		1.15	1.30	1.45	
RGB contrast adjustment characteristic	Δv_{uTXR}	—	(Note T23)	15.5	16.5	18.5	dB
	Δv_{uTXG}	—		15.5	16.5	18.5	
	Δv_{uTXB}	—		15.5	16.5	18.5	
Analog RGB bright adjustment characteristic	$V_{brTXmax}$	—	(Note T24)	3.0	3.2	3.4	V
	$V_{brTXcnt}$	—		2.6	2.8	3.0	
	$V_{brTXmin}$	—		2.1	2.3	2.5	
Analog RGB mode switching voltage	V_{TXON}	—	Pin 2	0.65	0.85	1.05	V
Analog RGB mode switching transfer characteristic	τ_{RYS}	—	(Note T25)	—	15	50	ns
	tP_{RYS}	—		—	20	50	
	Δt_{RYS}	—		—	0	10	
	τ_{FYS}	—		—	10	50	
	tP_{RYS}	—		—	30	50	
	Δt_{RYS}	—		—	0	10	
Text ACL characteristic	$TXACL_1$	—	(Note T26)	–6.7	–4.7	–2.7	dB
	$TXACL_2$	—		–16.5	–14.5	–12.5	
Analog OSD gain	G_{OSDR}	—	(Note T27)	2.95	3.30	3.70	times
	G_{OSDG}	—		2.95	3.30	3.70	
	G_{OSDB}	—		2.95	3.30	3.70	
Analog OSD gain 3-axis difference	$G_{OSDG/R}$	—	—	0.94	1.00	1.06	—
	$G_{OSDB/R}$	—		0.94	1.00	1.06	
Analog OSD frequency characteristic	Gf_{OSDR}	—	At –3dB	35	40	—	MHz
	Gf_{OSDG}	—		35	40	—	
	Gf_{OSDB}	—		35	40	—	
Analog OSD input dynamic range	DR_{18}	—	—	0.80	1.20	1.50	Vp-p
	DR_{19}	—		0.80	1.20	1.50	
	DR_{21}	—		0.80	1.20	1.50	

Characteristics	Symbol	Test Circuit	Test Condition	Min	Typ.	Max	Unit
Analog OSD input white peak slice level	$OSDV_{WPSR}$	—	(Note T28)	2.45	2.70	2.95	Vp-p
	$OSDV_{WPSG}$	—		2.45	2.70	2.95	
	$OSDV_{WPSB}$	—		2.45	2.70	2.95	
Analog OSD black peak limit level	$OSDV_{BPSR}$	—	(Note T29)	1.30	1.45	1.60	V
	$OSDV_{BPSG}$	—		1.30	1.45	1.60	
	$OSDV_{BPSB}$	—		1.30	1.45	1.60	
OSD contrast adjustment characteristic	$V_{UOSDR11}$	—	(Note T30)	0.58	0.64	0.71	Vp-p
	$V_{UOSDG11}$	—		0.58	0.64	0.71	
	$V_{UOSDB11}$	—		0.58	0.64	0.71	
	$V_{UOSDR10}$	—		0.47	0.53	0.59	
	$V_{UOSDG10}$	—		0.47	0.53	0.59	
	$V_{UOSDB10}$	—		0.47	0.53	0.59	
	$V_{UOSDR01}$	—		0.31	0.37	0.45	
	$V_{UOSDG01}$	—		0.31	0.37	0.45	
	$V_{UOSDB01}$	—		0.31	0.37	0.45	
	$V_{UOSDR00}$	—		0.19	0.22	0.24	
	$V_{UOSDG00}$	—		0.19	0.22	0.24	
	$V_{UOSDB00}$	—		0.19	0.22	0.24	
Analog OSD bright adjustment characteristic	V_{brOSD0}	—	(Note T31)	2.20	2.40	2.60	V
	V_{brOSD1}	—		2.05	2.25	2.45	
	V_{brOSD2}	—		1.95	2.15	2.35	
	V_{brOSD3}	—		1.80	2.00	2.20	
Analog OSD mode switching voltage	V_{OSDON1}	—	Pin 80	2.05	2.30	2.55	V
	V_{OSDON2}	—	Pin 1	2.05	2.30	2.55	
Analog OSD mode switching transfer characteristic	τ_{RYS1}	—	(Note T32)	—	15	50	ns
	tP_{RYS1}	—		—	20	50	
	ΔtP_{RYS1}	—		—	0	10	
	τ_{FYS1}	—		—	10	50	
	tP_{RYS1}	—		—	30	50	
	ΔtP_{RYS1}	—		—	0	10	
	τ_{RYS2}	—		—	15	50	
	tP_{RYS2}	—		—	20	50	
	ΔtP_{RYS2}	—		—	0	10	
	τ_{FYS2}	—		—	10	50	
	tP_{RYS2}	—		—	30	50	
	ΔtP_{RYS2}	—		—	0	10	
OSD ACL characteristic	$OSDACL_1$	—	(Note T33)	—	0.00	—	dB
	$OSDACL_2$	—		—	0.00	—	
	$OSDACL_3$	—		–6.7	–4.7	–2.7	
	$OSDACL_4$	—		–16.5	–14.5	–12.5	

Characteristics		Symbol	Test Circuit	Test Condition	Min	Typ.	Max	Unit
OSD blending characteristic		$\alpha 41TV_1$	—	(Note T34)	–7	–6	–5	dB
		$\alpha 42TV_1$	—		–7	–6	–5	
		$\alpha 43TV_1$	—		–7	–6	–5	
		$\alpha 41TV_2$	—		–4	–3	–2	
		$\alpha 42TV_2$	—		–4	–3	–2	
		$\alpha 43TV_2$	—		–4	–3	–2	
		$\alpha 41TV_3$	—		—	–55	–50	
		$\alpha 42TV_3$	—		—	–55	–50	
		$\alpha 43TV_3$	—		—	–55	–50	
		$\alpha 41OSD_1$	—		–6.5	–5.5	–4.5	
		$\alpha 42OSD_1$	—		–6.5	–5.5	–4.5	
		$\alpha 43OSD_1$	—		–6.5	–5.5	–4.5	
		$\alpha 41OSD_2$	—		–12.0	–10.5	–9.0	
		$\alpha 42OSD_2$	—		–12.0	–10.5	–9.0	
		$\alpha 43OSD_2$	—		–12.0	–10.5	–9.0	
		$\alpha 41OSD_3$	—		—	–40	–30	
		$\alpha 42OSD_3$	—		—	–40	–30	
		$\alpha 43OSD_3$	—		—	–40	–30	
Input crosstalk	Y → RGB input	$V_{V \to A}$	—	Input: Signal 1 (f_o = 4 MHz, Amplitude 0.7 Vp-p)	—	–50	–45	dB
	Y → OSD input	$V_{V \to O}$	—		—	–55	–45	
	RGB input → Y	$V_{A \to V}$	—		—	–50	–45	
	RGB input → OSD input	$V_{A \to O}$	—		—	–50	–45	
	OSD input → Y	$V_{O \to V}$	—		—	–45	–40	
	OSD input → RGB input	$V_{O \to A}$	—		—	–50	–45	
	RGB input in three axes	—	—	Input: Signal 1 (f_o = 1 MHz, Amplitude 0.7 Vp-p)	—	–50	–40	
	OSD input in three axes	—	—		—	–50	–40	
Blue stretch point/gain		BLP_{min}	—	(Note T35)	23	28	33	IRE
		BLP_{max}	—		55	60	65	
		BLG_{min}	—		2.4	2.9	3.4	dB
		BLG_{max}	—		5.4	6.4	7.4	
Blue stretch γ correction		$BL\gamma 1$	—	(Note T36)	84	89	94	IRE
		$BL\gamma 2$	—		89	94	99	
		$BL\gamma 3$	—		93	98	103	
		$BL\gamma 4$	—		98	103	108	
White letters improvement		WPL1	—	(Note T37)	16	21	25	Vp-p
		WPL2	—		51	56	61	
		WPL3	—		97	102	107	

Sync Block

Characteristics	Symbol	Test Circuit	Test Condition	Min	Typ.	Max	Unit
Sync input horizontal sync phase	S_{PH}	—	(Note HA01)	0.55	0.65	0.75	µs
HD input horizontal sync phase	HD_{PH}	—	(Note HA02)	0.58	0.68	0.78	µs
Polarity detecting rage	HD_{DUTY1}	—	(Note HA03)	—	0.5	2.0	%
	HD_{DUTY2}	—		62	67	72	
	HD_{DUTY3}	—		—	99.5	98	
	HD_{DUTY4}	—		47.5	52.5	57.5	
Sync input threshold amplitude	V_{thS00}	—	(Note HA04)	10	16	22	%
	V_{thS01}	—		18	24	30	
	V_{thS10}	—		26	32	38	
	V_{thS11}	—		34	40	46	
HD input threshold voltage	V_{thHD}	—	(Note HA05)	0.65	0.75	0.85	Vp-p
Horizontal picture position (phase) adjustment variable range	ΔH_{SFT-}	—	(Note HA06)	11	12.5	14	%
	ΔH_{SFT+}	—		11	12.5	14	
Horizontal picture position (phase) shift switching amount	H_{SFT}	—	—	5.2	6.7	9.2	%
Curve correction variable amount	$\Delta H_{\#40}$	—	(Note HA07)	2.9	3.4	3.9	%
Clamp pulse phase/width/level	CP_{S0}	—	(Note HA08)	3.1	3.8	4.5	%
	CP_{W0}	—		2.0	2.5	3.0	
	CP_{V0}	—		4.7	5.0	5.3	V
	CP_{S1}	—		0	0.7	1.5	%
	CP_{W1}	—		1.9	2.4	2.9	
	CP_{V1}	—		4.7	5.0	5.3	V
	CP_{S2}	—		3.2	4.2	5.2	%
	CP_{W2}	—		2.2	2.7	3.2	
	CP_{V2}	—		4.7	5.0	5.3	V
Black peak detection pulse phase	HBP_{S00a}	—	(Note HA09)	1.2	3.0	5.9	%
	HBP_{S00b}	—		1.2	3.0	5.9	
	HBP_{S01a}	—		6.0	8.0	11.0	
	HBP_{S01b}	—		6.0	8.0	11.0	
	HBP_{s10a}	—		10.0	13.0	15.0	
	HBP_{s10b}	—		10.0	13.0	15.0	
	HBP_{s11a}	—		16.0	18.0	21.0	
	HBP_{s11b}	—		16.0	18.0	21.0	
FBP threshold	V_{thFBP}	—	(Note HA10)	4.8	5.3	5.8	V
HVCO oscillation start voltage	V_{VCO}	—	Pin 42: Monitor, V_{CC} voltage	3.0	4.0	5.0	V
H-OUT start voltage	V_{HON}	—	Pin 37: Monitor, V_{CC} voltage	5.0	6.0	7.0	V
H-OUT stop voltage	V_{HOFF}	—	Pin 37: Monitor, V_{CC} voltage	4.3	5.3	6.3	V
H-OUT pulse duty	TH_A	—	(Note HB01)	38	41	43	%
	TH_B	—		44	47	49	

Characteristics		Symbol	Test Circuit	Test Condition	Min	Typ.	Max	Unit
Horizontal free-run frequency		F15K	—	(Note HB02)	15.59	15.75	15.91	kHz
		F28K	—		27.90	28.125	28.35	
		F31K	—		31.19	31.5	31.82	
		F33K	—		33.41	33.75	34.09	
		F37K	—		37.60	37.9	38.40	
		F45K	—		44.52	45.0	45.48	
Horizontal oscillation frequency variable range		$F15K_{MIN}$	—	(Note HB03)	14.78	15.08	15.38	kHz
		$F15K_{MAX}$	—		16.37	16.70	17.03	
		$F28K_{MIN}$	—		26.00	26.90	27.80	
		$F28K_{MAX}$	—		28.90	29.70	30.60	
		$F31K_{MIN}$	—		29.47	30.06	30.65	
		$F31K_{MAX}$	—		32.72	33.39	34.06	
		$F33K_{MIN}$	—		31.41	31.94	32.57	
		$F33K_{MAX}$	—		34.91	35.62	36.33	
		$F37K_{MIN}$	—		36.50	37.30	38.20	
		$F37K_{MAX}$	—		40.20	41.10	42.10	
		$F45K_{MIN}$	—		43.20	44.00	44.80	
		$F45K_{MAX}$	—		47.85	48.65	49.45	
Horizontal oscillation control sensitivity		BH15K	—	Hz/0.1 V (Note HB04)	176	220	264	—
		BH28K	—		320	400	480	
		BH31K	—		352	440	528	
		BH33K	—		376	470	564	
		BH37K	—		390	480	570	
		BH45K	—		520	650	780	
H-OUT output voltage		V_{HOH}	—	(Note HB05)	4.8	5.1	5.2	V
		V_{HOL}	—		—	0.1	0.3	
Horizontal oscillation frequency control voltage threshold	Pin 55	V_{fHSW1}	—	—	1.7	2.0	2.3	V
	Pin 41	V_{fHSW2L}	—		1.3	1.5	1.7	
		V_{fHSW2M}	—		4.3	4.5	4.7	
		V_{fHSW2H}	—		7.3	7.5	7.7	
DAC switch voltage	DAC1	$VDAC_{1H}$	—	TEST = (00), DAC1 = (0)	8.5	9.0	—	V
		$VDAC_{1L}$	—	TEST = (00), DAC1 = (1)	—	0.3	0.7	
	DAC2	$VDAC_{2H}$	—	TEST = (00), DAC2 = (1)	8.5	9.0	—	
		$VDAC_{2L}$	—	TEST = (00), DAC2 = (0)	—	0.3	0.7	
VP output pulse width		VP_W	—	(Note V01)	4	4.5	5	H
Vertical free-run (maximum pull-in range)	000	VPt0	—	—	1278	1281	1284	H
	001	VPt1	—		846	849	852	
	010	VPt2	—		722	725	728	
	011	VPt3	—		657	660	663	
	100	VPt4	—		610	613	616	
	101	VPt5	—		360	363	366	
	110	VPt6	—		304	307	310	
Vertical minimum pull-in range		T_{VPULL}	—	(Note V02)	47	48	49	H

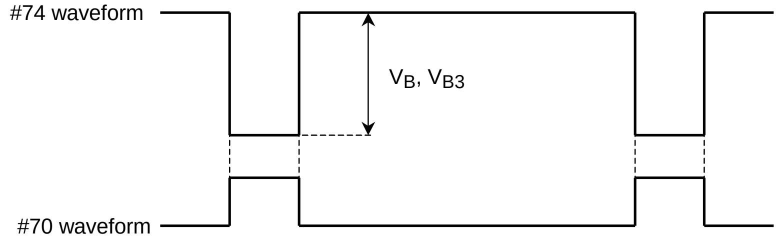
Characteristics		Symbol	Test Circuit	Test Condition	Min	Typ.	Max	Unit
Vertical black peak detection pulse	000	$VBPP_{0E}$	—	(Note V03)	51	52	53	H
		$VBPP_{0S}$	—		1099.5	1100.5	1101.5	
	001	$VBPP_{1E}$	—		51	52	53	
		$VBPP_{1S}$	—		729.5	730.5	731.5	
	010	$VBPP_{2E}$	—		49.5	50.5	51.5	
		$VBPP_{2S}$	—		599.5	600.5	601.5	
	011	$VBPP_{3E}$	—		49.5	50.5	51.5	
		$VBPP_{3S}$	—		544.5	545.5	546.5	
	100	$VBPP_{4E}$	—		51	52	53	
		$VBPP_{4S}$	—		499.5	500.5	501.5	
	101	$VBPP_{5E}$	—		51	52	53	
		$VBPP_{5S}$	—		289.5	290.5	291.5	
	110	$VBPP_{6E}$	—		51	52	53	
		$VBPP_{6S}$	—		239.5	240.5	241.5	
Vertical blanking end phase		V_{BLKMIN}	—	(Note V04)	15	16	17	H
		V_{BLKMAX}	—		45	46	47	
VP output voltage	High	V_{VPH}	—	pin 35 voltage	4.6	5.0	5.4	V
	Low	V_{VPL}	—		—	0.1	0.5	
SYNC input to VP output delay time		15.75 kHz	—	—	10.0	11.6	13.4	μs
		28.125 kHz	—		5.4	6.4	8.8	
		31.5 kHz	—		4.8	5.8	7.6	
		33.75 kHz	—		4.4	5.4	7.2	
		37.9 kHz	—		3.9	4.8	6.6	
		45 kHz	—		3.1	4.1	5.9	
Compression BLK 1 (start phase)	000	$CBLK1_{000min}$	—	—	1087	1088	1089	H
		$CBLK1_{000max}$	—		1117	1118	1119	
	001	$CBLK1_{001min}$	—		719	720	721	
		$CBLK1_{001max}$	—		749	750	751	
	010	$CBLK1_{010min}$	—		591	592	593	
		$CBLK1_{010max}$	—		621	622	623	
	011	$CBLK1_{011min}$	—		527	528	529	
		$CBLK1_{011max}$	—		557	558	559	
	100	$CBLK1_{100min}$	—		487	488	489	
		$CBLK1_{100max}$	—		517	518	519	
	101	$CBLK1_{101min}$	—		279	280	281	
		$CBLK1_{101max}$	—		309	310	311	
	110	$CBLK1_{110min}$	—		223	224	225	
		$CBLK1_{110max}$	—		253	254	255	

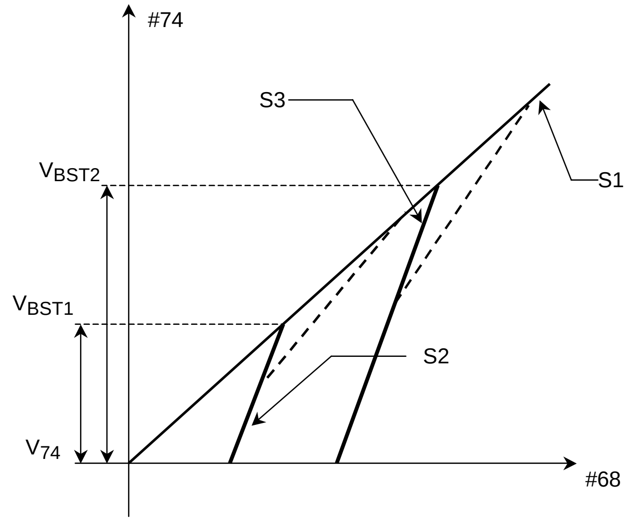
Characteristics		Symbol	Test Circuit	Test Condition	Min	Typ.	Max	Unit
Compression BLK 2 (end phase)	000	$CBLK2_{000min}$	—	—	49	50	51	H
		$CBLK2_{000max}$	—		77	78	79	
	001	$CBLK2_{001min}$	—		49	50	51	
		$CBLK2_{001max}$	—		77	78	79	
	010	$CBLK2_{010min}$	—		49	50	51	
		$CBLK2_{010max}$	—		77	78	79	
	011	$CBLK2_{011min}$	—		49	50	51	
		$CBLK2_{011max}$	—		77	78	79	
	100	$CBLK2_{100min}$	—		49	50	51	
		$CBLK2_{100max}$	—		77	78	79	
	101	$CBLK2_{101min}$	—		49	50	51	
		$CBLK2_{101max}$	—		77	78	79	
	110	$CBLK2_{110min}$	—		49	50	51	
		$CBLK2_{110max}$	—		77	78	79	
External V-BLK input current		I_{EXTBLK}	—	Pin 35 input current	520	625	780	μA

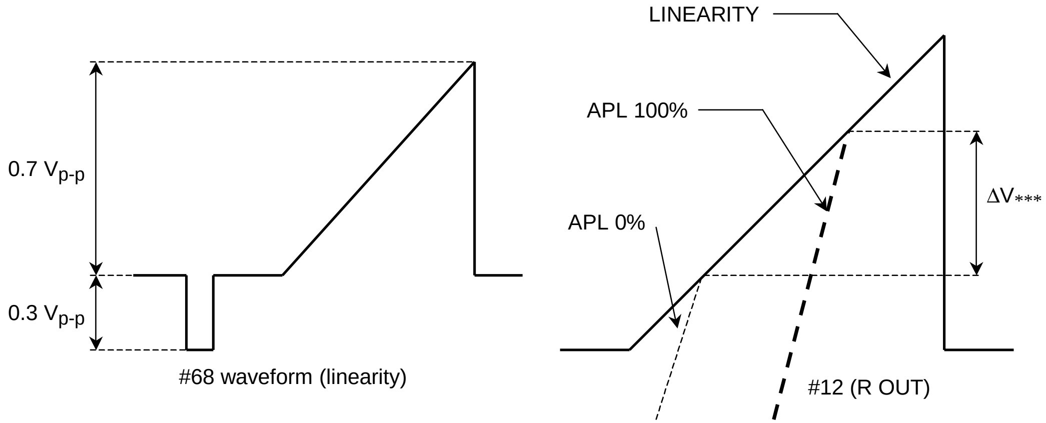
Test Condition for Picture Quality (Sharpness) Block

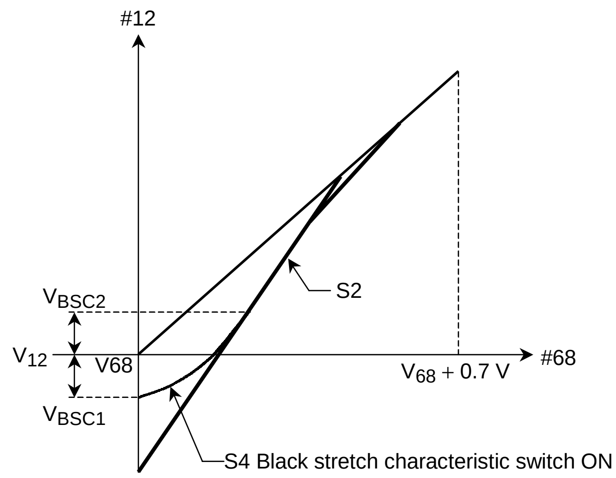
Common Test Condition for Picture Quality (Sharpness) Block

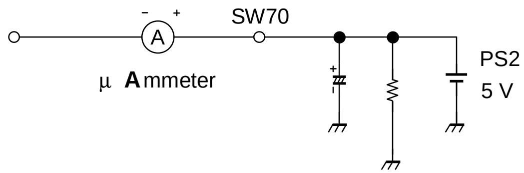
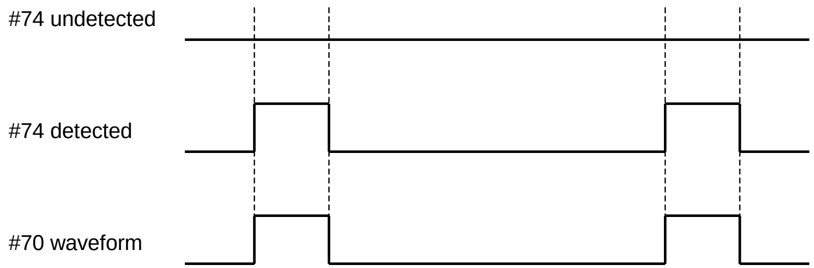
1. SW67 = SW66 = B, SW63 = B, SW60 to SW61 = B, SW44 = ON, SW40 = B, SW18 to SW26 = A, SW77 = OPEN
2. Send bus control data as preset values, turn ACB operation switching to ACB OFF (00), select Sync input (1), turn P-MODE to Normal 1(000), WPL-LEVEL to max (111), and change subaddress (1C) to (03).
3. Input sync signal, which is in sync with input signal for testing except “Sweep”, to #53 (Sync input). “H-Freq.” should be the same frequency as the one of #53.
4. Set Y/color difference input mode to (0), sync separator level to 20 % (01), and vertical free-running frequency to 307H (110).

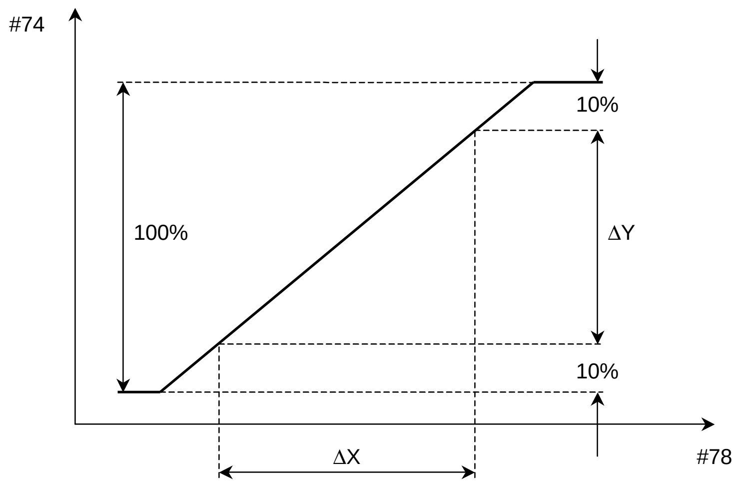
Note No.	Characteristics	Test Conditions SW Mode					Test Method (Test condition: V_{CC} = 9 V/2 V, Ta = 25 ± 3°C)
		SW71	SW70	SW68	SW64	SW74	
P01	Black detection level shift	B	C	C	B	OPEN	1. Connect external power supply PS to #68, and monitor #70 and #74. 2. Set black stretch point 1 to OFF (000), and black detection level to 0 IRE (1). 3. Increase PS voltage from 4.95 V in steps of 1 mV. At the moment when #70 picture period (High) drops to Low level, monitor DC difference on #74 V_B. 4. Set black detection level to 3 IRE (0). 5. Repeat the step 3 above and monitor DC difference, V_{B3} on #74. 
P02	Black stretch amp maximum gain	B	A	A	B	OPEN	1. Set SW70 to A (maximum gain), and input 500-kHz sine wave to TPA. 2. Adjust signal amplitude to 0.1 Vp-p on #68. 3. Set black stretch point 1 to OFF (000), and measure #74 amplitude V_A. 4. Set black stretch point 1 to 001 (black stretch ON), and measure #74 amplitude V_B. 5. Calculate GBS using a following equation. $GBS = 20 \times \ell og\ (V_B \div V_A)$ [dB]

Note No.	Characteristics	Test Conditions					Test Method (Test condition: V_{CC} = 9 V/2 V, Ta = 25 ± 3°C)
		SW Mode					
		SW71	SW70	SW68	SW64	SW74	
P03	Black stretch start point 1	A	A	C	B	OPEN	1. Set SW70 to A (maximum gain), and black stretch point 1 to OFF (000). Apply 0 V to #71. 2. Connect external power supply PS to #68, increase voltage from V_3, and plot #74 voltage change S1. The #74 voltage is set as V_0 when V_3 is applied, and as V_{100} when V_3 + 0.7 V is applied. 3. Set black stretch point 1 to minimum (001), increase PS voltage from V_3, and then plot #74 voltage change S2. 4. Set black stretch point to maximum (111), repeat 3 above, then plot #74 voltage change S3. 5. Determine intersection points of S1, S2 (V_{BST1}), and S3 (V_{BST2}) as shown in the figure below. Also calculate P_{BST1} and P_{BST2} using following equations. V_Z [V] = V_{100} [V] − V_0 [V] P_{BST1} [(IRE)] = [(V_{BST1} [V] − V_{74} [V]) ÷ V_Z] × 100 (IRE) P_{BST2} [(IRE)] = [(V_{BST2} [V] − V_{74} [V]) ÷ V_Z] × 100 (IRE) 

Note No.	Characteristics	Test Conditions SW Mode					Test Method (Test condition: V_{CC} = 9 V/2 V, Ta = 25 ± 3°C)
		SW71	SW70	SW68	SW64	SW74	
P04	Black stretch start point 2	A	A	A	B	ON	1. Set black stretch point 1 to OFF (000), apply 0 V to #71, input TG7 LINEARITY to TPA, adjust amplitude on #68 as shown in the figure below, set unicolor to center (1000000), and measure amplitude of #12 (R OUT), V_{P12}. 2. Set black stretch point 1 to 001 (black stretch ON), connect external power supply PS to #74, and monitor #12 (R OUT). 3. Set black stretch start point 2 data to minimum (00). When PS is V_{74} (APL 0%), and V_{74} + 1.0 V (APL 100%), determine black stretch start point difference ΔV_{00} as shown in the figure below. (Monitor input waveform and output waveform with an oscilloscope, adjust the both waveforms to have the same amplitude (gradient), and compare them to determine the bend point of the output.) 4. Set black stretchstart point 2 data to maximum (11), determine black stretch start point difference $\Delta V1_1$. 5. Calculate following equations. $P_{BS1} = (\Delta V_{00}/V_{P12}) \times 100$ $P_{BS2} = (\Delta V_{11}/V_{P12}) \times 100$ 

Note No.	Characteristics	Test Conditions					Test Method (Test condition: V_{CC} = 9 V/2 V, Ta = 25 ± 3°C)
		SW Mode					
		SW71	SW70	SW68	SW64	SW74	
P05	Black stretch characteristic switch	A	A	C	B	OPEN	1. Set SW70 to A (maximum gain), black stretch point 1 (18) to maximum (E0), subaddress (1C) data to (00) and (1E) data to (08). 2. Apply 0 V to #71 and connect external power supply PS to #68. Set PS to V_{68} + 0.7 V, and adjust unicolor so that DC level of #12 is +1.0 V. Plot voltage change S4 of #12 (voltage in picture period). 3. Determine intersection points (V_{BSC1} and V_{BSC2}) of S2 and S4 obtained from the plot in black stretch start point 1. Then calculate P_{BSC1} and P_{BSC2} using following equation. 4. Set black stretch characteristic switch subaddress data (1C)/(1E) to (20)/(00) and (20)/(08) respectively. As described in steps 2 and 3, determine intersection points (V_{BSC3}, V_{BSC4}, V_{BSC5} and V_{BSC6}) and calculate P_{BSC3}, P_{BSC4}, P_{BSC5} and P_{BSC6}. $P_{BSC*} = (V_{BSC*}\ [V] - V_{12}\ [V]) \div 1.0 \times 100$ [(IRE)] 

Note No.	Characteristics	Test Conditions SW Mode SW71	SW70	SW68	SW64	SW74	Test Method (Test condition: V_{CC} = 9 V/2 V, Ta = 25 ± 3°C)
P06	Black stretch area reinforcement current	B	—	C	B	ON	1. Connect external power supply PS1 to #68. 2. Leave SW70 open, put an ammeter between SW70A and #70, connect external power supply PS2 to SW70A, set PS1 to 5.7 V, and set PS2 to 5 V. 3. Measure current value IBSA0 and IBSA1 when bus data of black stretch area reinforcement [18] is set to ON [80] and OFF [81]. Calculate IBSA using the following equation. IBSA = IBSA0 − IBSA1 
P07	D.ABL detection voltage	B	A	C	B	OPEN	1. Set D.ABL sensitivity to maximum (11), and black stretch point 1 to OFF (000). 2. Connect external power supply PS to #78 and decrease voltage from 6.5 V. 3. Repeat 2 when D.ABL detection voltage is changed to 00, 01, 10, and 11. At the moment when #74 picture period changes to Low, measure respective PS voltages V_{00}, V_{01}, V_{10}, and V_{11}. 4. Calculate voltage differences between V_{00} and V_{01} (DV_{01}), between V_{00} and V_{10} (DV_{10}), and between V_{00} and V_{11} (DV_{11}) $DV_{***} = V_{00} - V_{01}$ (V_{10}, V_{11}) 

<table>
<tr><th rowspan="3">Note No.</th><th rowspan="3">Characteristics</th><th colspan="5">Test Conditions</th><th rowspan="3">Test Method (Test condition: V_{CC} = 9 V/2 V, Ta = 25 ± 3°C)</th></tr>
<tr><th colspan="5">SW Mode</th></tr>
<tr><th>SW71</th><th>SW70</th><th>SW68</th><th>SW64</th><th>SW74</th></tr>
<tr><td>P08</td><td>D.ABL sensitivity</td><td>B</td><td>A</td><td>C</td><td>B</td><td>ON</td><td>1. Set black stretch point 1 to OFF (000), and connect external power supply to #78.
2. Set D.ABL detection voltage to minimum (00). Interrelation between #78 voltage and #74 voltage when D.ABL sensitivity is set to minimum (00) and maximum (11) can be plotted as figure shown below.
3. Measure gradients SDAMIN and SDAMAX using the figure below.
$S_{DAMIN} = \Delta Y/\Delta X$ $S_{DAMAX} = \Delta Y/\Delta X$

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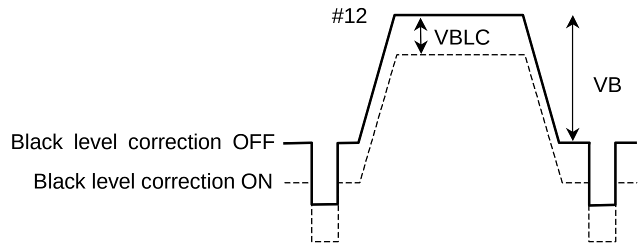
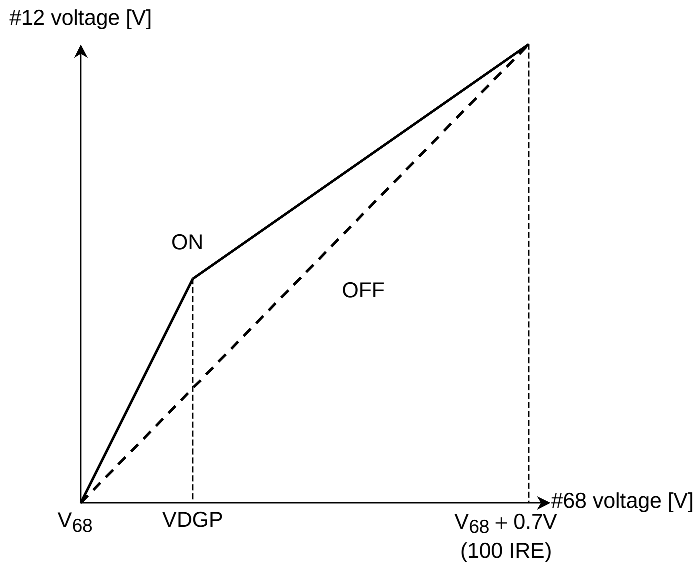
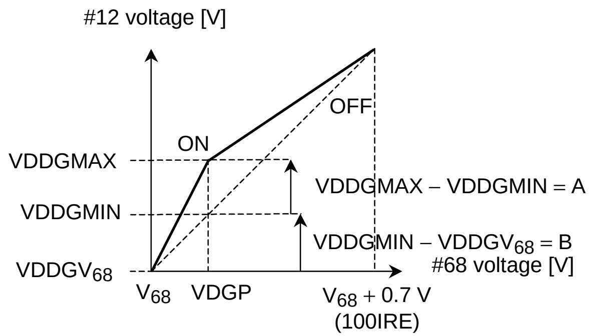
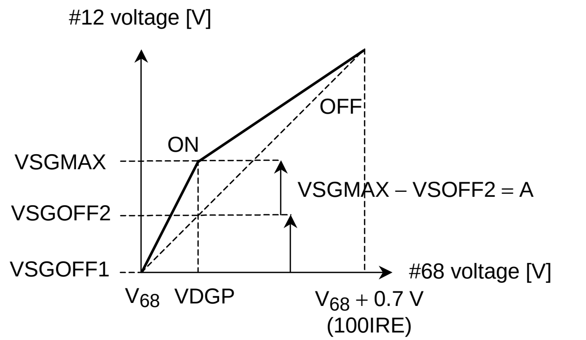
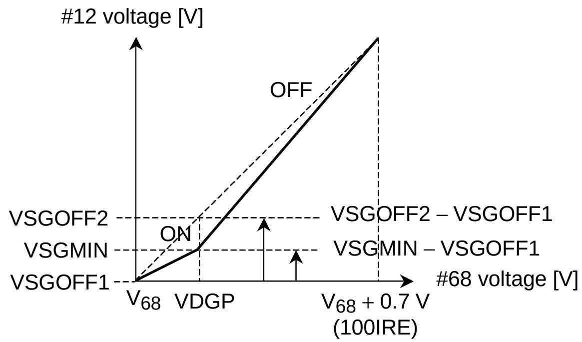
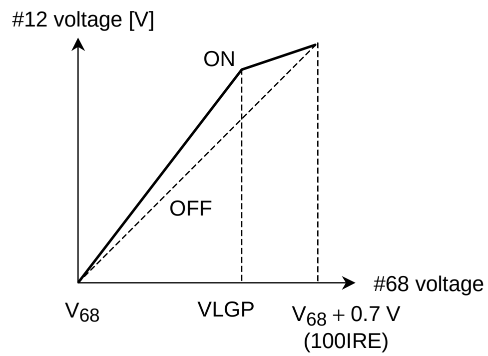
Note No.	Characteristics	Test Conditions SW Mode SW71	 SW70	 SW68	 SW64	 SW74	Test Method (Test condition: V_{CC} = 9 V/2 V, Ta = 25 ± 3°C)
P09	Black level correction	B	A	A	B	OPEN	1. Set black stretch point 1[18] to OFF (00). 2. Input signal of 0.7-V picture period amplitude to #68, and measure #12 picture period amplitude VB [V]. 3. Set black level correction [18] to ON [04], determine DC change VBLC [V], and calculate BLC [V] using the following equation BLC = (VBLC/VB)] × 100 [(IRE)] 

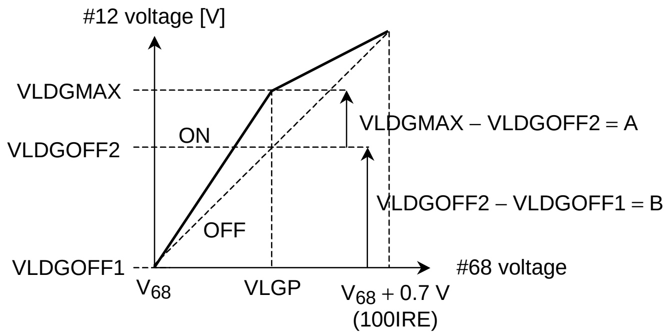
Note No.	Characteristics	Test Conditions SW Mode					Test Method (Test condition: V_{CC} = 9 V/2 V, Ta = 25 ± 3°C)
		SW71	SW70	SW68	SW64	SW74	
P10	Dynamic Yγ correction point	A	B	C	B	OPEN	1. Connect external power supply PS1 to #68, PS2 to TP1, and set PS2 to 0 V. 2. Set dark area dynamic Yγ gain VS dark area to MIN (00), static Yγ gain1 to OFF (000). 3. Increase PS1 from V_{68} [V] to V_{68} [V] + 0.7 V and plot voltage change of #12 picture period. Take 0 for V_{68} [V] when the change is plotted. (V_{68} is pin voltage of pin 68) 4. Set dark area dynamic Yγ gain VS dark area max (11), static Yγ gain1 to max (111) and PS2 to 1.2 V. 5. Increase PS1 from V_{68} [V] to V_{68} [V] + 0.7 V and plot voltage change of #12 picture period. 6. Measure VDGP by the following figure, and P_{DGP} using the following equation. DGP = (VDGP [V] − V_{68} [V])/0.7 [V] × 100 

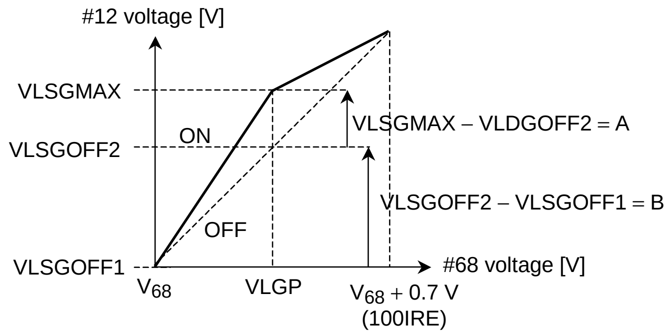
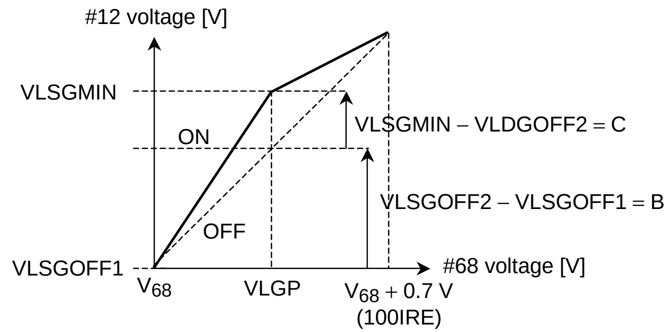
Note No.	Characteristics	Test Conditions					Test Method (Test condition: V_{CC} = 9 V/2 V, Ta = 25 ± 3°C)
		SW Mode					
		SW71	SW70	SW68	SW64	SW74	
P11	Dark area dynamic Yγ gain	A	B	C	B	OPEN	1. Connect external power supply PS1 to #68, external power supply PS2 to TP1, and set PS2 to 0 V. 2. Set dark area dynamic Yγ gain [1C] to MIN [03], and dark area static Yγ gain [1C] to 0dB [17]. 3. Set PS1 to V_{68} [V], and measure #12 picture period voltage $VDDGV_{68}$ [V]. Set PS1 VDGP [V], and measure #12 picture period voltage VDDGMIN [V]. 4. Set dark area dynamic Yγ gain [1C] to MAX [D7], PS2 to 1.2 V, measure voltage VDDGMAX [V] of #12 picture period when PS1 is VDGP [V], and calculate the following equations. VDDGMAX – VDDGMIN = A VDDGMIN – $VDDGV_{68}$ = B GDDGMAX = 20 ℓog [B/(B-A)] [dB] 

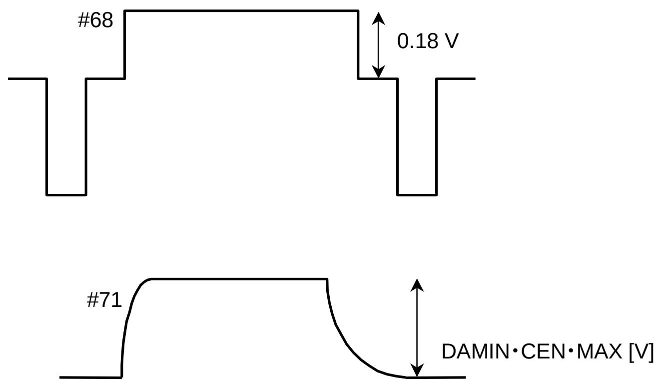
Note No.	Characteristics	Test Conditions SW Mode SW71	SW70	SW68	SW64	SW74	Test Method (Test condition: V_{CC} = 9 V/2 V, Ta = 25 ± 3°C)
P12	Dark area static Yγ gain	A	B	C	B	OPEN	1. Connect external power supply PS1 to #68, external power supply PS2 to TP1, and set PS2 to 0 V. 2. Set dark area dynamic Yγ gain [1C] to MIN [03], and dark area static Yγ gain [1C] to OFF [03]. 3. Set PS1 to V_{68} [V], and measure #12 picture period voltage VSGOFF1 [V]. 4. Set PS1 to VDGP [V], and measure #12 picture period voltage VSGOFF2 [V]. 5. Set dark area static Yγ gain [1C] to MAX [1F], PS1 to VDGP [V], measure #12 picture period voltage VSGMAX, and calculate GDSGMAX using the following equations. VSGMAX – VSGOFF2 = A VSGOFF2 – VSGOFF1 = B GDSGMAX = 20 × ℓog [B/(B - A)] [dB]  6. Set dark area static Yγ gain [1C] to MIN [07], PS1 to VDGP [V], measure #12 picture period voltage VSGMIN, and calculate GDSGMIN using the following equation. GDSGMIN = 20 × ℓog [(VSGMIN – VSGOFF1)/(VSGOFF2 – VSGOFF1)] [dB] 

Note No.	Characteristics	Test Conditions SW Mode SW71	SW70	SW68	SW64	SW74	Test Method (Test condition: V_{CC} = 9 V/2 V, Ta = 25 ± 3°C)
P13	Light area Yγ correction point	A	B	C	A	OPEN	1. Connect external power supply PS1 to #68, external power supply PS2 to TP1, and set PS2 to 0 V. 2. Set dark area static Yγ gain [1C] to 0dB [17], and bright area static Yγ gain [1C] to 0dB [17]. 3. Increase PS1 from V_{68} [V] to V_{68} [V] + 0.7 [V], and plot the voltage change of #12 picture period. Take 0 for V_{68} [V] when the change is plotted. (V_{68} is pin voltage of pin 68) 4. Set light area static Yγ gain [1C] to MAX [04]. 5. Increase PS1 from V_{68} [V] to V_{68} [V] + 0.7 [V], and plot the voltage change of #12 picture period. 6. Measure VLGP using the following figure, and PLGP using the following equation. LGP = (VLGP [V] – V_{68} [V])/0.7 [V] × 100 (IRE) 

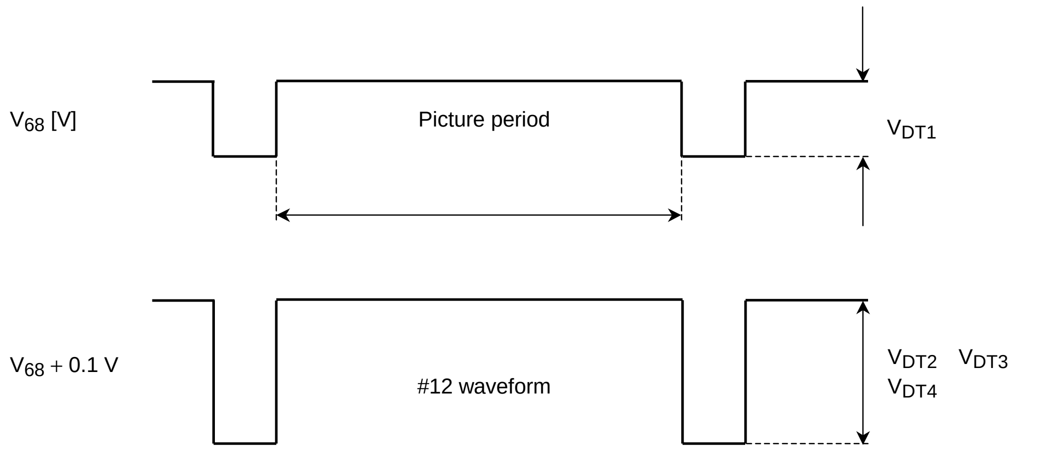
Note No.	Characteristics	Test Conditions SW Mode					Test Method (Test condition: V_{CC} = 9 V/2 V, Ta = 25 ± 3°C)
		SW71	SW70	SW68	SW64	SW74	
P14	Light area dynamic Yγ gain	A	B	C	A	OPEN	1. Connect external power supply PS1 to #68, external power supply PS2 to TP7, and set PS2 to 1.2 V. 2. Set dark area static Yγ gain [1C] to 0dB [17], and light area static Yγ gain [1C] to 0dB [17]. 3. Set PS1 to V_{68} [V], and measure #12 picture period voltage VLDGOFF1. 4. Set PS1 to VLGP [V], and measure #12 picture period voltage VLDGOFF2. 5. Set light area static Yγ gain [1C] to MAX [14], PS2 to 0 V, PS1 to VLGP [V], determine #12 picture period voltage VLDGMAX [V] using the following equations. VLDGMAX – VLDGOFF2 = A VLDGOFF2 – VLDGOFF1 = B GLDG = 20 × ℓog [B/(B – A)]

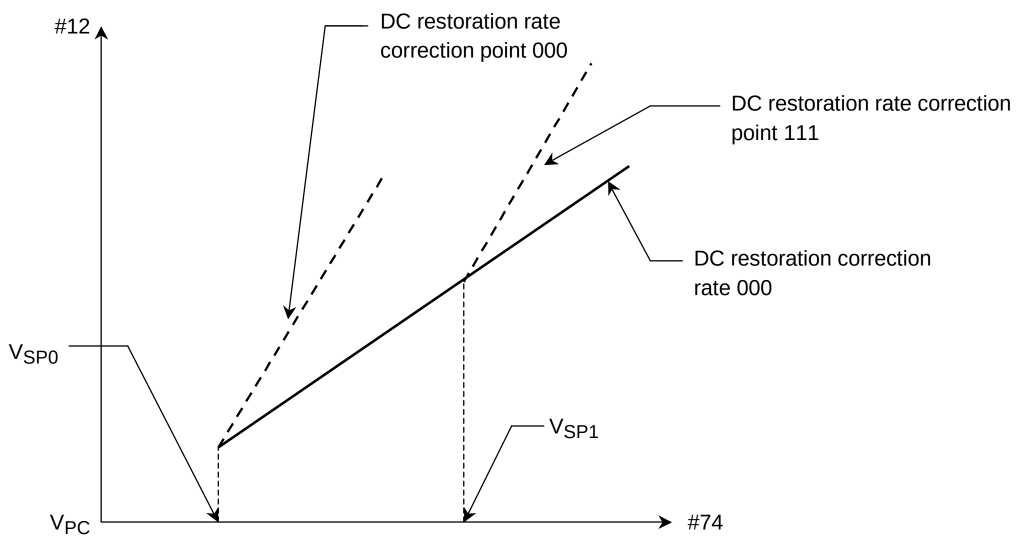


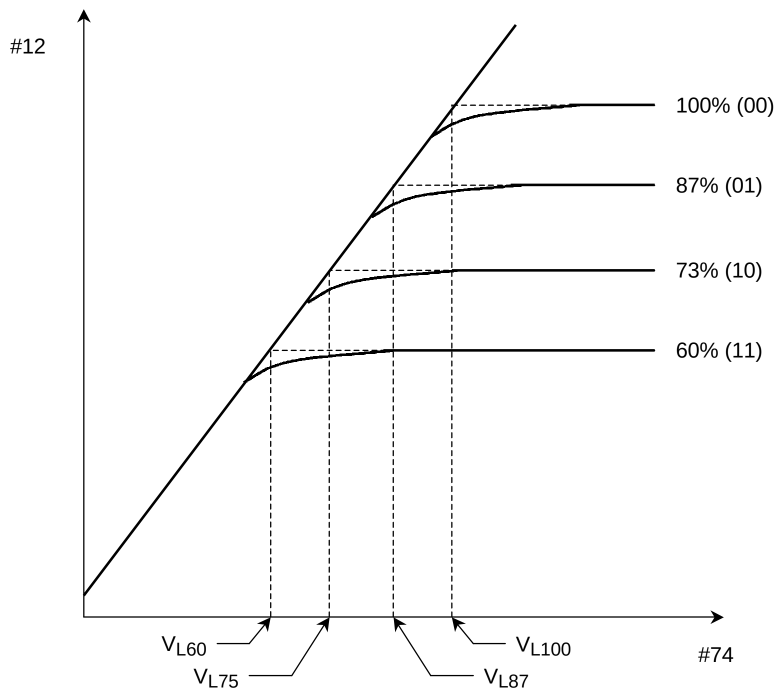
Note No.	Characteristics	Test Conditions SW Mode SW71	 SW70	 SW68	 SW64	 SW74	Test Method (Test condition: V_{CC} = 9 V/2 V, Ta = 25 ± 3°C)
P15	Light area static Yγ gain	B	B	C	A	OPEN	1. Connect external power supply PS1 to #68, external power supply PS2 to TP7, and set PS2 to 0 V. 2. Set dark area static Yγ gain [1C] to 0dB [17], and light area static Yγ gain [1C] to 0dB [17]. 3. Set PS1 to V_{68} [V], and measure #12 picture period voltage VLSGOFF1 [V]. 4. Set PS1 to VLGP [V], and measure #12 picture period voltage VLDGOFF2 [V]. 5. Set light area static Yγ gain [1C] to MAX [14], PS1 to VLGP [V], measure #12 picture period voltage VlSGMAX, and calculate GLASGMAX [dB] using the following equations. VLSGMAX − VLSGOFF2 = A VLSGOFF2 − VLSGOFF1 = B GLSGMAX = 20 × ℓog [B/(B − A)] [dB]  6. Set light area static Yγ gain [1C] to MIN [16], PS1 to VLGP [V], measure #12 picture period voltage VLSGMIN, and calculate GLASGMIN [dB] using the following equations. VLSGMIN − VLSGOFF2 = C VLSGOFF2 − VLSGOFF1 = B GLSGMIN = 20 × ℓog [B/(B − C)] [dB] 

Note No.	Characteristics	Test Conditions SW Mode					Test Method (Test condition: V_{CC} = 9 V/2 V, Ta = 25 ± 3°C)
		SW71	SW70	SW68	SW64	SW74	
P16	Dark area detection sensitivity	A	B	A	A	OPEN	1. Input the signal whose picture period amplitude is 0.18 V to #68 as shown in the figure below. 2. Measure #71 pin voltage DAMIN, DACEN, and DAMAX [V] when dark area detection sensitivity [1D] is set to MIN [00], CEN [04] and MAX [07]. 

Note No.	Characteristics	Test Conditions					Test Method (Test condition: V_{CC} = 9 V/2 V, Ta = 25 ± 3°C)
		SW Mode					
		SW71	SW70	SW68	SW64	SW74	
P17	DC restoration rate correction gain	B	B	C	B	ON	1. Set DC restoration rate correction point to minimum (000), DC restoration rate correction limit point to 80% (11), and connect external power supply PS1 to #68. 2. Monitor DC level of #12 picture period. Set PS1 to V_{68} + 0.7 V, and adjust uncolor so that DC level is + 0.7. 3. Set DC restoration correction rate to minimum (000), and measure V_{DT1} and V_{DT2} of V_{68} [V] and V_{68} + 0.1 V as shown in the figure below. 4. Set #68 to V_{68} + 0.1 V, DC restoration correction rate to maximum (111), and measure V_{DT3}. 5. Set DC restoration correction rate SW to less than 100 % (1), #68 to V_{68} + 0.1 V, DC restoration correction rate to maximum (111), and measure V_{DT4}. 6. Calculate ADT_{100}, ADT_{135}, and ADT_{65} using following equations. $ADT_{100} = (V_{DT2}\ [V] - V_{DT1}\ [V]) \div 0.1\ [V]$ $ADT_{135} = (V_{DT3}\ [V] - V_{DT1}\ [V]) \div 0.1\ [V]$ $ADT_{65} = 1 - ((V_{DT2}\ [V] - V_{DT4}\ [V]) \div 0.1\ [V])$



Note No.	Characteristics	Test Conditions					Test Method (Test condition: V_{CC} = 9 V/2 V, Ta = 25 ± 3°C)
		SW Mode					
		SW71	SW70	SW68	SW64	SW74	
P18	DC restoration rate correction point	B	B	C	B	ON	1. Set DC restoration rate correction point to minimum (000), DC restoration rate correction limit point to 80% (11), and connect external power supply PS1 to #68. 2. Monitor DC level of #12 picture period. Set PS1 to V_{68} + 0.7 V, and adjust unicolor so that DC level is + 1.0. 3. Set DC restoration correction rate to minimum (000), and increase PS1 from V_{68}. Plot relation between #74 (DC voltage) and #12 (voltage in picture period). 4. Set DC restoration correction rate to maximum (111), and increase PS1 from V_{68}. Plot relation between #74 and #12. 5. Set DC restoration correction rate to maximum (111), DC restoration rate correction point (111), and increase PS1 from V_{68}. Plot relation between #74 and #12. 6. Determine V_{DT0}, and V_{DT1} using the following equations. $V_{DT0} = [(V_{SP0} - V_{74})/1\ V] \times 100\%$ $V_{DT1} = [(V_{SP1} - V_{74})/1\ V] \times 100\%$ 

<table>
<tr><th rowspan="3">Note No.</th><th rowspan="3">Characteristics</th><th colspan="5">Test Conditions</th><th rowspan="3">Test Method (Test condition: V_{CC} = 9 V/2 V, Ta = 25 ± 3°C)</th></tr>
<tr><th colspan="5">SW Mode</th></tr>
<tr><th>SW71</th><th>SW70</th><th>SW68</th><th>SW64</th><th>SW74</th></tr>
<tr><td>P19</td><td>DC restoration rate correction limit point</td><td>B</td><td>B</td><td>B</td><td>C</td><td>ON</td><td>1. Set unicolor to maximum (1111111), DC restoration rate correction point to minimum (000), and connect external power supply PS1 to #74.
2. Set DC restoration correction rate to maximum (111).
3. Increase PS from 5 V. Monitor #12, and plot DC restoration correction amount.
4. Repeat the step 3 above by changing data at DC restoration rate correction limit point. Measure the value using the figure below. Calculate P_{DTL60}, P_{DTL75}, P_{DTL87}, and P_{DTL100} using following equations.
$P_{DTL60} = [(V_{L60} - V_{74})/1.0] \times 100\%$
$P_{DTL75} = [(V_{L75} - V_{74})/1.0] \times 100\%$
$P_{DTL87} = [(V_{L87} - V_{74})/1.0] \times 100\%$
$P_{DTL100} = [(V_{L100} - V_{74})/1.0] \times 100\%$

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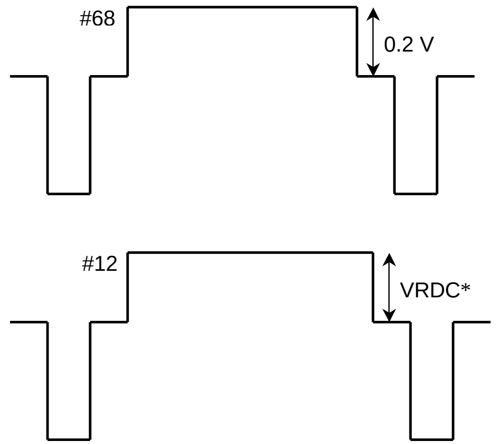
Note No.	Characteristics	Test Conditions SW Mode SW71	SW70	SW68	SW64	SW74	Test Method (Test condition: V_{CC} = 9 V/2 V, Ta = 25 ± 3°C)
P20	DC fluctuation at switching sharpness control peak frequency	B	B	A	B	ON	1. Set unicolor [05] to MAX [7F], SRT gain [19] to MIN [00], and CDE [15] to CEN [80]. Input setup signal (0.2 Vp-p) to TPA as shown in the figure below. 2. Set sharpness [09] to MIN [00] and MAX [80]. Monitor #43, measure DC level VRDCMIN and VRDCMAX [V]. Calculate VRDC [V] using the following equation. VRDC = VRDCMIN − VRDCMAX [V] 

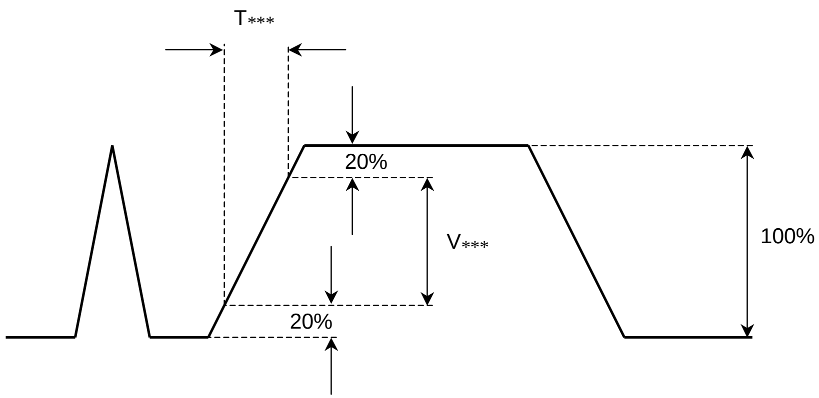
<table>
<tr><th rowspan="3">Note No.</th><th rowspan="3">Characteristics</th><th colspan="5">Test Conditions</th><th rowspan="3">Test Method (Test condition: V_{CC} = 9 V/2 V, Ta = 25 ± 3°C)</th></tr>
<tr><th colspan="5">SW Mode</th></tr>
<tr><th>SW71</th><th>SW70</th><th>SW68</th><th>SW64</th><th>SW74</th></tr>
<tr><td>P21</td><td>Sharpness control range</td><td>B</td><td>B</td><td>A</td><td>B</td><td>ON</td><td>1. Input sine wave to TPA. (The frequency is variable.)
2. Set #68 amplitude to 20 mVp-p.
3. Set unicolor to maximum (1111111), SRT-GAIN to minimum (00000), APACON peak frequency to 13.5 M (00), and color detail enhancer (CDE) to center (10).
4. Set picture mute to OFF (P-MODE: Normal 1, 000), and monitor #12.
5. Set picture sharpness to center (1000000). Set input frequency to 100 kHz, and measure the amplitude V_{100}.
6. Set picture sharpness to maximum (1111111). Set input frequency to F_{AP00}, measure the amplitude V_{MAX00}, and calculate G_{MAX00} using the following equations.
7. Set picture sharpness to minimum (0000000). Set input frequency to F_{AP00}, measure the amplitude V_{MIN00}, and calculate G_{MIN00} using the following equations.
8. Set APACON peak frequency to 9.5 M (01). Set input frequency to F_{AP01}, measure V_{MAX01}/V_{MIN01} and calculate G_{MAX01}/G_{MIN01}.
9. Set APACON peak frequency to 6.4 M (10). Set input frequency to F_{AP10}, measure V_{MAX10}/V_{MIN10} and calculate G_{MAX10}/G_{MIN10}.
10. Set APACON peak frequency to 4.5 M (11). Set input frequency to F_{AP11}, measure V_{MAX11}/V_{MIN11} and calculate G_{MAX11}/G_{MIN11}.
$G_{MAX***} = 20 \times \ell og\ (V_{MAX***} \div V_{100})$ [dB]
$G_{MIN***} = 20 \times \ell og\ (V_{MIN***} \div V_{100})$ [dB]

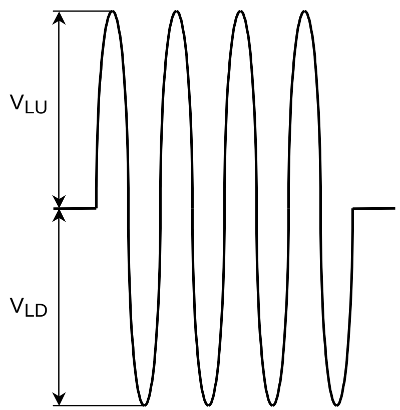
Note: When a spectrum analyzer is used, measure gain for low frequency.</td></tr>
</table>

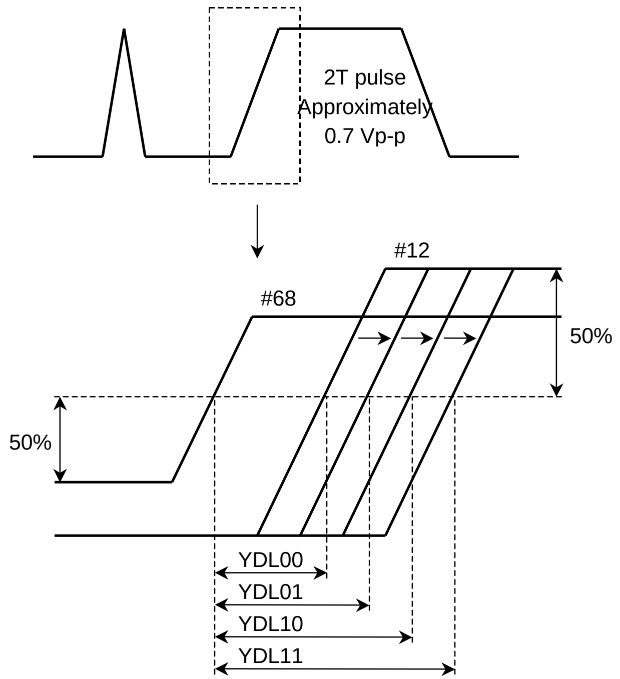
<table>
<tr><th rowspan="3">Note No.</th><th rowspan="3">Characteristics</th><th colspan="5">Test Conditions</th><th rowspan="3">Test Method (Test condition: V_{CC} = 9 V/2 V, Ta = 25 ± 3°C)</th></tr>
<tr><th colspan="5">SW Mode</th></tr>
<tr><th>SW71</th><th>SW70</th><th>SW68</th><th>SW64</th><th>SW74</th></tr>
<tr><td>P22</td><td>Sharpness control center characteristic</td><td>B</td><td>B</td><td>A</td><td>B</td><td>ON</td><td>1. Input sine wave to TPA. (The frequency is variable.)
2. Set the amplitude of #68 to 20 mVp-p.
3. Set unicolor to maximum (1111111), SRT-GAIN to minimum (00000), APACON peak frequency to 13.5 M (00), and color detail enhancer (CDE) to center (10).
4. Set picture mute to OFF (P-MODE: Normal 1, 000), and monitor #12.
5. Set picture sharpness to center (1000000). Set input frequency to 100 kHz, and measure the amplitude V_{100}.
6. Set picture sharpness to center (1000000). Set input frequency to F_{AP00}, measure #12 amplitude V_{CEN00}, and calculate G_{CEN00} using the following equations.
7. Set APACON peak frequency to 9.5 M (01). Set input frequency to F_{AP01}, measure V_{CEN01} and calculate G_{CEN01}.
8. Set APACON peak frequency to 6.4 M (10). Set input frequency to F_{AP10}, measure V_{CEN10} and calculate G_{CEN10}.
9. Set APACON peak frequency to 4.5 M (11). Set input frequency to F_{AP11}, measure V_{CEN11} and calculate G_{CEN11}.
$G_{CEN***} = 20 \times \ell og\ (V_{CEN***} \div V_{100})$ [dB]

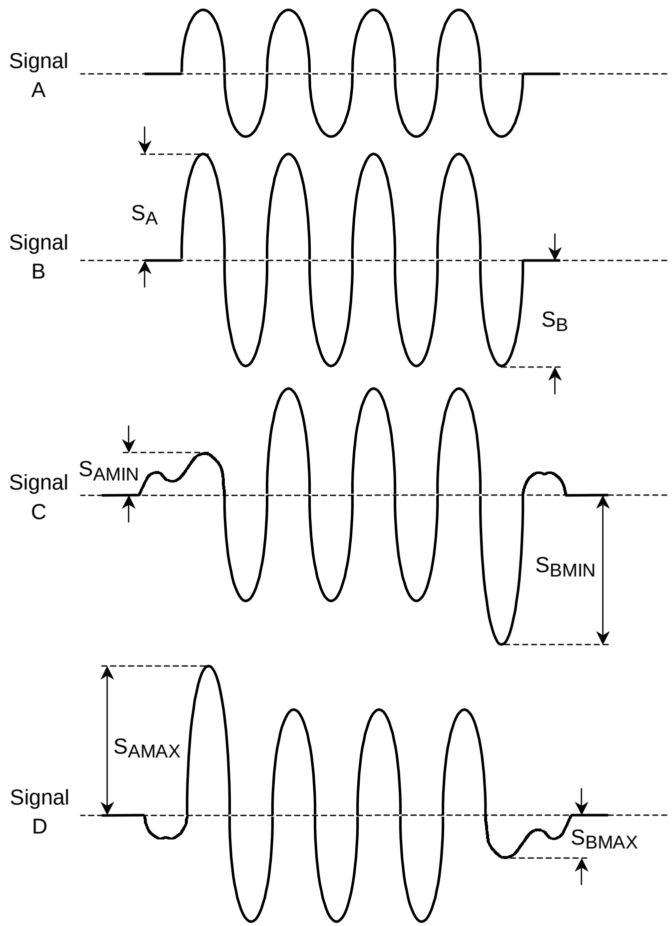
Note: When a spectrum analyzer is used, measure gain for low frequency.</td></tr>
</table>

Note No.	Characteristics	Test Conditions SW Mode SW71	SW70	SW68	SW64	SW74	Test Method (Test condition: V_{CC} = 9 V/2 V, Ta = 25 ± 3°C)
P23	2T pulse response SRT control	B	B	A	B	ON	1. Input 2T pulse (0.7 Vp-p) signal to TPA. Set unicolor to maximum (1111111), SRT-GAIN to minimum (00000), CDE to center (10) picture sharpness control to center (1000000). 2. Set APACON peak frequency to13.5 M (00), and monitor #12. 3. Measure $T_{SRTMIN00}$ and $V_{SRTMIN00}$ as shown in the figure below. 4. Set SRT-GAIN to maximum (11111), and measure $T_{SRTMAX00}$ and $V_{SRTMAX00}$. 5. Set APACON peak frequency to 9.5 M (01). Set SRT-GAIN to minimum (00000) and maximum (11111). Measure $T_{SRTMIN01}/V_{SRTMIN01}$ and $T_{SRTMAX01}/ V_{SRTMAX01}$. 6. Set APACON peak frequency to 6.4 M (10). Set SRT-GAIN to minimum (00000) and maximum (11111). Measure $T_{SRTMIN10}/V_{SRTMIN10}$ and $T_{SRTMAX10}/ V_{SRTMAX10}$. 7. Set APACON peak frequency to 4.5 M (11). Set SRT-GAIN to minimum (00000) and maximum (11111). Measure $T_{SRTMIN11}/V_{SRTMIN11}$ and $T_{SRTMAX11}/V_{SRTMAX11}$. 8. Calculate the following equations. $T_{SRT00} = 20 \times \ell og\ [((V_{SRTMAX00}/T_{SRTMAX00})/(V_{SRTMIN00}/T_{SRTMIN00}))$ $T_{SRT01} = 20 \times \ell og\ [(V_{SRTMAX01}/T_{SRTMAX01})/(V_{SRTMIN01}/T_{SRTMIN01})]$ $T_{SRT10} = 20 \times \ell og\ [(V_{SRTMAX10}/T_{SRTMAX10})/(V_{SRTMIN10}/T_{SRTMIN10})]$ $T_{SRT11} = 20 \times \ell og\ [(V_{SRTMAX11}/T_{SRTMAX11})/(V_{SRTMIN11}/T_{SRTMIN11})]$

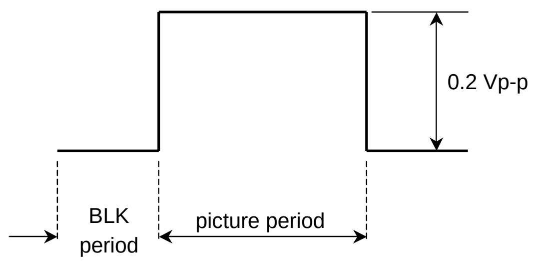


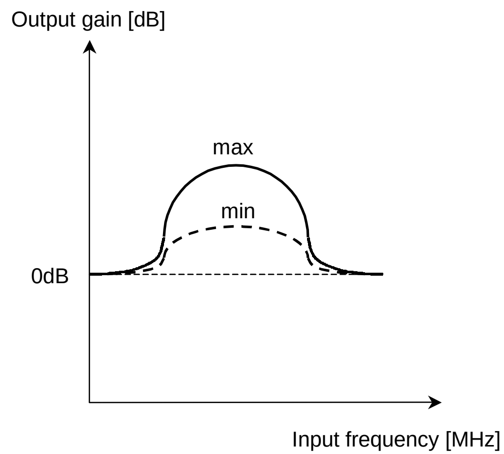
Note No.	Characteristics	Test Conditions SW Mode					Test Method (Test condition: V_{CC} = 9 V/2 V, Ta = 25 ± 3°C)
		SW71	SW70	SW68	SW64	SW74	
P24	VSM gain	B	B	A	B	ON	1. Input sine wave of F_{VSM} frequency to TPA. Set #68 amplitude to 0.02 Vp-p. 2. Turn on SW77 and change VSM gain from minimum (001) to maximum (111). Measure #77 amplitude, V_{001}, V_{011}, V_{100}, V_{101}, V_{110}, and V_{111}. Set input amplitude to 0.7 Vp-p, and VSM gain to OFF (000). Measure TP77 amplitude V_{000}. 3. Calculate the following equations. $G_{V000} = 20 \times \ell og\ (V_{000}/0.7)$ [dB] $G_{V001} = 20 \times \ell og\ (V_{001}/0.02)$ [dB] $G_{V010} = 20 \times \ell og\ (V_{010}/0.02)$ [dB] $G_{V011} = 20 \times \ell og\ (V_{011}/0.02)$ [dB] $G_{V100} = 20 \times \ell og\ (V_{100}/0.02)$ [dB] $G_{V101} = 20 \times \ell og\ (V_{101}/0.02)$ [dB] $G_{V110} = 20 \times \ell og\ (V_{110}/0.02)$ [dB] $G_{V111} = 20 \times \ell og\ (V_{111}/0.02)$ [dB]
P25	VSM limit	B	B	B	A	ON	1. Input sine wave of frequency F_{VSM} to TPA. 2. Set VSM gain to 111, and #68 amplitude to 0.7 Vp-p. 3. Turn on SW77 and measure TP77 amplitude V_{LU} and V_{LD} [Vp-p] as shown in the figure below. 

Note No.	Characteristics	Test Conditions					Test Method (Test condition: V_{CC} = 9 V/2 V, Ta = 25 ± 3°C)
		SW Mode					
		SW71	SW70	SW68	SW64	SW74	
P26	Y delay time switching	B	B	A	B	ON	1. Set unicolor to maximum (1111111), SRT-GAIN to minimum (00000), and input 2T pulse signal (approximately 0.7 V (p-p)) to TPA. 2. Set picture sharpness to center (1000000). 3. Monitor #68 and #12 as shown in the figure below. Measure YDL00 that is the time difference between signals #68 and #12. 4. Set Y/C-DL1 to +5 ns (1), and measure YDL01 as shown in the figure below. 5. Set Y/C-DL1 to 0 ns (0), Y/C-DL2 to +10 ns (1) and measure YDL10 as shown in the figure below. 6. Set Y/C-DL1 to +5 ns (1), Y/C-DL2 to +10 ns (1) and measure YDL11 as shown in the figure below. 7. Determine YDLA, YDLB, and YDLC using the following equations. YDLA = YDL01 – YDL00 YDLB = YDL10 – YDL00 YDLC = YDL11 – YDL00 

Note No.	Characteristics	Test Conditions					Test Method (Test condition: V_{CC} = 9 V/2 V, Ta = 25 ± 3°C)
		SW Mode					
		SW71	SW70	SW68	SW64	SW74	
P27	Y group delay correction	B	B	A	B	ON	1. Input Multi Burst signal (4.2-MHz frequency, 0.1 Vp-p at #68) of A signal in TPA. Set unicolor to maximum (1111111), SRT-GAIN to minimum (00000), and Color detail enhancer (CDE) to minimum (00000). 2. Set sharpness to flat (DEC [30]), APACON peak frequency to 4.5 M (11), and monitor #12. 3. Sine wave signal A input becomes like signal B on #12 as shown in the figure on the right. Measure S_A and S_B. 4. When group delay correction is set to minimum (0000), signal A becomes like signal C on #12. Measure S_{AMIN} and S_{BMIN}. 5. When group delay correction is set to maximum (1111), signal A becomes like signal D on #12. Measure S_{AMAX} and S_{BMAX}. 6. Calculate the following equations. $G_{AMIN} = 20 \times \ell og\ (S_{AMIN}/S_A)$ [dB] $G_{BMIN} = 20 \times \ell og\ (S_{BMIN}/S_B)$ [dB] $G_{AMAX} = 20 \times \ell og\ (S_{AMAX}/S_A)$ [dB] $G_{BMAX} = 20 \times \ell og\ (S_{BMAX}/S_B)$ [dB]  Note: Sine wave input starts and ends within the picture period such as a burst signal. The wave is not continuous.

Note No.	Characteristics	Test Conditions					Test Method (Test condition: V_{CC} = 9 V/2 V, Ta = 25 ± 3°C)
		SW Mode					
		SW71	SW70	SW68	SW64	SW74	
P28	Color detail enhancer (CDE)	B	B	A	B	ON	1. Set unicolor to maximum (1111111), SRT-GAIN to minimum (00000), color to center (1000000), and color limiter level to 2 Vp (1). Input SWEEP signal to TPA so that #68 amplitude is 20 mVp-p. Set SW67 to A, and input signal as shown in the figure below (#67 amplitude is 0.2 Vp-p) to TP67. 2. Set picture sharpness to center (1000000), Y detail control to center (1000), and monitor #14 with a spectrum analyzer. 3. When CDE is at minimum (00), set low frequency area to 0dB, and determine peak level G_{CDEMIN}. 4. When CDE is at maximum (11), set low frequency area to 0dB, and determine peak level G_{CDEMAX}. 5. Calculate the following equation. $G_{CDE00} = G_{CDEMAX00} - G_{CDEMIN00}$ 6. When APACON peak frequency is 13.5 M (00), 9.5 M (01), 6.4 M (10), and 4.5 M (11), calculate G_{CDE00}, G_{CDE01}, G_{CDE10}, and G_{CDE11} respectively using above equation.



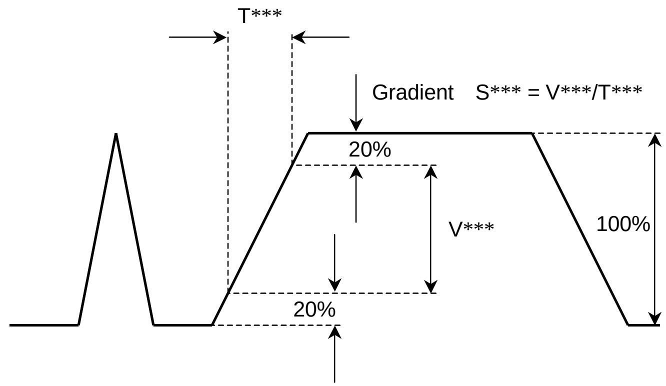


Note No.	Characteristics	Test Conditions SW Mode					Test Method (Test condition: V_{CC} = 9 V/2 V, Ta = 25 ± 3°C)
		SW71	SW70	SW68	SW64	SW74	
P29	Y detail control range	B	B	A	B	ON	1. Set unicolor to maximum (1111111), SRT-GAIN to minimum (00000), CDE to center (10), and APACON peak frequency to 4.5 M (11). Input SWEEP signal to TPA. 2. Set #68 amplitude to 20mVp-p. 3. Set picture sharpness to center (1000000), Y detail control to maximum (1111), and monitor #12 with a spectrum analyzer. 4. Set low frequency area to 0dB, and measure each peak level G_{YDMAX}. 5. Set Y detail control to center (1000), and measure peak level G_{YDCEN}. 6. Set Y detail control to minimum (0000), and measure peak level G_{YDMIN}.

Test Conditions for Color Difference Block 1: YUV input and matrix

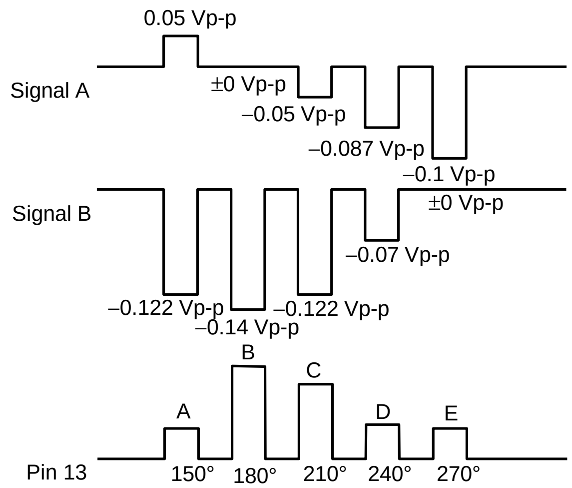
Common Test Condition for Color Difference Block 1: YUV input and matrix

1. SW71 = B, SW70 = B, SW44 = ON, SW18 to SW26 = A, SW77 = OPEN, SW74 = OPEN
2. Transfer BUS control data with preset values.
3. Turn ACB operation switching to ACB OFF (0), and turn high blight color OFF (0).
4. Input sync signal [must be sync with input signal for testing except Sweep.] to #53 (sync input), and set SYNC-IN-SW to 1.

Note No.	Characteristics	Test Conditions SW Mode				Test Method (Test condition: V_{CC} = 9 V/2 V, Ta = 25 ± 3°C)
		SW68	SW67	SW66	SW64	
S01	Color SRT gain	C	A	A	B	1. Set Y mute ON (P-MODE: Y-MUTE, 001), brightness to center (10000000), color to center (1000000), unicolor to maximum (1111111). 2. Input 2T pulse signal to TP67 so that #67 amplitude is 423 mVp-p. 3. Monitor #14 output waveform. When color SRT peak frequency is 4.5 MHz (0), measure gradients of color SRT gain for minimum (00), center (10), and maximum (11) that are SB00MIN, SB00CEN, and SB00MAX as shown in the figure below. Set SB00MIN to 0dB, calculate $GS_{B00CEN} = 20 \times \ell og$ (SB00CEN/SB00MIN) and $GS_{B00MAX} = 20 \times \ell og$ (SB00MAX/SSB00MIN). 4. When color SRT peak is 5.8 MHz (1), measure gradients of color SRT gain for minimum (00), center (10), and maximum (11). Calculate $G_{SB01CEN}$ and $G_{SB01MAX}$. 5. Input 2T pulse signal to TP66 so that #66 amplitude is 300 mVp-p. 6. Monitor #12 output waveform. When color SRT peak frequency is 4.5 MHz (0), measure gradients of color SRT gain for minimum (00), center (10), and maximum (11) that are SR00MIN, S_{R00CEN}, and S_{R00MAX} as shown in the figure below. Set SR00MIN to 0dB, calculate GSB00CEN = $20 \times \ell og$ (SB00CEN/SB00MIN) and GSB00MAX = $20 \times \ell og$ (SB00MAX/SSB00MIN). 7. When color SRT peak is 5.8 MHz (1), measure gradients of color SRT gain for minimum (00), center (10), and maximum (11). Calculate $G_{SR01CEN}$ and $G_{SR01MAX}$. 
		SW63	SW61	SW60	—	
		B	B	B	—	

<table>
<tr><th rowspan="3">Note No.</th><th rowspan="3">Characteristics</th><th colspan="4">Test Conditions</th><th rowspan="3">Test Method (Test condition: V_{CC} = 9 V/2 V, Ta = 25 ± 3°C)</th></tr>
<tr><th colspan="4">SW Mode</th></tr>
<tr><th>SW68</th><th>SW67</th><th>SW66</th><th>SW64</th></tr>
<tr><td rowspan="3">S02</td><td rowspan="3">Dynamic Y/C compensation</td><td>C</td><td>A</td><td>A</td><td>B</td><td rowspan="3">1. Input 100-kHz sync signal to TP67, and set #67 amplitude to 0.2 Vp-p.
2. Set Y mute OFF (P-MODE: Normal 1, 000), brightness to center (1000000), color to center (1000000), unicolor to maximum (1111111), and Y/C Gain Comp to minimum (00). Set black stretch point 1 to OFF (000), dark area static Yγ gain to minimum (00), light area static Yγ gain to maximum (11), and SW1 to B. Apply 5.16 V to #68 from external power supply PS1.
3. Monitor #14 output waveform, and measure amplitude VBDY0.
4. Set Y/C Gain Comp to maximum (11). Set SW1 to B. Set black stretch point 1 to OFF (000), dark area static Yγ gain to maximum (11), light area static Yγ gain to maximum (00), and monitor #14 amplitude VBDY1.
5. Set Y/C Gain Comp to maximum (11). Switch SW1 to A, and TPI to GND. Set black stretch point 1 to maximum (111), dark area static Yγ gain to minimum (00), bright area static Yγ gain to maximum (11), and monitor #14 amplitude VBDY2.
6. Calculate the following equations.
$GC_{BDY1} = 20 \times \ell og$ (VBDY1/VBDY0), $GC_{BDY2} = 20 \times \ell og$ (VBDY2/VBDY0)
7. Input 100-kHz sync signal to TP5, and repeat the procedure above. Calculate the following equations.
$GC_{RDY1} = 20 \times \ell og$ (VRDY1/VRDY0), $GC_{RDY2} = 20 \times \ell og$ (VRDY2/VBDY0)</td></tr>
<tr><td>SW63</td><td>SW61</td><td>SW60</td><td>SW74</td></tr>
<tr><td>B</td><td>B</td><td>B</td><td>OPEN</td></tr>
</table>

Note No.	Characteristics	Test Conditions SW Mode				Test Method (Test condition: V_{CC} = 9 V/2 V, Ta = 25 ± 3°C)
		SW68	SW67	SW66	SW64	
S03	YUV gain	A/C	A/B	A/B	B	1. Set picture mute to OFF (P-MODE: Normal 1, 000), brightness to maximum (11111111), color to center (1000000), and unicolor to maximum (1111111). 2. Set SW68 to A. Set SW67 and SW66 to B, and input 100-kHz sine wave to TPA. Set #68 amplitude to 0.2 Vp-p. 3. Set SW74 open. Measure #74 amplitude VY00 and VY01 when Y/color difference input mode is set to Y/Cb/Cr (0) and Y/Pb/Pr (1). 4. Set SW68 to C, SW67 to A, and SW66 to B. Input 100-kHz sine wave to TP67, and set #67 amplitude to 0.2 Vp-p. 5. Measure #14 amplitude VB00 when Y/color difference input mode is set to Y/Cb/Cr (0). 6. Measure #14 and #12 amplitude VBB01 and VBR01 when Y/color difference input mode is set to Y/Pb/Pr (1). 7. Set SW68 to C, SW67 to B, and SW66 to A. Input 100-kHz sine wave to TP66, and set #66 amplitude to 0.2 Vp-p. 8. Measure #12 amplitude VR00 when Y/color difference input mode is set to Y/Cb/Cr (0). 9. Measure #14 and #12 amplitude VRB01 and VRR01 when Y/color difference input mode is set to Y/Pb/Pr (1). 10. Calculate the following equations. $G_{Y00} = 20 \times \ell og\ (VY00/0.2)$, $G_{Y01} = 20 \times \ell og\ (VY01/0.2)$ $G_{CBB} = 20 \times \ell og\ (VB00/0.2)$, $G_{PBB} = 20 \times \ell og\ (VBB01/0.2)$, $G_{PBR} = 20 \times \ell og\ (VBR01/0.2)$ $G_{CRR} = 20 \times \ell og\ (VR00/02)$, $G_{PRB} = 20 \times \ell og\ (VRB01/0.2)$, $G_{PRR} = 20 \times \ell og\ (VRR01/0.2)$
		SW8	SW9	SW10	SW56	
		B	B	B	OPEN	

Note No.	Characteristics	Test Conditions SW Mode				Test Method (Test condition: V_{CC} = 9 V/2 V, Ta = 25 ± 3°C)
		SW68	SW67	SW66	SW64	
S04	Green stretch	C	A	A	—	1. Input signal B as shown in the figure below from TP67 (Cb/Pb1 input), and signal A from TP66 (Cr/Pr input). 2. Set brightness [06] to maximum (FF). 3. Measure amplitudes A, B, C, D, and E at #13 (Gout) as shown in the figure below. (A00 to E00) 4. Set green stretch [14] data to (08), and repeat the step 3 above. (A01 to E01) 5. Set green stretch [14] data to (10), and repeat the step 3 above. (A10 to E10) 6. Set green stretch [14] data to (18), and repeat the step 3 above. (A11 to E11) 7. Green stretch gain is calculated by the following equations $GrA01=\frac{A01}{A00}$ $GrA10=\frac{A10}{A00}$ $GrA11=\frac{A11}{A00}$ $GrB01=\frac{B01}{B00}$ $GrB10=\frac{B10}{B00}$ $GrB11=\frac{B11}{B00}$ $GrC01=\frac{C01}{C00}$ $GrC10=\frac{C10}{C00}$ $GrC11=\frac{C11}{C00}$ $GrD01=\frac{D01}{D00}$ $GrD10=\frac{D10}{D00}$ $GrD11=\frac{D11}{D00}$ $GrE01=\frac{E01}{E00}$ $GrE10=\frac{E10}{E00}$ $GrE11=\frac{E11}{E00}$ 
		SW26	SW25	SW24	SW21	
		A	A	A	A	
		SW19	SW18	—	—	
		A	A	—	—	

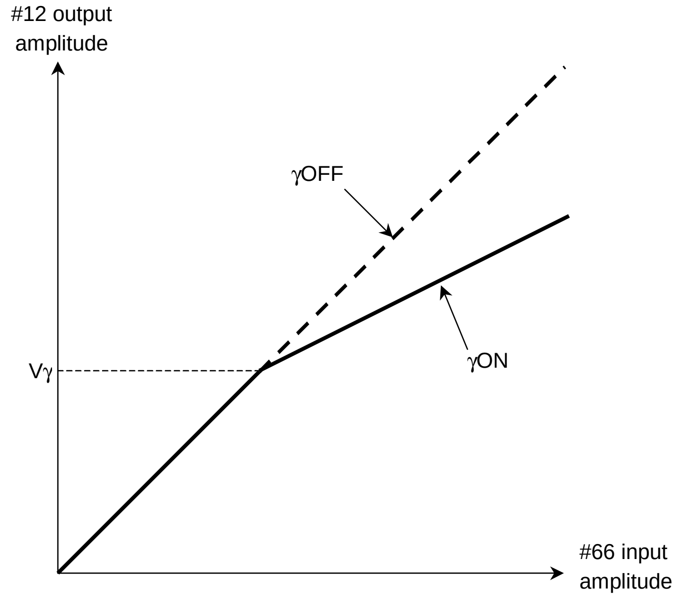
Test Conditions for Color Difference Block 2

Common Test Conditions for Color Difference Block 2

1. SW71 = B, SW70 = B, SW61 to SW63 = B, SW44 = ON, SW40 = B
2. Unless otherwise specified, measure each bus data with preset values.
3. Set the following data.
   Subaddress (00) Data (02)
   Subaddress (02) Data (0C)
   Subaddress (05) Data (7F)
   Subaddress (06) Data (6C)
   Subaddress (07) Data (40)
   Subaddress (0B) Data (7F)
   Subaddress (0C) Data (84)
   Subaddress (12) Data (F0)
   Subaddress (13) Data (F0)
   Subaddress (15) Data (00)
   Subaddress (18) Data (00)
   Subaddress (1A) Data (C0)
   Subaddress (1B) Data (E0)
   Subaddress (1C) Data (03)
   Subaddress (1D) Data (78)

Note No.	Characteristics	Test Conditions									Test Method
		SW Mode									
		SW68	SW67	SW66	SW26	SW25	SW24	SW21	SW19	SW18	
A01	Color difference contrast adjustment characteristic	C	A or B	A or B	A	A	A	A	A	A	1. Set brightness to maximum, and subaddress (12) data to (F0). 2. Input signal 3 (f_0 = 100 kHz, picture period amplitude = 0.23 Vp-p) from pin 66. 3. Change unicolor data to maximum (7F), center (40), and minimum (00), and measure pin 12 picture period amplitude V_{uCYMAX}, V_{uCYCNT}, and V_{uCYMIN} respectively. 4. Determine unicolor amplitude ratio between maximum and minimum in decibels. (ΔV_{uCY}) 5. Repeat the steps 2 to 4 above with the following pins: Input (picture period amplitude 0.2 Vp-p) from pin 67, and measure pin 14.

Note No.	Characteristics	Test Conditions SW Mode SW68	SW67	SW66	SW26	SW25	SW24	SW21	SW19	SW18	Test Method
A02	Color adjustment characteristic	C	A or B	A or B	A	A	A	A	A	A	1. Set brightness to maximum, and subaddress (12) data to (F0). 2. Input signal 3 (f_0 = 100 kHz, picture period amplitude = 0.115 Vp-p) from pin 66. 3. Change color data to maximum (7F), center (40), and minimum (01), and measure pin 12 picture period amplitudes V_{CCYMAX}、V_{CCYCNT}, and V_{CCYMIN} respectively. 4. Calculate amplitude ratios of maximum and minimum against color center in decibels. (ΔV_{CCY}) 5. Repeat the steps 2 to 4 above with the following pins: Input (picture period amplitude 0.1Vp-p) from pin 67 and measure pin 14.
A03	Color difference halftone characteristic	C	A or B	A or B	A	A	A	A	A	A	1. Input signal 3 (f_0 = 100 kHz, picture period amplitude 0.2 Vp-p) from pin 66. 2. Measure pin 12 output picture period amplitude vHTARY. 3. Apply 1.5 V to pin 79 from external power supply. 4. Measure pin 12 output picture period amplitude vHTBRY. 5. Calculate GHT_{RY} = vHTBRY/vHTARY 6. Repeat the steps 1 to 5 above and measure pin 13. Calculate GHT_{GY} = vHTBGY/vHTAGY 7. Repeat the steps 1 to 5 above and measure pin 67. Calculate GHT_{BY} = vHTBBY/vHTABY.

Note No.	Characteristics	Test Conditions SW Mode									Test Method
		SW68	SW67	SW66	SW26	SW25	SW24	SW21	SW19	SW18	
A04	Color γ characteristic	C	B	A	A	A	A	A	A	A	1. Input signal 2 from pin 66. 2. Increase signal 2 amplitude A. Determine gamma correction point Vγ1, Vγ2, and Vγ3 of subaddress data (14). Set subaddress (14) data as follows: (01) – γOFF (03) –γ1ON (05) –γ2ON (07) –γ3ON Measure #12 output signal amplitude levels and chart a characteristic diagram. 3. Determine Vγ where γ starts applying and gradient Δ at γ ON when linearity at γ OFF is 1. 

Note No.	Characteristics	Test Conditions SW Mode SW68	SW67	SW66	SW26	SW25	SW24	SW21	SW19	SW18	Test Method
A05	Color limiter characteristic	C	B	A	A	A	A	A	A	A	1. Input signal 2 (picture period amplitude = 0.56 Vp-p) from pin 67. 2. Set subaddress (14) to (00)/(01), and measure pin 12 output signal picture period amplitude, CLT_0/CLT_1.
A06	High-bright color gain	C	B	A	A	A	A	A	A	A	1. Input signal 2 (picture period amplitude = 0.28 Vp-p) from pin 67. 2. Adjust color so that pin 14 output picture period amplitude is 1.2 Vp-p. 3. Set subaddress (0B) data to (80) and measure pin 14 output signal picture period amplitude v_{14}. 4. Calculate the following equation. $HBC_1 = (1.2 - v_{14})/1.2$

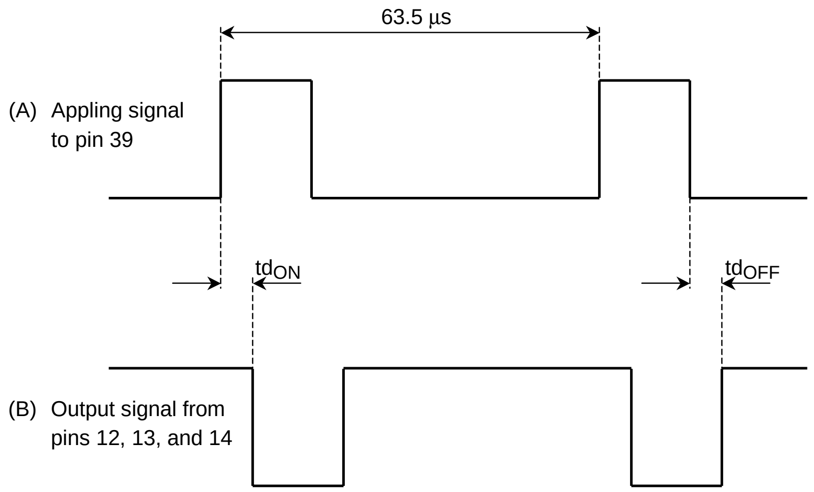
Test Conditions for Text Block

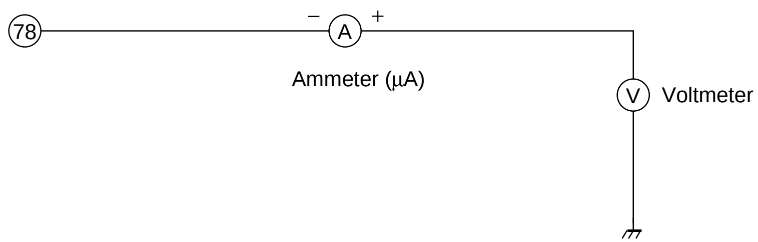
Common Test Conditions for Text Block

1. SW71 = B, SW70 = B, SW60 to SW64 = B, SW44 = ON, SW40 = B
2. Unless otherwise specified, measure each bus data with preset values.
3. Set the following data.
   Subaddress (00) Data (02)
   Subaddress (02) Data (0C)
   Subaddress (05) Data (7F)
   Subaddress (06) Data (6C)
   Subaddress (07) Data (40)
   Subaddress (0B) Data (7F)
   Subaddress (0C) Data (84)
   Subaddress (12) Data (F0)
   Subaddress (13) Data (F0)
   Subaddress (15) Data (00)
   Subaddress (18) Data (00)
   Subaddress (1A) Data (C0)
   Subaddress (1B) Data (E0)
   Subaddress (1C) Data (03)
   Subaddress (1D) Data (78)

Note No.	Characteristics	Test Conditions									Test Method
		SW Mode									
		SW68	SW67	SW66	SW26	SW25	SW24	SW21	SW19	SW18	
T01	AC gain	A	B	B	A	A	A	A	A	A	1. Input signal 1 (f_0 = 100 kHz, picture period amplitude = 0.2 Vp-p) from pin 68. 2. Measure pins 12, 13, and 14 picture period amplitude, V_{12}, V_{13}, and V_{14}. 3. Calculate AC gain using the following equations. $G_R = V_{12}/0.2$ $G_G = V_{13}/0.2$ $G_B = V_{14}/0.2$
T02	Unicolor adjustment characteristic	A	B	B	A	A	A	A	A	A	1. Input signal 1 (f_0 = 100 kHz, picture period amplitude = 0.2 Vp-p) from pin 68. 2. Change unicolor data to maximum (7F), center (40), and minimum (00) and measure pin 12 picture period amplitude, V_{uMAX}, V_{uCNT}, and V_{uMIN} respectively. 3. Calculate amplitude ratio of V_{uMAX} and V_{uMIN} in decibels (ΔV_u)
T03	Brightness adjustment characteristic	A	B	B	A	A	A	A	A	A	1. Input signal 2 from pin 68 and adjust pin 12 picture period output amplitude to 1 Vp-p. 2. Change brightness data to maximum (7F), center (80), and minimum (00) and measure pin 12 voltages, V_{brMAX}, V_{brCNT}, and V_{brMIN} respectively.

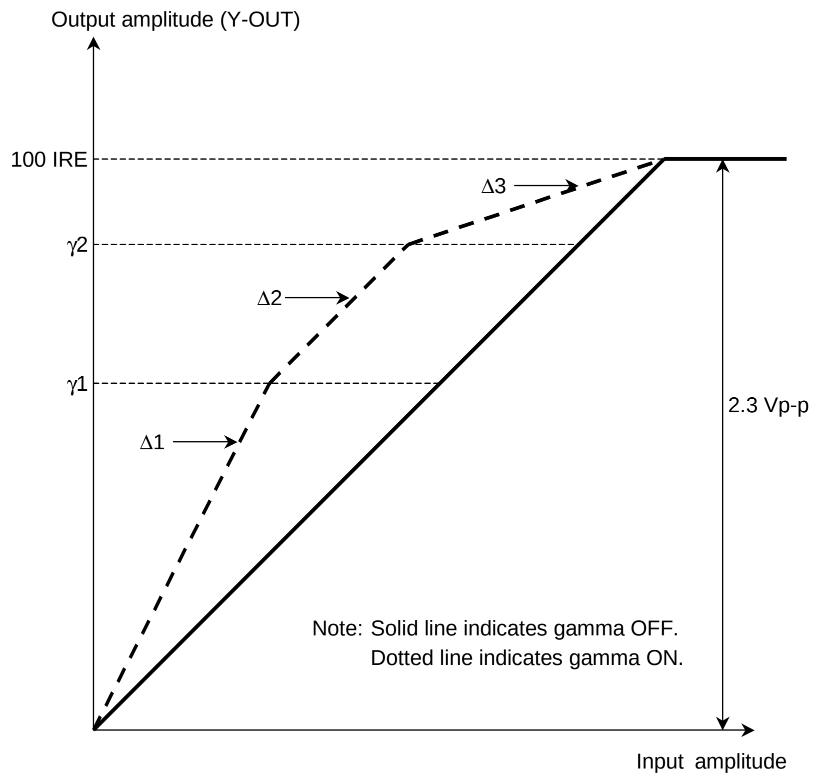
Note No.	Characteristics	Test Conditions SW Mode SW68	SW67	SW66	SW26	SW25	SW24	SW21	SW19	SW18	Test Method
T04	White peak slice level	C	B	B	A	A	A	A	A	A	1. Set subcontrast to maximum. 2. Apply external power supply to pin 68 and gradually increase voltage from 5.8 V. 3. When picture period of pin 12 is clipped, measure pin 12 picture period amplitude voltage, V_{wps1}. 4. Change subaddress (0C) data to (FC) and repeat the steps 1 to 3 above. (V_{wps2})
T05	Black peak slice level	C	B	B	A	A	A	A	A	A	1. Apply external power supply to pin 68 and gradually decrease voltage from 5.8 V. 2. When picture periods are clipped, measure pins 14, 13, and 12 voltage, V_{bps}.
T06	RGB output S/N	C	B	B	A	A	A	A	A	A	1. Adjust brightness data so that picture period voltage of pin 14 is 2.4 V. 2. Set color data to minimum. 3. Measure noise levels n14-, n13-, and n12-Vp-p in picture period of pin 14, 13, and 12 with an oscilloscope. 4. Calculate S/N. $N_{14} = -20 \times \ell og\ [2.3/(0.2 \times n14)]$ $N_{13} = -20 \times \ell og\ [2.3/(0.2 \times n13)]$ $N_{12} = -20 \times \ell og\ [2.3/(0.2 \times n12)]$
T07	Halftone characteristic	A	B	B	A	A	A	A	A	A	1. Input signal 1 (f_0 = 100 kHz, picture period amplitude 0.2 Vp-p) from pin 68. 2. Measure pin 14 picture period amplitude v14A. 3. Apply 1.5 V to pin 79 from external power supply. 4. Measure pin 14 picture period amplitude v14B 5. Calculate the following equation. G_{HT1} = v14B/v14A 6. Stop applying voltage to pin 79. Set subaddress (1A) to data (E2) and measure pin 14-picture period amplitude, v14C. 7. Calculate the following equation. G_{HT2} = v414C/v14A

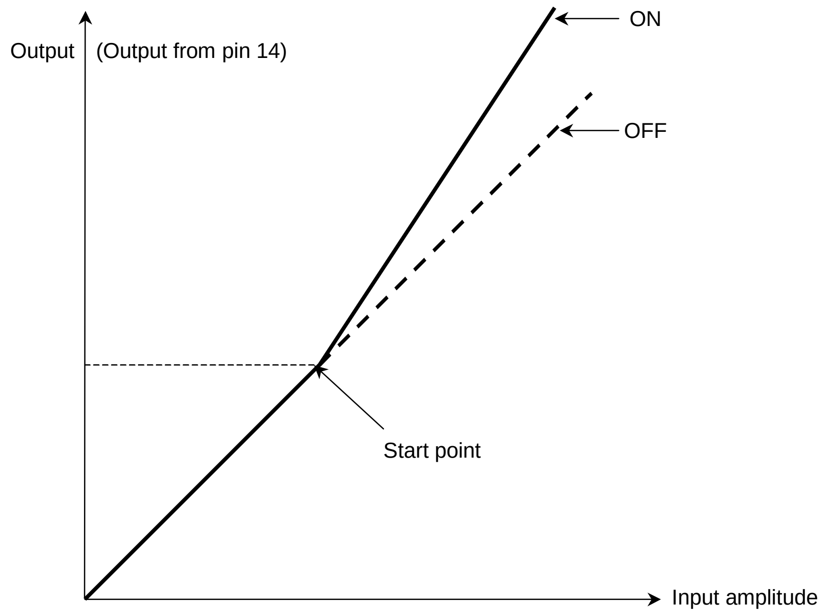
Note No.	Characteristics	Test Conditions									Test Method
		SW Mode									
		SW68	SW67	SW66	SW26	SW25	SW24	SW21	SW19	SW18	
T08	BLK pulse delay time	C	B	B	A	A	A	A	A	A	1. Apply signal shown in the figure (A) below to pin 39 (BLK input), and measure td_{ON} and td_{OFF} of output signals from pins 12, 13, and 14 shown in the figure (B) below. 

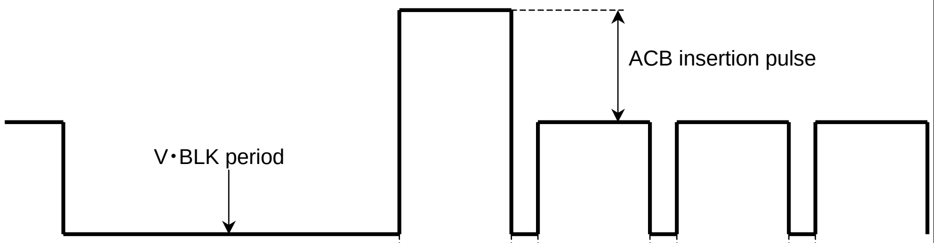
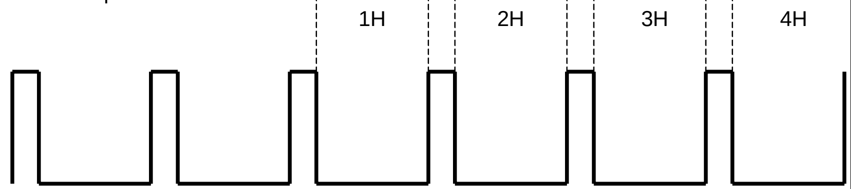
Note No.	Characteristics	Test Conditions									Test Method
		SW Mode									
		SW68	SW67	SW66	SW26	SW25	SW24	SW21	SW19	SW18	
T09	Drive adjustment variable range	A	B	B	A	A	A	A	A	A	1. Input signal 1 (f_0 = 100 kHz, picture period amplitude 0.2 Vp-p) from pin 68. 2. Measure picture period amplitude of pin 13 when subaddress (0D) data is changed to maximum (FE), center (80), and minimum (00). 3. Use picture period amplitude at center as the base. Determine amplitude ratio DR_{G1+} and DR_{G1-} at maximum and minimum in decibels. 4. Repeat the steps 1 to 3 above to measure amplitude ratio of pin 14, DR_{B1+} and DR_{B1-} in decibels when subaddress (0E) data is changed. 5. Repeat the steps 1 to 3 above to measure amplitude ratio of pin 13, DR_{G2+} and DR_{G2-} in decibels when subaddress (0E) center data is set to (81) used as the base. 6. Repeat the steps 1 to 3 above to measure picture period amplitude ratio of pin 14, DR_{B2+} and DR_{B2-} in decibels when subaddress (0E) data is changed to maximum (FF), center (81), and minimum (01). 7. Repeat the steps 1 to 3 above to measure picture period amplitude ratio of pin 12, DR_{R1+} and DR_{R2-} in decibels when subaddress (0D) data is changed to maximum (FF), center (81), and minimum (01). 8. Repeat the steps 1 to 3 above to measure picture period amplitude ratio of pin 14, DR_{B3+} and DR_{B3-} in decibels when subaddress (0D) data is set to (81), and subaddress (0E) data is changed. 9. Repeat the steps 1 to 3 above to measure picture period amplitude ratio of pin 13, DR_{G3+} and DR_{G3-} in decibels when subaddress (0E) data is set to (81), and subaddress (0D) data is changed to maximum (FF), center (81), and minimum (01). 10. Repeat the steps 1 to 3 above to measure picture period amplitude ratio of pin 12, DR_{R2+} and DR_{R2-} in decibels when subaddress (0D) data is set to (81), and subaddress (0E) data is changed to maximum (FF), center (81), and minimum (01).
T10	#78 input impedance	C	B	B	A	A	A	A	A	A	1. Connect external power supply, an ammeter, and a voltmeter to pin 78. Adjust voltage so that current value is set to zero. 2. Measure the current when voltage of pin 78 is increased by 0.2V. (I_{in}) 3. Calculate the following equation. $\mathbf{Z}_{in53} = 0.2\ V/I_{in}\ (\Omega)$ 

Note No.	Characteristics	Test Conditions SW Mode SW68	SW67	SW66	SW26	SW25	SW24	SW21	SW19	SW18	Test Method
T11	ACL characteristic	A	B	B	A	A	A	A	A	A	1. Input signal 1 (f_0 = 100 kHz, picture period amplitude 0.2 Vp-p) from pin 68. 2. Measure pin 12 picture period amplitude, vACL1. 3. Apply "DC voltage of pin 78 – 0.8 V" to pin 78 from external power supply and measure pin 12-picture period amplitude, vACL2. 4. Apply "DC voltage of pin 78 – 1.3 V" to pin 78 from external power supply and measure pin 12-picture period amplitude, vACL3. 5. Calculate the following equations. $ACL_1 = -20 \times \ell og$ (vACL2/vACL1) $ACL_2 = -20 \times \ell og$ (vACL3/vACL1)
T12	ABL point	C	B	B	A	A	A	A	A	A	1. Measure DC voltage of pin 78, VABL1. 2. Set subaddress (1B) data to (1C). 3. Apply external voltage to pin 78, and decrease voltage from 6.5 V. When voltage of pin 12 starts changing, measure pin 78 voltage, VABL2. 4. Change subaddress (1B) data to (3C), (5C), (7C), (9C), (BC), (DC), and (FC) under the status of the step 3 above. Measure pin 78 voltage: VABL3, VABL4, VABL5, VABL6, VABL7, VABL8, and VABL9. 5. ABL_{P1} = VABL2 – VABL1 ABL_{P5} = VABL6 – VABL1 ABL_{P2} = VABL3 – VABL1 ABL_{P6} = VABL7 – VABL1 ABL_{P3} = VABL4 – VABL1 ABL_{P7} = VABL8 – VABL1 ABL_{P4} = VABL5 – VABL1 ABL_{P8} = VABL9 – VABL1

<table>
<tr><th rowspan="3">Note No.</th><th rowspan="3">Characteristics</th><th colspan="9">Test Conditions
SW Mode</th><th rowspan="3">Test Method</th></tr>
<tr></tr>
<tr><th>SW68</th><th>SW67</th><th>SW66</th><th>SW26</th><th>SW25</th><th>SW24</th><th>SW21</th><th>SW19</th><th>SW18</th></tr>
<tr><td>T13</td><td>ABL gain</td><td>C</td><td>B</td><td>B</td><td>A</td><td>A</td><td>A</td><td>A</td><td>A</td><td>A</td><td>1. Apply 6.5-V external voltage to pin 78.
2. Set subaddress (1B) data to (00).
3. Set brightness data to maximum.
4. Apply 4.5-V external voltage to pin 78.
5. Change subaddress (1B) data to (00), (04), (08), (0C), (10), (14), (18), and (1C). Repeat the step 3 above, and measure VABL11, VABL12, VABL13, VABL14, VABL15, VABL16, VABL17, and VABL18.
6. ABL_{G1} = VABL11 – VABL10
ABL_{G2} = VABL12 – VABL10
ABL_{G3} = VABL13 – VABL10
ABL_{G4} = VABL14 – VABL10
ABL_{G5} = VABL15 – VABL10
ABL_{G6} = VABL16 – VABL10
ABL_{G7} = VABL17 – VABL10
ABL_{G8} = VABL18 – VABL10</td></tr>
<tr><td>T14</td><td>RGB output mode</td><td>C</td><td>B</td><td>B</td><td>A</td><td>A</td><td>A</td><td>A</td><td>A</td><td>A</td><td>1. Adjust brightness data so that picture period voltage of pin 12 is 2.4 V.
2. Set subaddress (1B) data to (01).
3. Measure pins 12, 13, and 14 picture period voltage, V_{12R}, V_{13R}, and V_{14R}.
4. Set subaddress (1B) data to (02), and repeat the step 3 above. Measure pins 12, 13, and 14 picture period voltage, V_{12G}, V_{13G}, and V_{14G}.
5. Set subaddress (1B) data to (03), and repeat the step 3 above. Measure pins 12, 13, and 14 picture period voltage, V_{12B}, V_{13B}, and V_{14B}.</td></tr>
</table>

Note No.	Characteristics	Test Conditions									Test Method
		SW Mode									
		SW68	SW67	SW66	SW26	SW25	SW24	SW21	SW19	SW18	
T15	Y-OUT γ characteristic	A	B	B	A	A	A	A	A	A	1. Input RAMP waveform from pin 68. Adjust input amplitude so that picture period amplitude of pin 12 is 2.3 Vp-p. 2. Set subaddress (0C) data to (81). 3. Adjust input amplitude so that picture period amplitude of pin 12 is 2.3 Vp-p. 4. Monitor pin 12. According to the figure below, determine Y-OUT γ correction start points γ1 and γ2. Also determine ratios of gradients at Y-OUT ON to Y-OUT OFF in decibel. (Δ1, Δ2, and Δ3) 

Note No.	Characteristics	Test Conditions									Test Method
		SW Mode									
		SW68	SW67	SW66	SW26	SW25	SW24	SW21	SW19	SW18	
T16	White-peak blue characteristic	A	B	B	A	A	A	A	A	A	1. Input 0.7-Vp-p RAMP signal from pin 68. 2. Set subcontrast data to maximum. 3. Set subaddress (1F) data to (04). 4. Set subaddress (1E) data to (01), and monitor pin 14. Determine blue stretch start point BS_{Pmin} using the figure below. 5. Repeat the step 4 above by changing subaddress (1E) data to (04) and (07). Determine blue stretch start point BS_{PCNT} and BS_{Pmax}. 6. Set subaddress (1E) data to (04). 7. Monitor pin 14 and calculate ratio of blue stretch ON gradient in relative to blue stretch OFF gradient in decibel (BS_{GCNT}) using the figure below. 8. Repeat the step 7 above by changing subaddress (1F) data to (00) and (07). Calculate gradient ratio in decibel (BS_{Gmin} and BS_{Gmax}). Note: Calculate white-peak blue start point in IRE as setting positive amplitude at pedestal level of output signal to 2.3 Vp-p = 100 IRE. 

Note No.	Characteristics	Test Conditions									Test Method
		SW Mode									
		SW68	SW67	SW66	SW26	SW25	SW24	SW21	SW19	SW18	
T17	ACB insertion pulse phase and amplitude	A or C	B	B	A	A	A	A	A	A	1. Input signal 1(f_0 = 100 kHz, picture period amplitude = 0.2 Vp-p) from pin 68. Control drive gain adjustment data so that pins 14 and 13 picture period amplitude equals that of pin 12. Set brightness data to 108. 2. Measure pins 4, 6, and 7 voltage. Apply measured voltages from external power supply. 3. Set subaddress (02) data to (40). 4. Use output signals from pins 12, 13, and 14, and measure ACB insertion pulse phase as shown in the Figure 1. Note: Take picture period following FBP input fall after V • BLK ends as phase 1H. After next H• BLK, count the phase as 2H, 3H, and so on.  Figure 1: RGB Output  Figure 2: FBP Input (#39) 5. Monitor pins 12, 13, and 14. Measure ACB insertion pulse amplitudes (level from picture period amplitude at quiescent.): VACB1R, VACB1G, and VACB2B. 6. Set subaddress (02) data to (80), and repeat the step 5 above: VACB2R, VACB2G, and VACB2B. 7. Set subaddress (02) data to (C0), and repeat the step 5 above: VACB3R, VACB3G, and VACB3B.

Note No.	Characteristics	Test Conditions: SW Mode SW68	SW67	SW66	SW26	SW25	SW24	SW21	SW19	SW18	Test Method
T18	IK input amplitude	A or C	B	B	A	A	A	A	A	A	1. Input signal 1(f_0 = 100 kHz, picture period amplitude = 0.2 Vp-p) from pin 68. Control drive gain adjustment data so that pins 14 and 13 picture period amplitude equals that of pin 12. 2. Set subaddress (02) data to (40). 3. Measure voltage amplitude of pin-8 input signal in ACB insertion period. 1H = IK_R 2H = IK_G 3H = IK_B
T19	IK input cover range	C	B	B	A	A	A	A	A	A	1. Input signal 1(f_0 = 100 kHz, picture period amplitude = 0.2 Vp-p) from pin 68. Control drive gain adjustment data so that pins 14 and 13 picture period amplitude equals that of pin 12. 2. Set subaddress (02) data to (40). 3. Measure pin 8 DC voltage in V・BLK period. (#8VBLK) 4. Apply the current externally to pin 8. 5. Measure DC voltage of pin 8 in V・BLK period when pin-12 picture period voltage begins to be decreased. (#8VBLK+) 6. Apply current outward from pin 8. 7. Measure DC voltage of pin 8 in V・BLK period when pin-12 picture period voltage begins to be increased. (#8VBLK–) 8. DIK_{in+} = (#8VBLK+) – (#8VBLK) DIK_{in-} = (#8VBLK–) + (#8VBLK)
T20	Analog RGB gain	A	B	B	A or B	A or B	A or B	A	A	A	1. Input signal 1(f_0 = 100 kHz, picture period amplitude = 0.2 Vp-p) from pin 68. Control drive gain adjustment data so that pins 14 and 13 picture period amplitude equals that of pin 12. 2. Apply 5-V external voltage to pin 2. 3. Input signal 1(f_0 = 100 kHz, picture period amplitude = 0.2 Vp-p) from pin 24. 4. Measure pin 12 picture period amplitude, v12R. 5. Repeat the steps 3 and 4 above with the following pins: Input from pin 25, and measure output from pin 13 (v13G). Input from pin 26, and measure output from pin 14 (v14B). 6 Calculate the following equations. GTXR = v12R/0.2 GTXG = v13G/0.2 GTXB = v14B/0.2
T21	Analog RGB white peak slice level	A	B	B	A	A	A	A	A	A	1. Input signal 1(f_0 = 100 kHz, picture period amplitude = 0.2 Vp-p) from pin 68. Control drive gain adjustment data so that pins 14 and 13 picture period amplitude equals that of pin 12. 2. Apply 5-V external voltage to pin 2. 3. Set RGB contrast data to maximum (7F). 4. Input signal 2 to pin 24. Gradually increase picture amplitude, and measure picture period amplitude voltage when output from pin 12 is clipped. 5. Repeat the steps 3 and 4 above with following pins: Input from pin 25 and measure output from pin 13. Input from pin 26 and measure output pin 14.

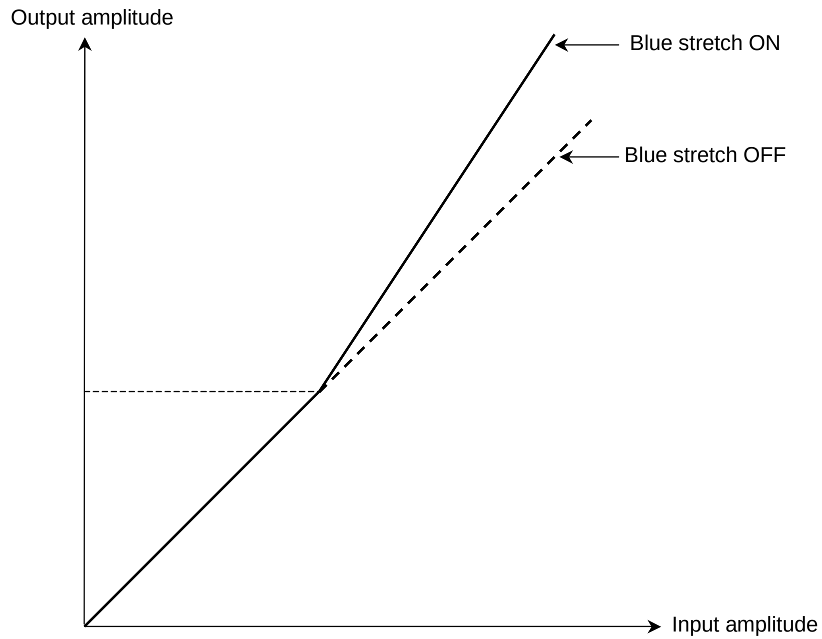
Note No.	Characteristics	Test Conditions									Test Method
		SW Mode									
		SW68	SW67	SW66	SW26	SW25	SW24	SW21	SW19	SW18	
T22	Analog RGB black peak limit level	A	B	B	A	A	A	A	A	A	1. Input signal 1(f_0 = 100 kHz, picture period amplitude = 0.2 Vp-p) from pin 68. Control drive gain adjustment data so that pins 14 and 13 picture period amplitude equals that of pin 12. 2. Apply 5-V external voltage to pin 2. 3. Set RGB contrast data to maximum (7F). 4. Input signal 2 to pin 24. Gradually decrease picture amplitude, and measure picture period amplitude voltage when output from pin 12 is clipped. 5. Repeat the step 4 above with the following pins: Input from pin 25 and measure output from pin 13. Input from pin 26 and measure output pin 14.
T23	RGB contrast adjustment characteristic	A	B	B	A or B	A or B	A or B	A	A	A	1. Input signal 1(f_0 = 100 kHz, picture period amplitude = 0.2 Vp-p) from pin 68. Control drive gain adjustment data so that pins 14 and 13 picture period amplitude equals that of pin 12. 2. Apply 5-V external voltage to pin 2. 3. Input signal 1 (f_0 = 100 kHz, picture period amplitude = 0.2 Vp-p) from pin 24. 4. RGB contrast data to maximum (7F), center (40), and minimum (00). Measure pin 12 picture period amplitudes V_{uTXR} (maximum, center, and minimum) respectively. 5. Calculate amplitude ratio of maximum and minimum in decibels. 6. Repeat the steps 4 and 5 above with the following pins: Input from pin 25 and measure pin 13. Input from pin 26 and measure pin 14.
T24	Analog RGB brightness adjustment characteristic	A	B	B	A or B	A or B	A or B	A	A	A	1. Input signal 1(f_0 = 100 kHz, picture period amplitude = 0.2 Vp-p) from pin 68. Control drive gain adjustment data so that pins 14 and 13 picture period amplitude equals that of pin 12. 2. Input signal 2 from pins 26, 25, and 24. 3. Apply 5-V external voltage to pin 2. 4. Adjust amplitude A of signal 2 so that picture period amplitude of pin 12 is 0.5 Vp-p. 5. Change RGB brightness data to maximum (FE), center (80), and minimum (00). Measure pins 12, 13, and 14 picture period voltage V_{brTX} (maximum, center, and minimum) respectively.
T25	Analog RGB mode switching transfer characteristic	C	B	B	A	A	A	A	A	A	1. Set RGB brightness data to maximum (FE). 2. Input signal 4 (signal amplitude = 1.5 Vp-p) from pin 2. 3. Measure input/output transfer characteristics using pin 12 according to the figure T-2. 4. Repeat the steps 2 and 3 above with the following pins: Input from pin 25 and measure pin 13. Input from pin 24 and measure pin 14. 5. Calculate maximum inter-axial rise/fall transfer delay time, using the data measured above.

Note No.	Characteristics	Test Conditions									Test Method
		SW Mode									
		SW68	SW67	SW66	SW26	SW25	SW24	SW21	SW19	SW18	
T26	Text ACL characteristic	A	B	B	A	A	B	A	A	A	1. Input signal 1(f_0 = 100 kHz, picture period amplitude = 0.2 Vp-p) from pin 68. Control drive gain adjustment data so that pins 14 and 13 picture period amplitude equals that of pin 12. 2. Apply 5-V external voltage to pin 2. 3. Input signal 1(f_0 = 100 kHz, picture period amplitude = 0.2 Vp-p) from pin 24. 4. Measure pin 12 picture period amplitude, vTXACL1. 5. Apply “pin 78 DC voltage – 0.8 V” to pin 78 from external power supply, and measure pin 12-picture period amplitude, vTXACL2. 6. Apply “pin 78 DC voltage – 1.3 V” to pin 78 from external power supply, and measure pin 12-picture period amplitude, vTXACL3. 7. $TXACL_1 = -20 \times \ell og$ (vTXACL2/vTXACL1) $TXACL_2 = -20 \times \ell og$ (vTXACL3/vTXACL1)
T27	Analog OSD gain	A	B	B	A	A	A	A or B	A or B	A or B	1. Input signal 1(f_0 = 100 kHz, picture period amplitude = 0.2 Vp-p) from pin 68. Control drive gain adjustment data so that pins 14 and 13 picture period amplitude equals that of pin 12. 2. Apply 5-V external voltage to pins 1 and 80. 3. Input signal 1(f_0 = 100 kHz, picture period amplitude = 0.2 Vp-p) from pin 18. 4. Measure pin 12 picture period amplitude, v12R. 5. Repeat the steps 3 and 4 above with the following pins: Input from pin 19, and measure pin 13. Input from pin 21 and measure pin 14. (v13G and v14B) 6. Calculate the following equations. G_{OSDR} = v12R/0.2 G_{OSDG} = v13G/0.2 G_{OSDB} = v14B/0.2
T28	Analog OSD input white peak slice level	A	B	B	A	A	A	A	A	A	1. Input signal 1(f_0 = 100 kHz, picture period amplitude = 0.2 Vp-p) from pin 68. Control drive gain adjustment data so that pins 14 and 13 picture period amplitude equals that of pin 12. 2. Apply 5-V external voltage to pins 1 and 80. 3. Input signal 2 from pin 18. Gradually increase picture amplitude, and measure picture period amplitude voltage when output from pin 12 is clipped. 4. Repeat the step 3 above with the following pins: Input from pin 19, and measure pin 13. Input from pin 21, and measure pin 14.
T29	Analog OSD black peak limit level	A	B	B	A	A	A	A	A	A	1. Input signal 1(f_0 = 100 kHz, picture period amplitude = 0.2 Vp-p) from pin 68. Control drive gain adjustment data so that pins 14 and 13 picture period amplitude equals that of pin 12. 2. Apply 5-V external voltage to pins 1 and 80. 3. Input signal 2 from pin 18. Gradually decrease picture amplitude, and measure picture period amplitude voltage when output from pin 12 is clipped. 4. Repeat the step 3 above with the following pins: Input from pin 19, and measure pin 13. Input from pin 21, and measure pin 14.

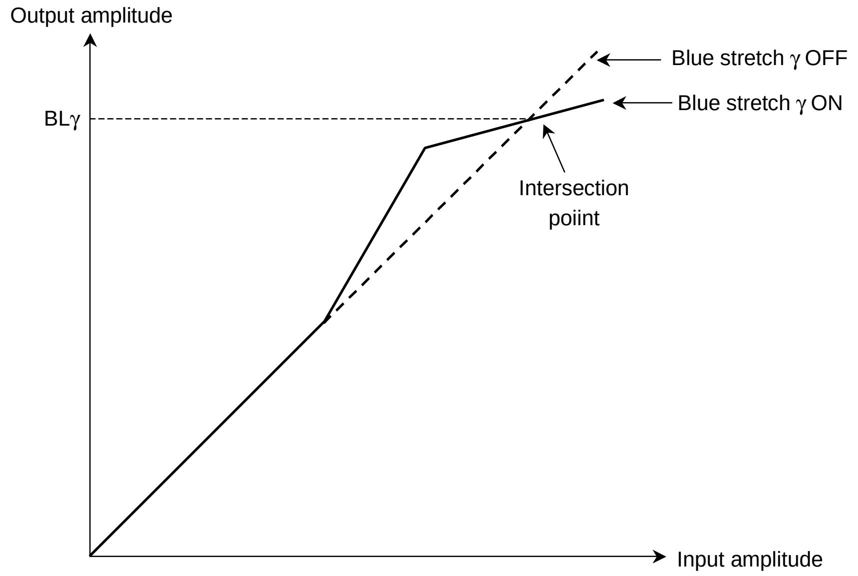
Note No.	Characteristics	Test Conditions									Test Method
		SW Mode									
		SW68	SW67	SW66	SW26	SW25	SW24	SW21	SW19	SW18	
T30	OSD contrast adjustment characteristic	A	B	B	A	A	A	A or B	A or B	A or B	1. Input signal 1(f_0 = 100 kHz, picture period amplitude = 0.2 Vp-p) from pin 68. Control drive gain adjustment data so that pins 14 and 13 picture period amplitude equals that of pin 12. 2. Apply 5-V external voltage to pins 1 and 80. 3. Input signal 1(f_0 = 100 kHz, picture period amplitude = 0.2 Vp-p) from pin 18. 4. Change OSD contrast data to (11), (10), (01), and (00). Measure pin 12 picture period amplitude V_{uOSDR} (11), (10), (01), and (00) respectively. 5. Repeat the steps 3 and 4 above with the following pins: Input from pin 19, and measure pin 13, V_{uOSDG} (11), (10), (01), and (00). Input from pin 21, and measure pin 14, VuOSDB (11), (10), (01), and (00).
T31	Analog OSD brightness adjustment characteristic	C	B	B	A	A	A	A	A	A	1. Input signal 1(f_0 = 100 kHz, picture period amplitude = 0.2 Vp-p) from pin 68. Control drive gain adjustment data so that pins 14 and 13 picture period amplitude equals that of pin 12. 2. Apply 5-V external voltage to pins 1 and 80. 3. Change OSD brightness data (subaddress 1D) to (38), (78), (B8), and (F8), and measure picture period voltage of pins 12, 13, and 14 respectively. Data (38) = V_{brOSD0} Data (78) = V_{brOSD1} Data (B8) = V_{brOSD2} Data (F8) = V_{brOSD3}
T32	Analog OSD mode switching transfer characteristic	C	B	B	A	A	A	A	A	A	1. Set OSD brightness data to maximum (11). 2. Input signal 4 (signal amplitude = 4.5 Vp-p) from pin 1. 3. Measure input/output transfer characteristics using pin 12 according to the figure T-2. 4. Repeat the steps 2 and 3 above, and measure pins 13 and 14. 5. Calculate maximum inter-axial rise/fall transfer delay time, using the data measured above. 6. Repeat the steps 1 to 5 above with the following pin. Input signal 4 (signal amplitude 4.5 Vp-p) from pin 80.

Note No.	Characteristics	Test Conditions									Test Method
		SW Mode									
		SW68	SW67	SW66	SW26	SW25	SW24	SW21	SW19	SW18	
T33	OSD ACL characteristic	A	B	B	A	A	A	A	A	B	1. Input signal 1(f_0 = 100 kHz, picture period amplitude = 0.2 Vp-p) from pin 68. Control drive gain adjustment data so that pins 14 and 13 picture period amplitude equals that of pin 12. 2. Set subaddress (07) data to (01). 3. Apply 5-V external voltage to pins 1 and 80. 4. Input signal 1 (f_0 = 100 kHz, picture period amplitude = 0.2 Vp-p) from pin 18. 5. Measure pin 12 picture period amplitude, vOSDACL1. 6. Apply “pin 78 DC voltage − 0.8 V” to pin 78 from external power supply, and measure pin 12-picture period amplitude, vOSDACL2. 7. Apply “pin 78 DC voltage – 1.3 V” to pin 78 from external power supply, and measure pin 12-picture period amplitude, vOSDACL3. 8. $OSDACL_1 = -20 \times \ell og$ (vOSDACL2/vOSDACL1) $OSDACL_2 = -20 \times \ell og$ (vOSDACL3/vOSDACL1) 9. OSDACL3、OSDACL4 Change subaddress (07) data to (80), and repeat the steps 6 to 8 above to measure OSDACL3 and OSDACL4.

Note No.	Characteristics	Test Conditions									Test Method
		SW Mode									
		SW68	SW67	SW66	SW26	SW25	SW24	SW21	SW19	SW18	
T34	OSD blending characteristic	A ↓ C	B	B	A	A	A	A ↓ B	A ↓ B	B ↓ B	1. Input signal 1(f_0 = 100 kHz, picture period amplitude = 0.2 Vp-p) from pin 68. 2. Measure pins 14, 13, and 12 picture period amplitude, v14a, v13a, and v12a. 3. Apply 5-V external voltage to pin 80. 4. Measure pins 14, 13, and 12 picture period amplitude, v14b, v13b, and v12b. 5. Calculate v14b amplitude in relation to v14a, v13b amplitude in relation to v13a, and v12b amplitude in relation to v12a in decibel: α14TV1, α13TV1, and α12TV1. 6. Apply 5-V external voltage to pin 1, and repeat the steps 3 to 5 above: α14TV2, α13TV2, and α12TV2. 7. Apply 5-V external voltage to pins 1 and 80, and repeat the steps 3 to 5 above: α14TV3, α13TV3, and α12TV3. 8. Set SW68 to C. Set SW21, 19, and 18 to B. 9. Input signal 1 (f_0 = 100 kHz, picture period amplitude = 0.2 Vp-p) from pins 21, 19, and 18. 10. Apply 5-V external voltage to pins 1 and 80. 11. Measure pins 14, 13, and 12 picture period amplitude, v14c, v13c, and v12c. 12. Apply 5-V external voltage to pin 1. 13. Measure pins 14, 13, and 12 picture period amplitude, v14d, v13d, and v12d. 14. Calculate v14d amplitude in relation to v14c, v13d amplitude in relation to v13c, and v12d amplitude in relation to v12c in decibel: α14OSD1, α13OSD1, and α12OSD1. 15. Apply 5-V external voltage to pin 80, and repeat the steps 12 to 14 above: α14OSD2, α13OSD2, and α12OSD2. 16. Apply 5-V external voltage to pins 1 and 80, and repeat the steps 12 to 14 above: α14OSD3, α13OSD3, and α12OSD3.

Note No.	Characteristics	Test Conditions SW Mode SW68	SW67	SW66	SW26	SW25	SW24	SW21	SW19	SW18	Test Method
T35	Blue stretch point/gain	A	B	B	A	A	A	A	A	A	1. Input RAMP signal 0.7 Vp-p from pin 68. 2. Set subcontrast data to maximum. 3. Set subaddress (15) data to (0C). 4. Set subaddress (1A) data to (C0), monitor pin 14, and measure blue stretch start point using the figure below (BLP_{min}). 5. Set subaddress (1A) data to (CC), and repeat the step 4 above. (BLP_{max}) 6. Set subaddress (1A) data to (C4). 7. Monitor pin 14 and measure gradient at blue stretch ON in decibel in relation to the one at blue stretch OFF according to the figure below. (BLG_{max}) 8. Set subaddress (15) data to (04), and repeat the step 7 above. (BLG_{min}) Note: Calculate blue stretch start point in IRE as setting positive amplitude at pedestal level of output signal to 2.3 Vp-p = 100 IRE. 

Note No.	Characteristics	Test Conditions									Test Method
		SW Mode									
		SW68	SW67	SW66	SW26	SW25	SW24	SW21	SW19	SW18	
T36	Blue stretch gamma correction	A	B	B	A	A	A	A	A	A	1. Input RAMP signal 0.7 Vp-p from pin 68. 2. Set subcontrast data to maximum. 3. Set subaddress (15) data to (08). 4. Set subaddress (09) data to (81). 5. Monitor pin 14 and measure amplitude of the intersection point of blue stretch γ OFF and blue stretch γ ON according to the figure below. Calculate pin 14 output amplitude in IRE as setting positive amplitude at pedestal level of output signal to 2.3 Vp-p = 100 IRE. 6. Set subaddress (1A) data to (C4), (C8), and (CC). Repeat the step 5 above. (BLγ2, BLγ3, and BLγ4)



Note No.	Characteristics	Test Conditions									Test Method
		SW Mode									
		SW68	SW67	SW66	SW26	SW25	SW24	SW21	SW19	SW18	
T37	White letters improvement	A	B	B	A	A	A	A	A	A	1. Apply a pulse to pin 68 as shown in Figure A. 2. Monitor # 12 output waveform. Plot # 12 output amplitude when changing # 68 input signal amplitude from 0 to 120 IRE (0.857 Vp-p) (See Figure B below). 3. Set subaddress (19) data to (80). 4. Monitor # 12 output waveform. Plot # 12 output amplitude when changing # 68 input signal amplitude from 0 to 120 IRE (0.857 Vp-p). Then, compare to the plot in the step 2, calculate a point where a gradient changes (WPL1). 5. Repeat the step 4 above by changing subaddress (19) data to (83) and (86). Calculate points where gradients change (WPL2, WPL3).

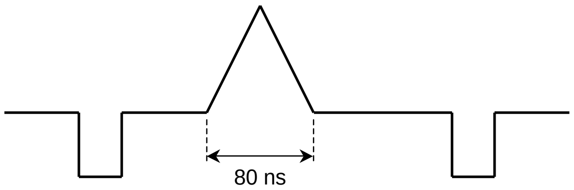


Figure A

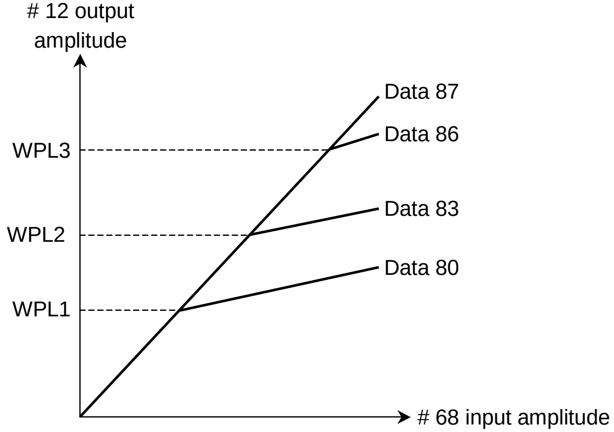
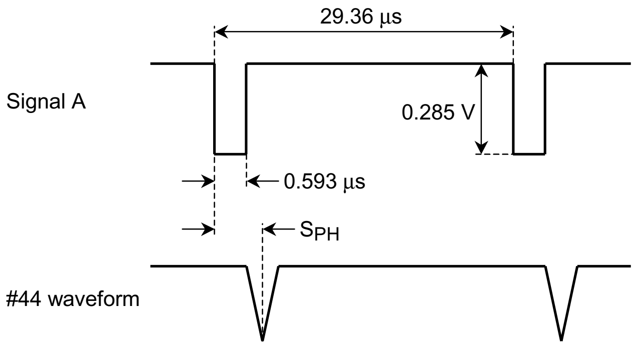
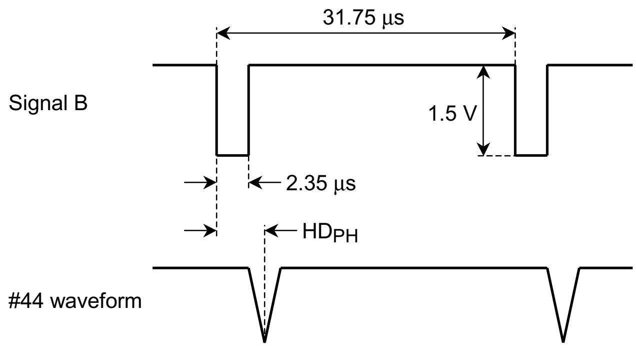
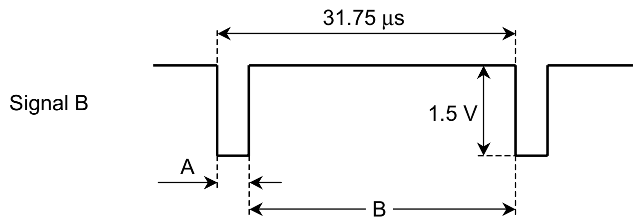
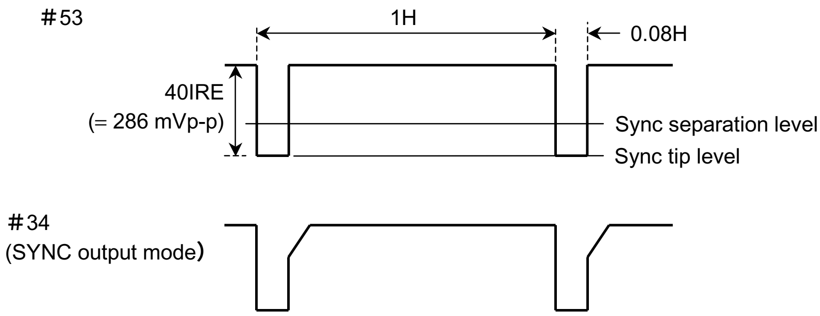


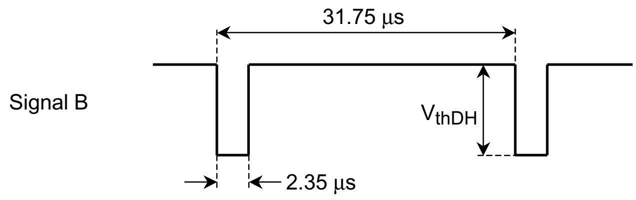
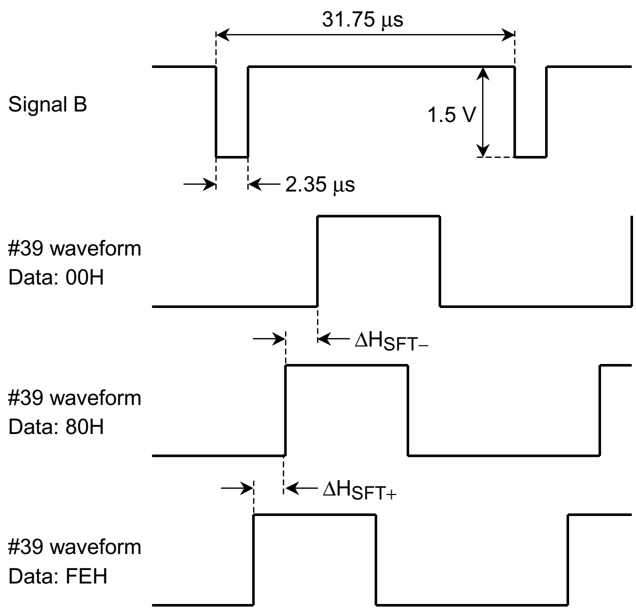
Figure B

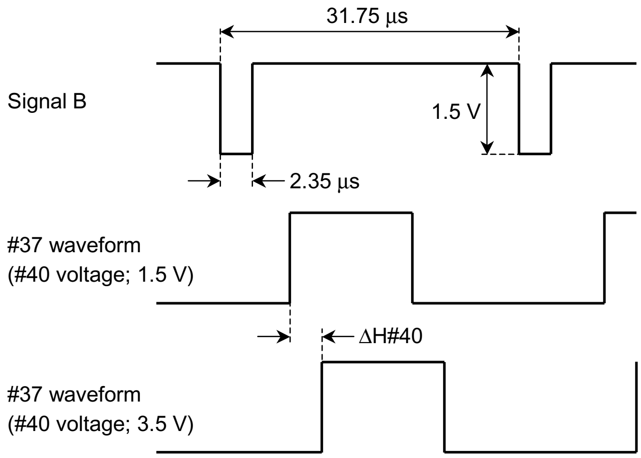
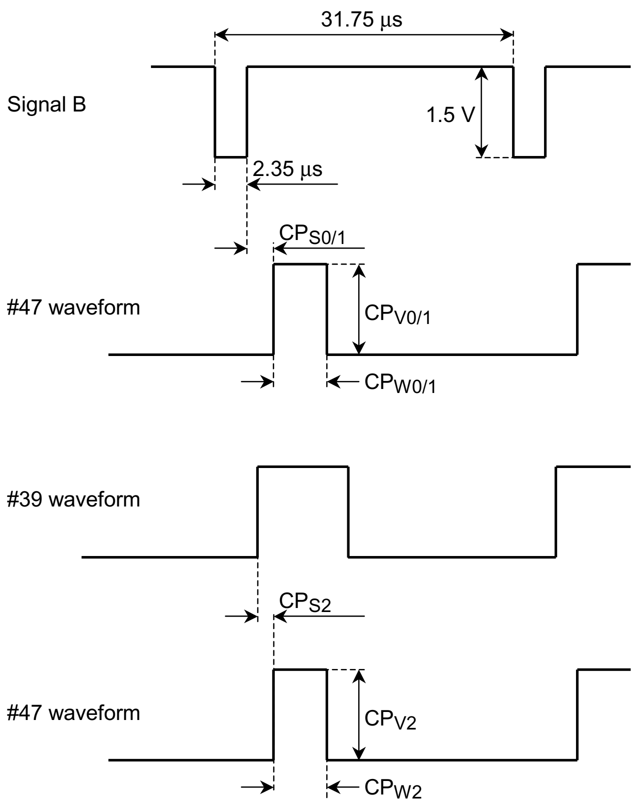
Test Condition for Synchronization Block

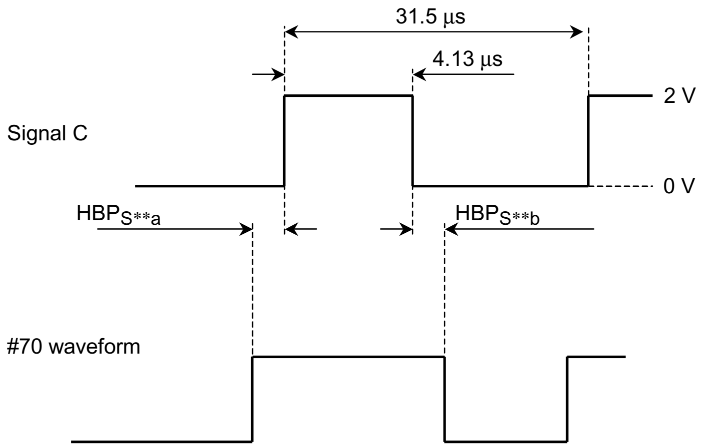
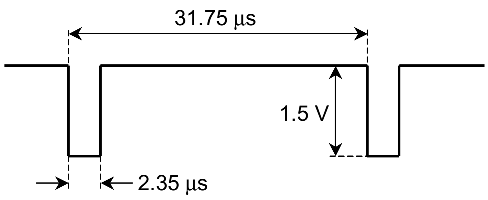
Common Test Conditions for Synchronization Block: unless otherwise specified, V_{CC} = 9 V, Ta = 25°C, bus data; preset value, SW68 = A, SW53 = A, SW INPUT = B, SW44 = ON, SW41 = OPEN, SW40 = B, SW39a = B, SW39b = OPEN, SW37 = B

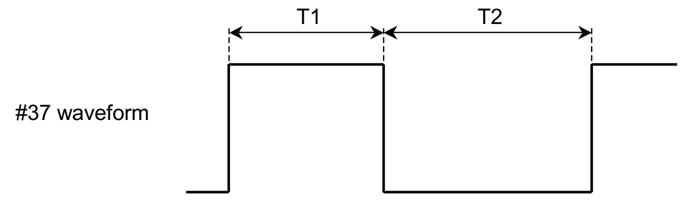
Note	Characteristics	Test Conditions
HA01	Sync input horizontal sync phase	1. Input signal A (as shown in the figure below) to TPA. Set subaddress (00) data to 82H. 2. Monitor # 53 (Sync input) and #44 (AFC filter) waveforms. Measure phase difference (S_{PH}). 
HA02	HD input horizontal sync phase	1. Set subaddress (00) data to 40H. 2. Input signal B (as shown in the figure below) to TP50. 3. Monitor #50 (Sync input) and #44 (AFC filter) waveforms. Measure phase difference (HD_{PH}). 

<table>
<tr><th>Note</th><th>Characteristics</th><th>Test Conditions</th></tr>
<tr><td>HA03</td><td>Polarity detection range</td><td>1. Set subaddress (00) data to 40H.
2. Input signal B (as shown in the figure below) to TP50 pin.
3. Decrease signal B duty from 10% (to shorter negative polarity period) and measure signal B duty (HD_{DUTY1}) when #50 input signal phase no longer locks with that of #37 (H-OUT).
4. Increase signal B duty from 10% (to longer negative polarity period) and measure signal B duty (HD_{DUTY2}) when #39 (FBP input) phase changes in relation to signal B.
5. Further increase signal B duty (to longer negative polarity period) and measure signal B duty (HD_{DUTY3}) when #50 input signal phase no longer locks with that of #37 (H-OUT).
6. Decrease signal B duty from 90 % (to shorter negative polarity period) and measure signal B duty (HD_{DUTY4}) when #39 (FBP input) phase changes in relation to signal B.

Duty = A/B × 100% (0 to 100%)</td></tr>
<tr><td>HA04</td><td>Sync input threshold amplitude</td><td>1. Set subaddress (00) data to 82H, and TEST mode to 01.
2. Connect variable power supply to #53 via 20-kΩ resistor.
3. Set variable power supply voltage to 0 V, and measure #53 voltage. (SYNC_TIP_00) Also check that #34 voltage is set to Low (GND level).
4. Increase variable power supply voltage so that #34 voltage becomes High (VCC level). Measure #53 voltage. (SYNC_OFF_00)
5. Calculate the following equation to determine SYNC input separation level at SYNC separation level is 00. V_{thS00} = (SYNC_OFF_00 – SYNC_TIP_00)/0.286 × 100
6. Change SYNC separation level to 01, 10, and 11. Calculate following equations to determine VthS01, VthS10, and VthS11.
V_{thS01} = (SYNC_OFF_01 – SYNC_TIP_01)/0.286 × 100
V_{thS10} = (SYNC_OFF_10 – SYNC_TIP_10)/0.286 × 100
V_{thS11} = (SYNC_OFF_11 – SYNC_TIP_11)/0.286 × 100
</td></tr>
</table>

Note	Characteristics	Test Conditions
HA05	HD input threshold amplitude	1. Set subaddress (00) data to 40H. 2. Input signal B (as shown in the figure below) to TP50. 3. Increase signal B amplitude from 0 Vp-p. When #37 (H-OUT) phase locks with that of signal B, measure signal B amplitude V_{thHD}. 
HA06	Horizontal picture phase adjustment variable range	1. Set subaddress (00) data to 40H. 2. Input signal B (the figure is shown below) to TP50. 3. Change subaddress (01) data from 80H to 00H, and measure phase change amount ΔH_{SFT-} of #39 (H-OUT) waveform. 4. Change slave address (01) data from 80H to FEH, and measure phase change amount ΔH_{SFT+} of #39 (H-OUT) waveform. 

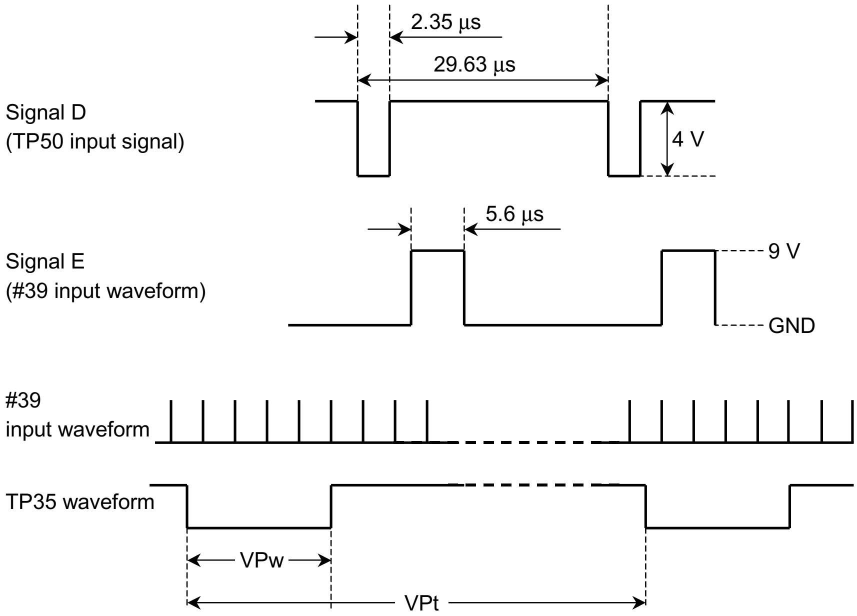
Note	Characteristics	Test Conditions
HA07	Curve correction amount	1. Set subaddress (00) data to 40H. 2. Input signal B (as shown in the figure below) to TP50. 3. Connect external voltage to #40 (curve correction), and measure phase change amount (ΔH#40) of #37 (H-OUT) output waveform at 1.5 V and 3.5 V. 
HA08	Clamp pulse phase, width and level	1. Set subaddress (00) data to 40H. 2. Input signal B (as shown in the figure below) to TP50. 3. Measure #47 (SCP output) clamp pulse phase (CP_{S0}), width (CP_{PW0}), and output level (CP_{V0}) in relation to signal B. 4. Set subaddress (01) data to 81H, and repeat the step 3 above to measure (CP_{S1}), (CP_{W1}), and (CP_{V1}). 5. Apply no signal input to TP50. 6. Measure #47 clamp pulse phase (CP_{S2}), width (CP_{W2}), and output level (CP_{V2}) in relation to #39. 

Note	Characteristics	Test Conditions
HA09	Black peak detection pulse phase and level	1. Set subaddress (00) data to 40H. 2. Set SW70 to C, SW68 to C, and SW39A to OPEN 3. Input signal C (as the figure shown below) to #39 (FBP input). 4. Measure #70 (BPH filter) black peak detection pulse phase (HBP_{S00a} and HBP_{S00b}) in relation to signal C. 5. Set HBP-PHS 1/2 to (01), (10), and (11). Measure black peak detection pulse phase. 
HA10	FBP input threshold	1. Set subaddress (00) data to 40H. 2. Input signal B (as shown in the figure below) to TP50. 3. Increase amplitude of FBP signal to be input to #39 (FBP input) from 0 Vp-p. When #37 (H-OUT) phase locks with that of signal B, measure #39 input amplitude V_{thFBP}. 

Note	Characteristics	Test Conditions
HB01	H-OUT pulse duty	1. No signal input. 2. Measure T1 and T2 (as shown in the figure below) from #37 (H-OUT) output waveform when subaddress (00) data is 80H and A0H. Calculate duties (TH_A and TH_B) using the following equation: $TH = T1/(T1 + T2) \times 100$ % 
HB02	Horizontal free-run frequency	1. Set SW44 to open. 2. Set subaddress (00) data to 01H and measure horizontal free-run frequency (F15K) according to #37 (H-OUT) output waveform. 3. Set subaddress (00) data to 00H, 41H, 81H, C0H, and C1H. Measure horizontal free-run frequency F28K, F31K, F33K, F37K, and F45K as in the step 2 above.
HB03	Horizontal oscillation frequency variable range	1. Set subaddress (00) data to 01H. 2. Connect 10-kΩ resistor between #44 and V_{CC}. Measure horizontal frequency ($F15K_{MIN}$) according to #37 (H-OUT) output waveform. 3. Connect 68-kΩ resistor between #44 and GND. Measure horizontal frequency ($F15K_{MAX}$) according to #37 (H-OUT) output waveform. 4. Set subaddress (00) data to 00H, 41H, 81H, C0H, and C1H. Repeat the steps 2 and 3 above and measure horizontal frequencies $F28K_{MIN}$, $F28K_{MAX}$, $F31K_{MIN}$, $F31K_{MAX}$, $F33K_{MIN}$, $F33K_{MAX}$, $F37K_{MIN}$, $F37K_{MAX}$, $F45K_{MIN}$, and $F45K_{MAX}$.
HB04	Horizontal oscillation control sensitivity	1. Set SW44 to open. 2. Connect external power supply to TP44, and set subaddress (00) data to 01H. 3. Apply V_{44} + 0.05 V, and V_{44} − 0.05 V to TP44. Measure frequencies FA and FB according to #37 (H-OUT) output waveform. Calculate frequency change rate (BH15K) using the following equation. BH15K = (FB − FA)/0.1 4. Set subaddress (00) data to 00H, 41H, 81H, C0H, and C1H. Repeat the step 2 above, and measure frequency change rate BH28K, BH31K, BH33K, BH37K, and BH45K
HB05	H-OUT output voltage	1. Set SW37 to open. 2. Measure voltage at High ($V37_H$) and Low ($V37_L$) of #37 (H-OUT) output waveform.

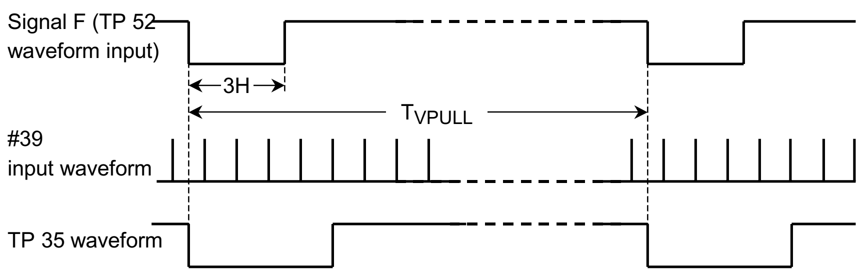
<table>
<tr><th>Note</th><th>Characteristics</th><th>Test Conditions</th></tr>
<tr><td>V01</td><td>VP output pulse width, Vertical free-run (maximum pull-in range)</td><td>

1. Input signal D (shown in the figure below) to TP50, and signal E (shown in the figure below) to #39 (FBP input).
2. Measure VP output pulse width (VPw) according to TP35 output waveform.
3. Measure VP pull-in range (VPt0) according to TP35 output waveform.
4. Set subaddress (03) data to 01H, 02H, 03H, 04H, 05H, and 06H. Measure pull-in range VPt1, VPt2, VPt3, VPt4, VPt5, and VPt6 as in the step 3 above.



</td></tr>
<tr><td>V02</td><td>Vertical minimum pull-in range</td><td>

1. Repeat the step 1 of Note #V01.
2. Input signal F (shown in the figure below) to TP52.
3. Increase signal-F cycle from 30 H. Measure the cycle (T_{VPULL}) when phase locks with that of TP35.



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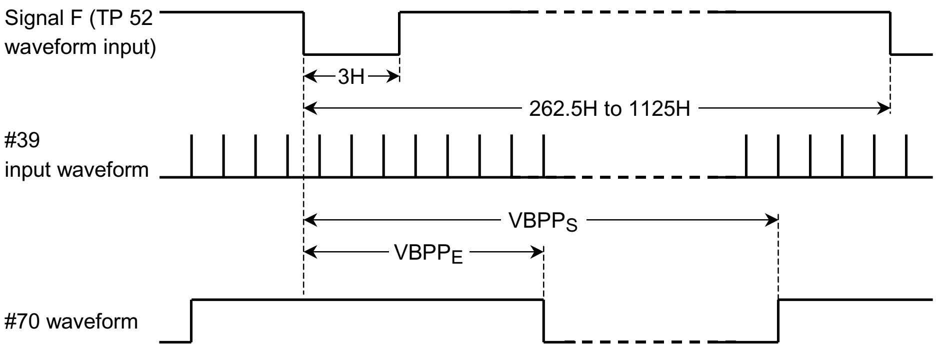
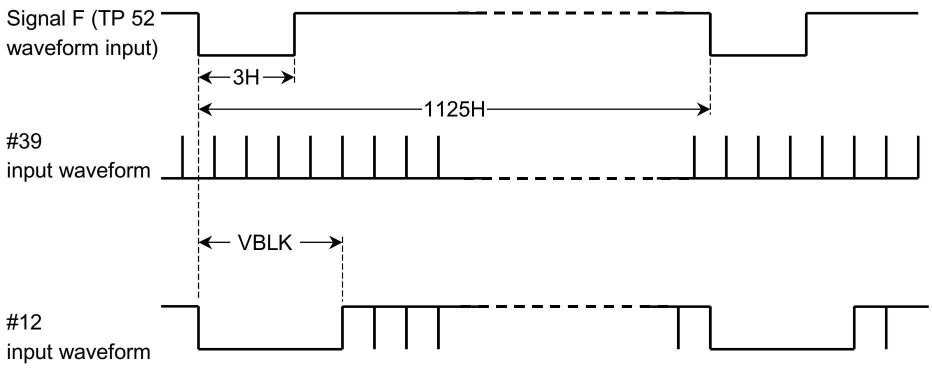
<table>
<tr><th>Note</th><th>Characteristics</th><th>Test Conditions</th></tr>
<tr><td>V03</td><td>Vertical black peak detection pulse</td><td>
1. Repeat the step 1 of Note #V01. Set SW70 to C, and SW68 to C.
2. Input signal F (shown in the figure below) to TP52.
3. Measure phase differences $VBPP_{0E}$ and $VBPP_{0S}$ according to #47 output waveform.
4. Set subaddress (03) data to 01H, 02H, 03H, 04H, 05H, and 06H. Measure phase differences $VBPP_{1E}$, $VBPP_{1S}$, $VBPP_{2E}$, $VBPP_{2S}$, $VBPP_{3E}$, $VBPP_{3S}$, $VBPP_{4E}$, $VBPP_{4S}$, $VBPP_{5E}$, $VBPP_{5S}$, $VBPP_{6E}$, and $VBPP_{6S}$ as in the step 3 above.


</td></tr>
<tr><td>V04</td><td>Vertical blanking stop phase</td><td>
1. Repeat the step 1 of Note #V01.
2. Input signal F (shown in the figure below) to TP52.
3. Set subaddress (03) data to 00H and F0H. Measure blanking stop phase $VBLK_{MIN}$ and $VBLK_{MAX}$ according to #12 output waveform.


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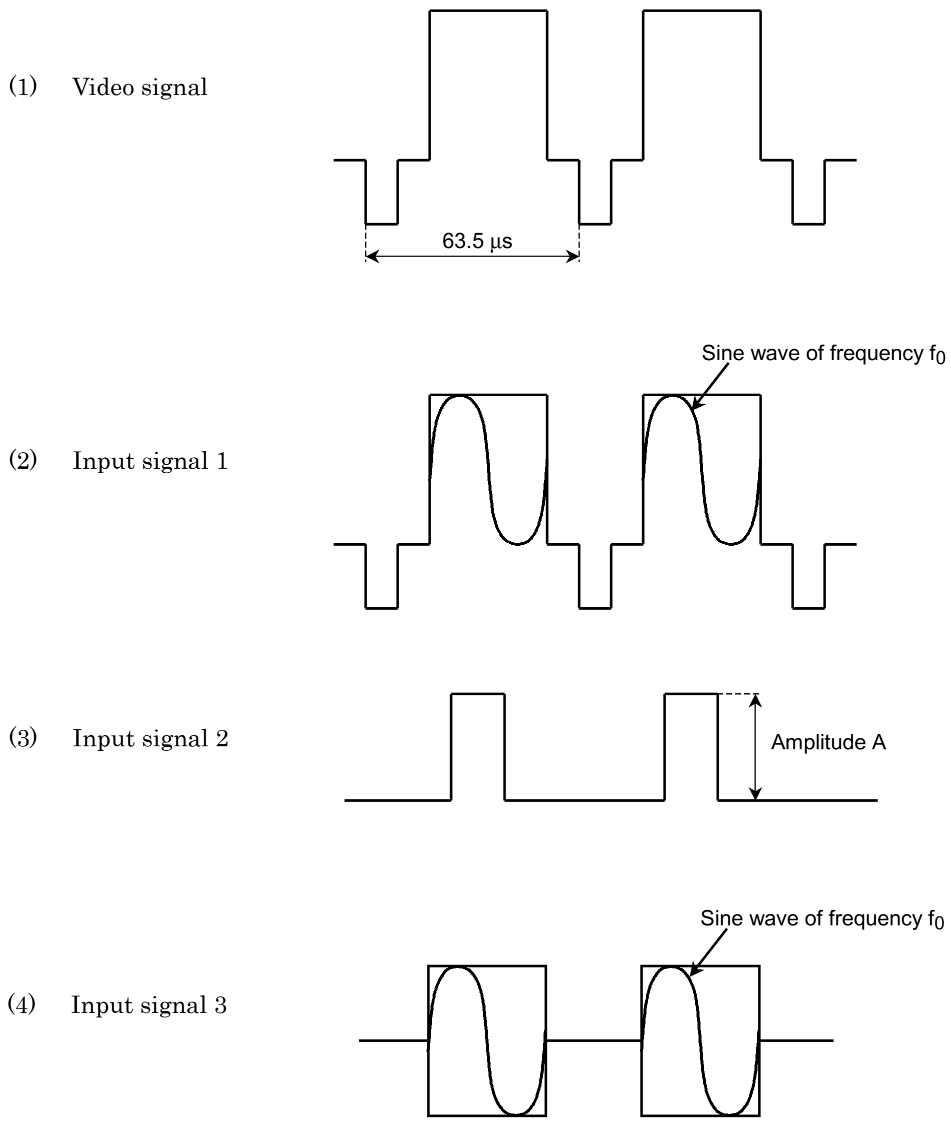


Figure T-1 Signals for Text/Color Difference Signal 2

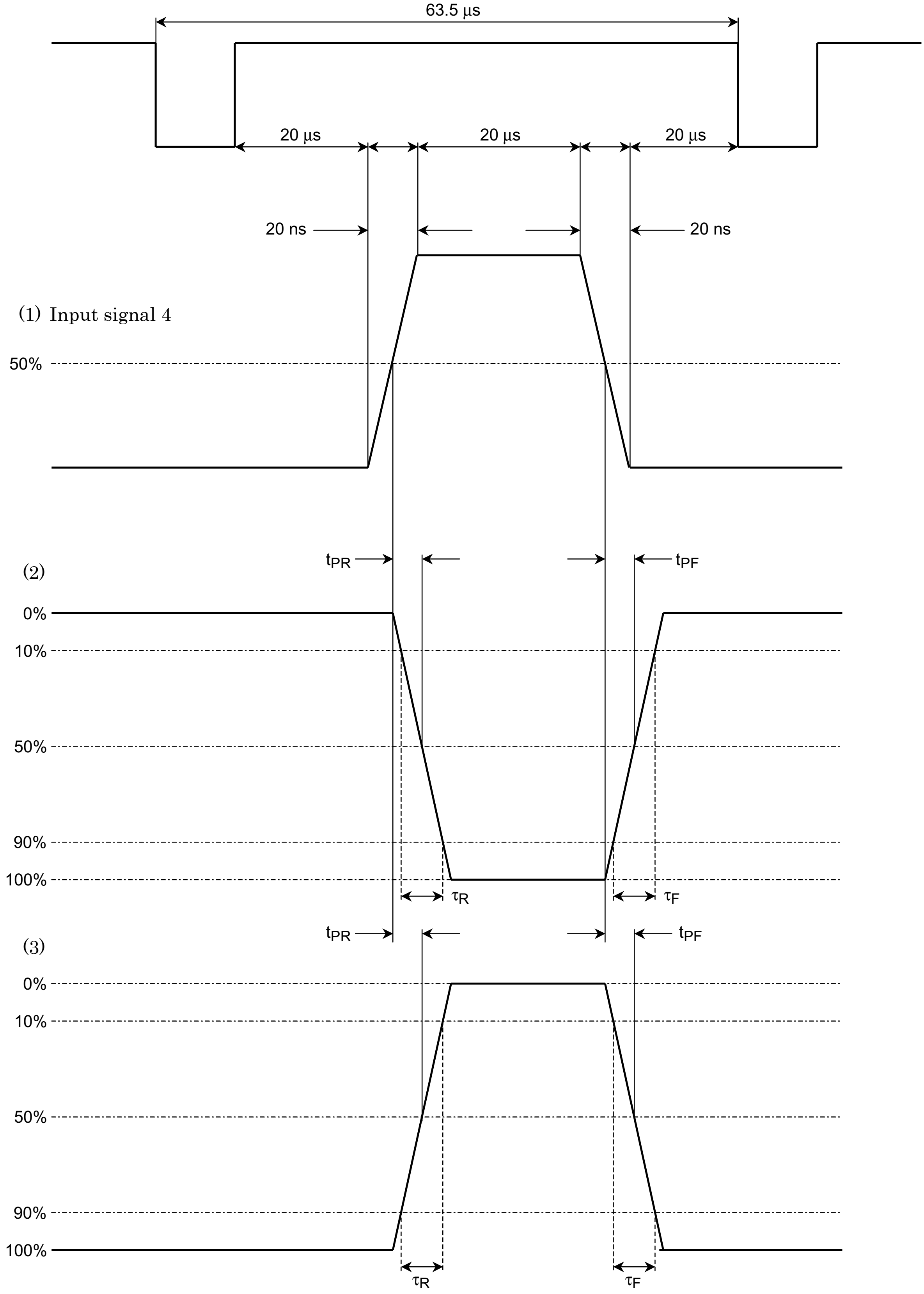
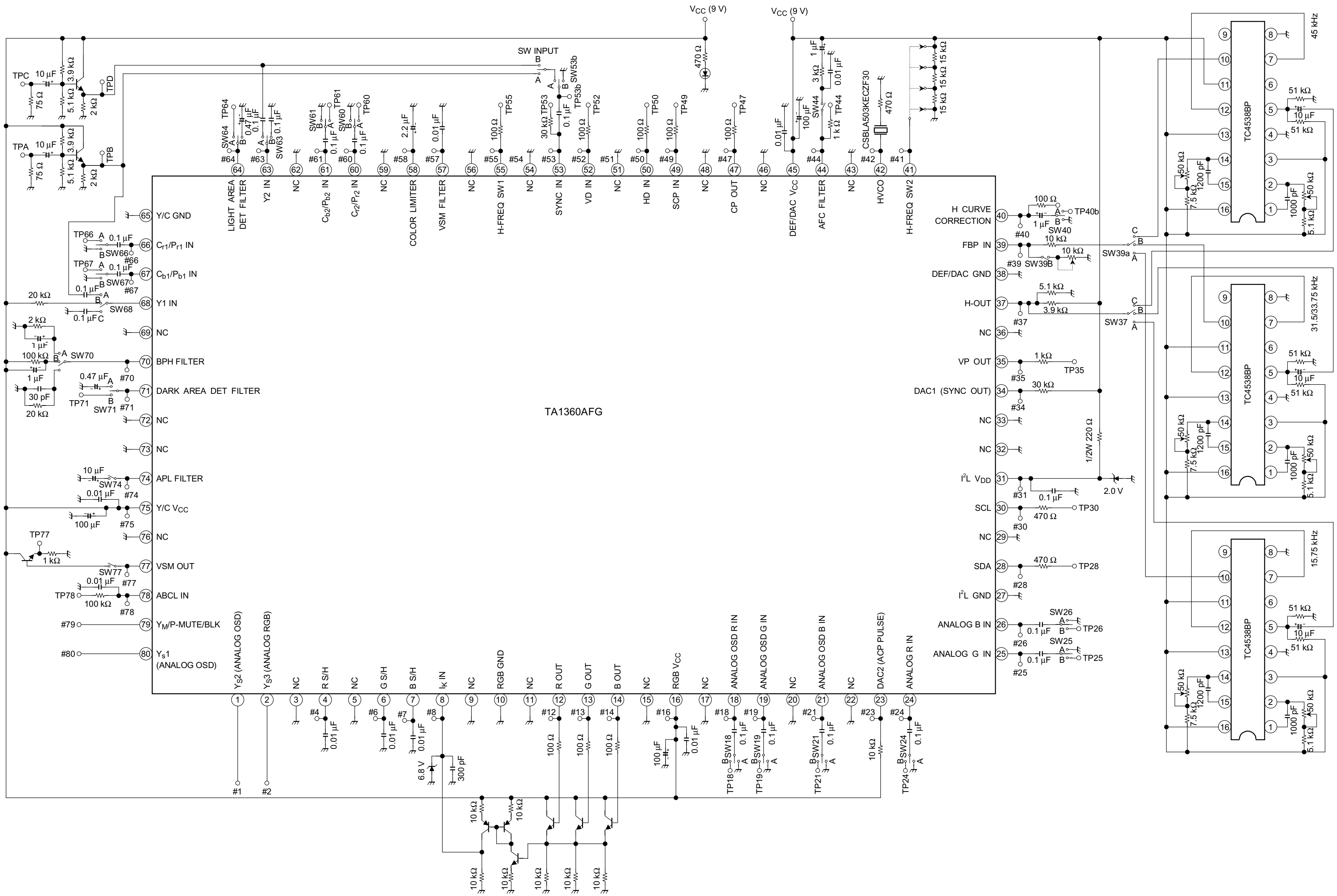
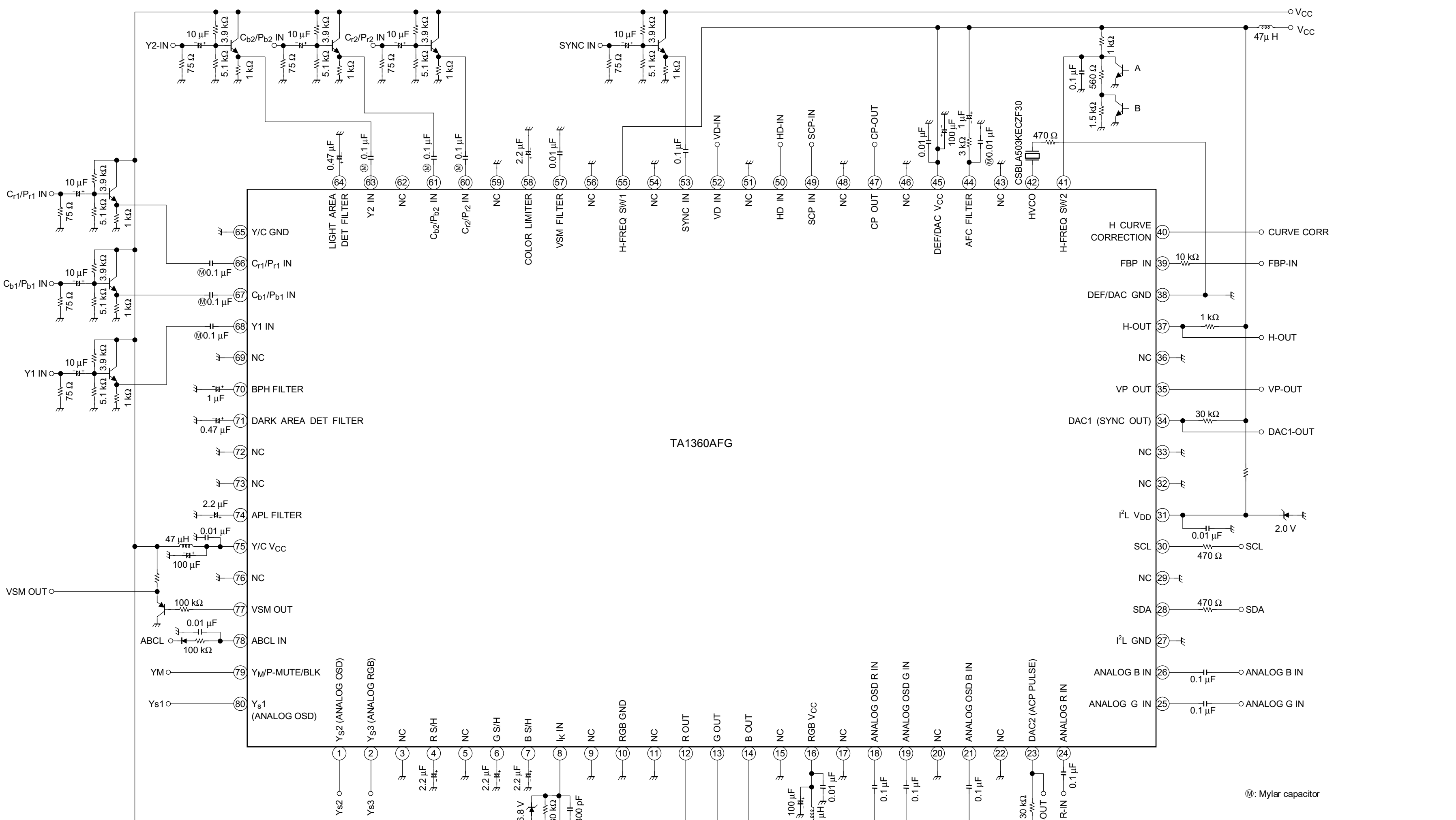


Figure T-2 Test Pulses for Text/Color Difference Signal 2

Test Circuit



Application Circuit

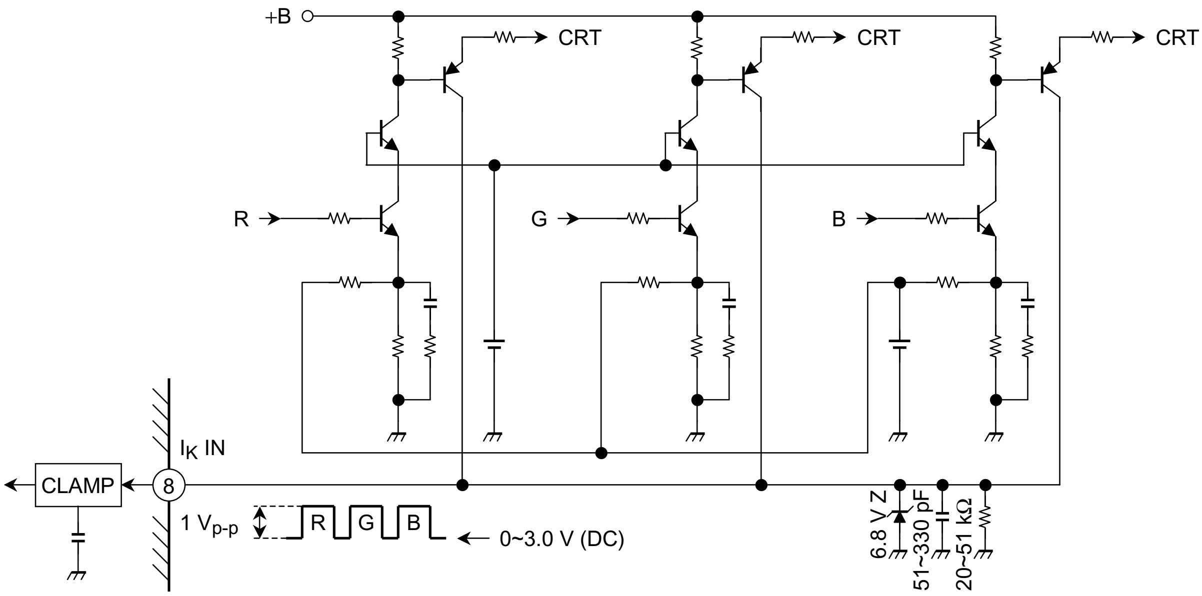


Application of H-FREQ switching (31.5 k/33.75 k/45 kHz)

Tr. / H-FREQ	A	B	Pin 55 voltage	Pin 41 voltage
31.5 kHz	L	L	9 V	6 V
33.75 kHz	L	H	9 V	3 V
45 kHz	H	*	9 V	0 V

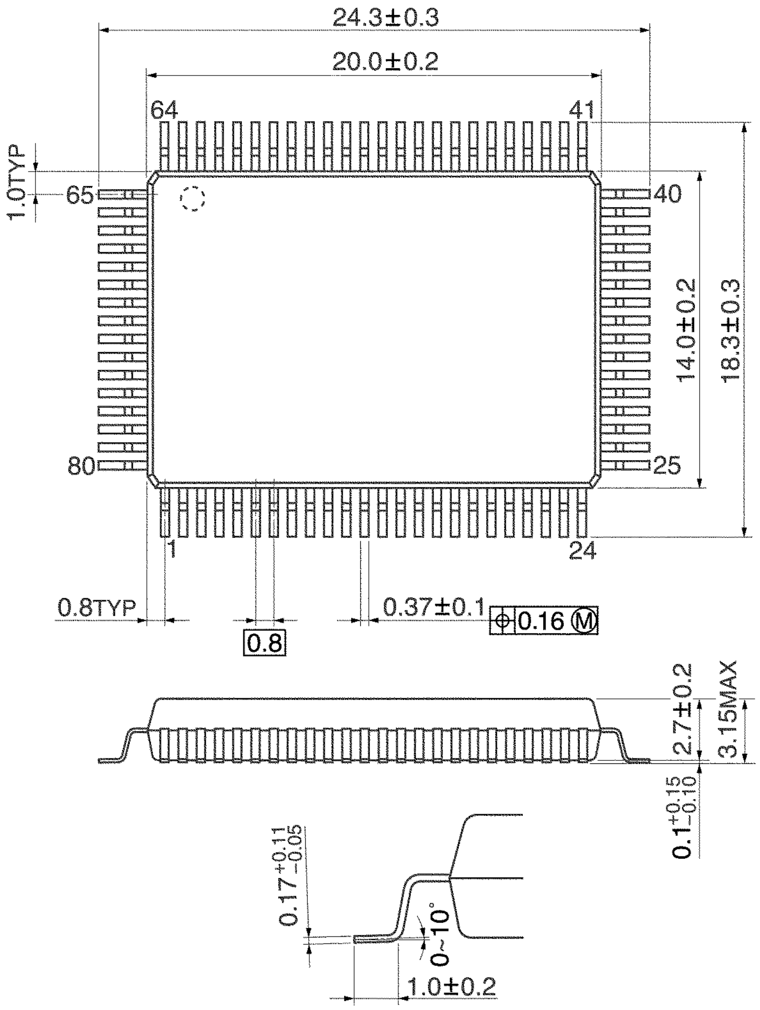
*: Don't care

ACB Application Circuit



Package Dimensions

QFP80-P-1420-0.80F Unit: mm



Weight: 1.6 g (typ.)

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