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# CDMA and FM (AMPS) I/Q Filter

**Preliminary Information** 

DS4724 - 3.1 May 1998

The JUPITER circuit is designed for use in dual band and dual mode mobile phones (CDMA/AMPS) and meets the requirements for IS-95 when used with other chips from Mitel that form the Planet chipset. JUPITER is an active filter incorporating circuits for receiving both CDMA and FM (AMPS).

#### **FEATURES**

- Low Power and Low Voltage Operation with a Sleep Mode
- Integrated CDMA and FM Filter with Wide Dynamic Range
- Low Inband Gain Ripple Performance and Good I/Q Matching for the Filter

# **ABSOLUTE MAXIMUM RATINGS**

Supply voltage, V <sub>CC MAX</sub>	-0.7V to $+5.3V$
Operating temperature, T <sub>OP</sub> (at pins)	-30°C to+70°C
Storage temperature, T <sub>STG</sub> (ambient)	-40°C to +150°C
Junction temperature	-30°C to +125°C
CMOS input logic high, V <sub>IH</sub>	V <sub>CC</sub> +0·6V (Max.)
CMOS input logic low, VIL	-0.6V (Min.)
Maximum input voltage at all pins	-0.6V to V <sub>CC MAX</sub> $+0.6V$

## **ORDERING INFORMATION**

JUPITER-1/KG/NP1S

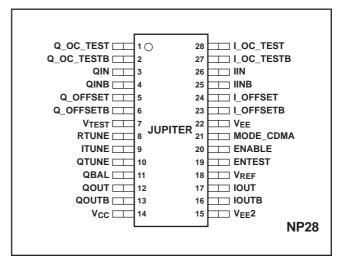


Fig. 1 Pin connections - top view

## **ESD PROTECTION**

All pins are protected against electrostatic discharge to both supplies. At least 2kV protection is provided to MIL-STD-883D Method 3015.7 (human body model).

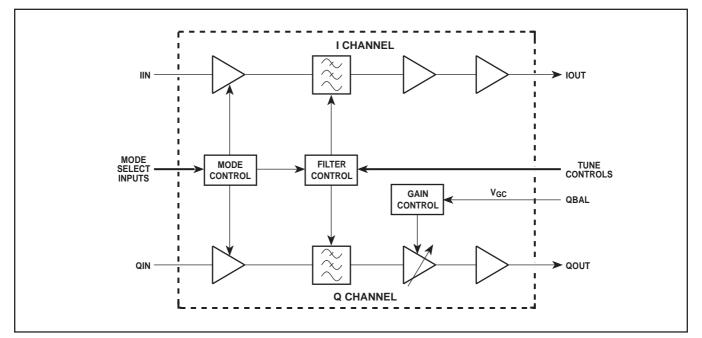


Fig. 2 Simplified block diagram

#### **CIRCUIT DESCRIPTION**

The block diagram of the JUPITER filter is shown in Fig. 3. Two tunable active low-pass gyrator filters are designed with balanced I/Q inputs and outputs.

#### **CDMA MODE**

In CDMA mode the filter (F1 on Fig. 3) is a 7th order 0.1dB ripple continuously tunable elliptic type with the corner frequency tuned to 690kHz for best stop band attenuation and minimal phase error (in the overall system). Variable gain stages after the filter provide the gain control capability. Overall, each of the CDMA I/Q channels has 45dB nominal voltage gain with the Q channel having  $\pm 2dB$  gain adjustment range. Separate I/Q frequency tuning functions are built into the device.

#### **FM MODE**

In FM mode the same filter is used; however, the biasing is designed such that the current density in the transconductor cells is reduced by a factor of 46, changing the filter's cutoff frequency to 15kHz. The filter characteristic of the main channel filter (gyrator filter) remains the same, i.e. a 0.1dB 7th order elliptic. In FM mode additional 2nd order Sallen and Key 0.1dB ripple Chebeyshev filters (F2) are included in the signal path prior to the gyrators. These improve the out-of-band blocking of the overall filter. Different amplifiers are used in FM mode to those used in CDMA mode to enable optimization of the gain distribution in FM mode for current consumption and dynamic range.

#### OPERATION

Signal inputs are DC coupled in both CDMA and FM modes. The device modes are selected by CMOS compatible logic signals as shown in Table 2. An external resistor should be connected between RTUNE and ground to set internal currents; a resistor with a tolerance of  $\pm 5\%$  and a temperature coefficient of less than 100ppm is recommended. V<sub>REF</sub> (pin 18) should be decoupled to V<sub>CC</sub> to give optimum supply rejection.

A test mode is provided for filter calibration. In this mode, a test signal is applied to the  $V_{\text{TEST}}$  input (pin 7) with ENTEST held high. The test mode is designed to interface with the PLUTO baseband processor, which can provide the test signal and I/QTUNE voltages and calibrates the filters using an internal auto calibration algorithm. The algorithm generates two test frequencies and calibrates the filters to give the correct attenuation at the upper frequency. The calibration is normally carried out in CDMA mode: the FM filter performance is scaled accordingly.

Pins are provided for DC offset control for I and Q channels (I\_OFFSET, I\_OFFSETB, Q\_OFFSET and Q\_OFFSETB). In typical operation, the I\_OFFSET/Q\_OFFSET pins would be controlled by a voltage derived from the baseband processor. However, it is also possible to minimise the DC offset using external components; this is primarily intended for test purposes. These feedback components between IOUT/QOUT and I\_OFFSET/Q\_OFFSET are shown in Fig. 4 but would not be used in the normal application

In test mode, these offset controls are disabled and the offsets are controlled using on-chip feedback. The loop filter for this feedback uses external 10nF capacitors on pins I\_OC\_TEST/B and Q\_OC\_TEST/B as shown in Fig. 4.

Pin	Name	I/O	Description			
1	Q_OC_TEST	Ι	Q channel offset control in test mode			
2	Q_OC_TESTB	I	Q channel offset control in test mode (balanced)			
3	QIN	Ι	Q channel CDMA/FM input.			
4	QINB	Т	Q channel CDMA/FM input (balanced)			
5	Q_OFFSET	Т	Q channel offset control			
6	Q_OFFSETB	Т	Q channel offset control (high gain mode)			
7	V <sub>TEST</sub>	Т	Test mode signal input for tuning operation			
8	RTUNE		Precision resistor for current definition (18k)			
9	ITUNE	I	I filter tuning control			
10	QTUNE	I	Q filter tuning control			
11	QBAL	I	Q channel gain adjust voltage, VGC			
12	QOUT	0	Q channel CDMA/FM output			
13	QOUTB	0	Q channel CDMA/FM output (balanced)			
14	V <sub>CC</sub>	Р	Supply			
15	V <sub>EE</sub> 2	Р	Ground			
16	IOUTB	0	I channel CDMA (balanced)			
17	IOUT	0	I channel CDMA			
18	V <sub>REF</sub>		Reference voltage decouple			
19	ENTEST	Ι	Mode control (see Table 2)			
20	ENABLE	Ι	Mode control (see Table 2)			
21	MODE_CDMA	Ι	Mode control (see Table 2)			
22	V <sub>EE</sub>	Р	Ground (substrate)			
23	I_OFFSETB	Ι	I channel offset control (high gain mode)			
24	I_OFFSET	Ι	I channel offset control			
25	IINB	I	I channel CDMA (balanced)			
26	IIN	Ι	I channel CDMA			
27	I_OC_TESTB	I	I channel offset control in test mode (balanced)			
28	I_OC_TEST	I	I channel offset control in test mode			

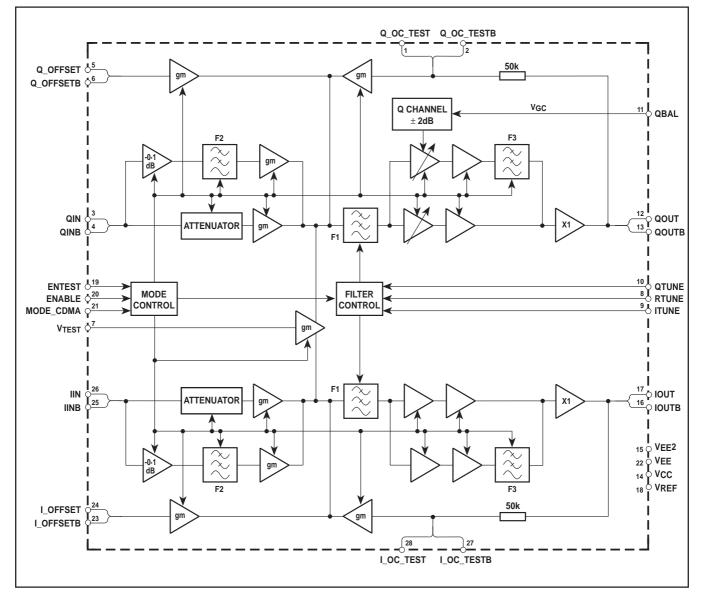


Fig. 3 Block diagram

Description	ENABLE	MODE_ CDMA	ENTEST	Comments	
Sleep mode	0	Х	1	All circuits powered down	
CDMA mode	1	1	0	Biasing and CDMA signal path on	
FM mode	1	0	0	Biasing and FM signal path on	
CDMA filter testmode	1	1	1	Biasing, CDMA test and CDMA signal path on, excluding input amplifier	
FM filter test mode	1	0	1	Biasing, FM test and FM signal path on, excluding input amplifier.	
Disallowed mode	0	Х	0	This is functionally the same as sleep mode but has higher I <sub>CC</sub> .	
				In sleep mode PLUTO applies a logic high to ENTEST	

Table 2 Truth table for mode control lines

# **ELECTRICAL CHARACTERISTICS**

The Electrical Characteristics are guaranteed over the following range of operating conditions unless otherwise stated (see Fig. 4 for test circuit):

 $T_{AMB} = -30^{\circ}C$  to  $+70^{\circ}C$ ,  $V_{CC} = 3V + 0.6V/-0.3V$ 

## **DC Characteristics**

		Value				
Characteristic	Min.	Min. Typ.		Units	Conditions	
General						
Supply voltage, V <sub>CC</sub>	2.7	3.0	3.6	V ∣ °C		
Operating temperature, T <sub>AMB</sub>	-30		+70	ۍ ۲		
Supply Current, I <sub>CC</sub>						
Sleep mode			0.15	mA	QBAL = ITUNE = QTUNE <0.5V	
FM mode		3.4	5.2	mA	QBAL = ITUNE = QTUNE = 1.2V	
CDMA mode		7.3	11.0	mA	QBAL = ITUNE = QTUNE = 1.2V	
Turn off time, CDMA/FM mode to Sleep mode		100		μs	I <sub>CC</sub> reduced to 10% of active value	
Mode Control Lines (CMOS)						
Input logic high, $V_{\rm IH}$	2.0		V <sub>CC</sub> +0.1	V	1	
Input logic low, V <sub>IL</sub>	-0.1		0.5	V		
Input high current I <sub>IH</sub>	-20		20	μA	All logic inputs	
Input low current, I <sub>IL</sub>	-20		20	μΑ	J	
Tune/Gain Control Lines						
DC level Input impedances:	0.5		2.0	V		
QBAL, ITUNE and QTUNE		200		kΩ	Referenced to on-chip ref. voltage (1.2V)	
I_OFFSET/B and Q_OFFSET/B		500		kΩ		
I/O DC Voltages						
Inputs IIN/B and QIN/B	$V_{cc} = 0.6$	V <sub>CC</sub> -0.4	$V_{cc} = 0.2$	V		
Outputs IOUT/B and QOUT/B		$V_{CC} - 1.4$		V		

# **ELECTRICAL CHARACTERISTICS**

# FM Mode AC Characteristics

All parameters are defined as differential unless otherwise stated

	Value					
Characteristic	Min.	Тур.	Max.	Units	Conditions	
Maximum input frequency			10	MHz		
Gain Characteristics I voltage gain $(A_V)$ IIN/B to IOUT/B Q voltage gain QIN/B to QOUT/B Q channel gain adjust Q channel gain control Gain variation over temperature and supply voltage Differential output amplitude balance, QOUT/QOUTB, IOUT/IOUTB	39 A <sub>V</sub> −1·5 ±2 −0·75	41 4.0	$ \begin{array}{r}     43 \\     A_V + 1.5 \\     8.0 \\     + 0.75 \\     \pm 0.25 \end{array} $	dB dB dB/V dB dB	External load = $50k\Omega//5pF$ QBAL = $1.2V$ QBAL = $0.5$ to $2V$ $V_{CC} = \pm 150mV$	
<b>Power Supply Rejection</b> In-band Out of band		10 0		dB dB	Measured at I/Q output frequency = 10kHz Measured at I/Q output frequency = 630kHz	
Noise Input referred		30	45	μVrms	Bandwidth = 10Hz to 5MHz. I and Q channels	
<b>1dB Compression</b> Output 1dB compression Out of band blocking signal causing 1dB compression of in-band signal	1.5	1.9		Vр-р	Frequency = 2kHz	
Blocking signal at 60kHz Blocking signal at 120kHz	266 266	380		mVrms mVrms mVrms	In-band frequency = 2kHz. All conditions 27°C only In-band frequency = 2kHz. All conditions	
Intermodulation Input referred intermodulation product		380 101 8·8		mVrms dBV μVrms	27°C only Unmodulated interferers 60kHz 75mVrms, 120kHz 7·5mVrms	
Filter Characteristic (Note 1) 3dB pass band Stop band attenuation 45kHz Stop band attenuation 60kHz to 10MHz I and Q bandwidth matching In-band gain ripple Group delay variation Average phase balance, I and Q channels	14.5 48 60	16·5 63 70 30	19.5 5 1.0 10	kHz dB dB % dBp-p μs deg	ITUNE = QTUNE = 1·2V } Frequency = 100Hz to 12·2kHz	
Offset Loop Correction Filter offset adjustment gain: I_OFFSET/Q_OFFSET I_OFFSET B/Q_OFFSETB Amplifier offset settling time: After power on	0.6	1.0 10 4.0	1.4	V/V V/V ms	Settling to within 5mV	
After CDMA to FM cycling Input Impedances			4.0	ms	Settling to within 5mV	
QIN/QINB and IN/INB	8.0	10	12	kΩ	Frequency = 2kHz	
Output Impedances QOUT/QOUTB and IOUT/IOUTB		1.0		kΩ	Frequency = 2kHz	

NOTE 1. Filter tuned in CDMA mode to -8dB at 720kHz

# **ELECTRICAL CHARACTERISTICS**

# CDMA Mode AC Characteristics

All parameters are defined as differential unless otherwise stated

	Value				Conditions	
Characteristic	Min. Typ. Max.		Units			
Maximum input frequency			10	MHz		
Gain Characteristics I voltage gain (A <sub>V</sub> ) IIN/B to IOUT/B Q voltage gain QIN/B to QOUT/B Q channel gain adjust Q channel gain control Gain variation over temperature and supply voltage Differential output amplitude balance, QOUT/QOUTB, IOUT/IOUTB	43 A <sub>V</sub> −1·5 ±2 −0·75	45 4.0	$47 \\ A_V + 1.5 \\ 8.0 \\ + 0.75 \\ \pm 0.25$	dB dB dB/V dB dB	External load = $50k\Omega//5pF$ QBAL = $1.2V$ QBAL = $0.5$ to $2V$ $V_{CC} = \pm 150mV$	
Power Supply Rejection In-band		20		dB	Measured at I/Q output frequency = 690kHz	
Noise Input referred		110		μVrms	Bandwidth = 10Hz to 5MHz. I and Q channels	
<b>1dB Compression</b> Output 1dB compression Out of band blocking signal causing 1dB	1.5	1.9		Vp-p	Frequency = 2kHz	
compression of in-band signal Blocking signal at 60kHz Blocking signal at 120kHz	110 110	150 150		mVrms mVrms mVrms mVrms	In-band frequency = 100kHz. All conditions 27°C only In-band frequency = 100kHz. All conditions 27°C only	
Intermodulation Input referred intermodulation product Input referred intermodulation product		-101 8·8 -101 8·8	-84-8 57 -84-8 57	dBV μVrms dBV μVrms dBV μVrms dBV μVrms	Unmodulated interferers 900kHz 24mVrms, 1700kHz 15mVrms 27°C only Unmodulated interferers 1·25MHz 24mVrms, 2·25MHz 15mVrms 27°C only	
Filter Characteristic (Note 1) ITUNE/QTUNE voltage	0.5	1.2	2.0	V	Tuning voltage to set filter to -8dB at 720kHz relative to 350kHz	
Pass band variation over supply and temperature variation I/Q tuning gain Stop band attenuation 900kHz to 10MHz I and Q bandwidth matching In-band gain ripple Average phase balance, I and Q channels	-3 50	0 240 55	+3 4 1.0 3	% kHz/V dB % dBp-p deg	$V_{CC} = \pm 150 \text{mV}$ ITUNE = QTUNE = 1.2V Frequency = 1kHz to 630kHz Frequency = 1kHz to 630kHz	

NOTE 1. Filter tuned to -8dB at 720kHz relative to 350kHz

Cont...

# ELECTRICAL CHARACTERISTICS CDMA Mode AC Characteristics (continued)

	Value					
Characteristic	Min.	Тур.	Max.	Units	Conditions	
Offset Loop Correction Filter offset adjustment gain: I_OFFSET/Q_OFFSET I_OFFSET B/Q_OFFSETB Amplifier offset settling time: After power on	1.2	2∙0 2∙0	2·8 10	V/V V/V ms	Settling to within 6mV	
After FM to CDMA cycling			4.0	ms	Settling to within 6mV	
Input Impedances QIN/QINB and IN/INB	8.0	10	12	kΩ	Frequency = 2kHz	
Output Impedances QOUT/QOUTB and IOUT/IOUTB		1.0		kΩ	Frequency = 2kHz	

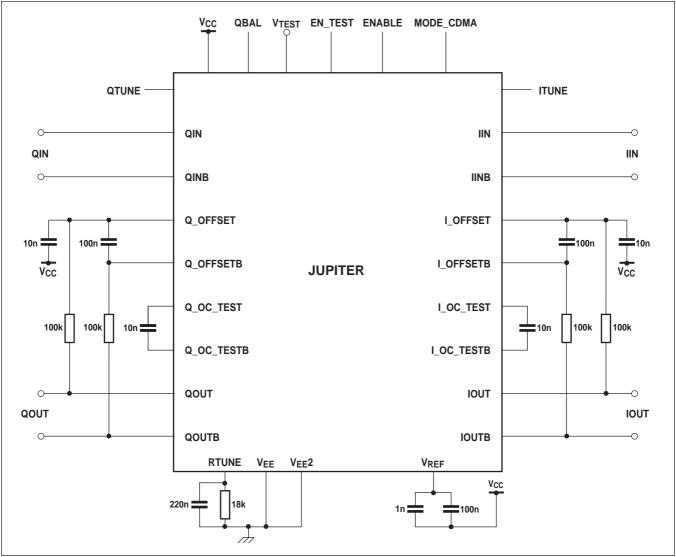
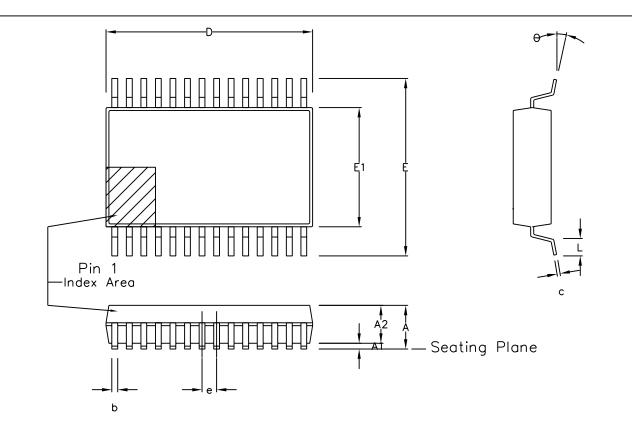


Fig. 4 Test circuit



Symbol		ol Dimer millimet			Altern. Dimensions in inches					
Symbol	MIN	Nominal	MAX		MIN	Nominal	MAX			
Α	1.70		2.00		0.067		0.079			
A1	0.05		0.20		0.002		0.008			
A2	1.65		1.85		0.065		0.073			
D	9.90		10.50		0.390		0.413			
E	7.40		8.20		0.291		0.323			
E1	5.00		5.60		0.197		0.220			
L	0.55		0.95		0.022		0.037			
е	0.0	65 BS	SC.		0.0	)26 B	SC.			
b	0.22		0.38		0.009		0.015			
С	0.09		0.25		0.004		0.010			
Θ	0°		8'		0°		ŝ			
	Pin features									
Ν	28									
Con	forms	s to J	IEDEC	MO	-150	AH Is	ss. B			

This drawing supersedes: -418/ED/51481/004 (Swindon/Plymouth)

# Notes:

- 1. A visual index feature, e.g. a dot, must be located within the cross-hatched area.
- 2. Controlling dimension are in millimeters.
- 3. Dimensions D and E1 do not include mould flash or protusion. Mould flash or protusion shall not exceed
- 0.20 mm per side. D and E1 are maximum plastic body size dimensions including mould mismatch.
  4. Dimension b does not include dambar protusion/intrusion. Allowable dambar protusion shall be 0.13 mm total in excess of b dimension. Dambar intrusion shall not reduce dimension b by more than 0.07 mm.

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