ADE-206-005B

HG29 Series
Bi-CMOS Gate Array

HITACHI

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Description

The HG29 series is the master sliced TTL level interface gate array using Hi-BiCMOS technology of super high speed and the low power dissipation. The HG29 series consists of the HG29A32 of 3,210 logic gates as fast as 0.45 ns at F.O. = 2, Al = 2 mm and the HG29M100 having 10,125 basic gates and a 4 k bits 3-port SRAM of variable bit-word configuration and fast access time, 10 ns (typ.). Both masters provide high speed input buffers of 0.7 ns, schmitt input buffers and high drive output buffers with an I_{OL} current capability of 24 mA. This means that the HG29 series is best suitable for applications requiring high-speed and high driving ability such as general purpose computers, work-stations and image processing systems. Especially, the HG29M100 can afford an LSI providing cash memories for testers, high-speed register files and the peripheral logics. Since device design is fully supported by a wide range of design automation (DA) tools and Hitachi's unique auto-diagnosis is available in HG29M100, high-quality customized LSIs can be developed in quick turn-around times.

Features

- Super high speed
  - Internal gate: 0.45 ns (typ.) at F.O. = 2, Al = 2 mm
  - Input buffer: 0.7 ns (typ.) at F.O. = 2, Al = 2 mm
  - Output buffer: 2.0 ns (typ.) at CL = 15 pF, 2.5 ns (typ.) at C_L = 50 pF
  - RAM t_{AA}*1: 10 ns (typ.)
- Low power dissipation
  - Internal gate: 0.24 mW (typ.) at 10 MHz
  - Input buffer: 2.0 mW (typ.) at 10 MHz
  - Output buffer: 5.5 mW (typ.) at C_L = 15 pF, 10 MHz
  - RAM: 100 mW (typ.) at 10 MHz
- Enhanced input/output functions
  - Schmitt-trigger input buffers
  - Selectable totem-pole, open-collector, or three-state outputs
  - Output buffer can construct logic functions ... save gates and gate stages
  - Selectable I_{OL} current drives of 12 mA or 24 mA. A 48 mA of I_{OL} buffer can be constructed by two output buffers.
- Simultaneously switching outputs
  - Max 24 outputs for HG29A32 and max 96 outputs for HG29M100 under the standard power supplies.
- Built-in RAM*1
  - 3-port (2 read, 1 write)
  - Variable bit-word construction
    9 bits × 512 words
    18 bits × 256 words
    36 bits × 128 words
  - Partial-write by each byte (9 bits)
- Auto-diagnosis function*1
  - Diagnosis test patterns are automatically generated by the DA system.
  - High speed macrocells for the diagnosis are constructed.
- Powerful design support
  - Design support by Design Center
  - Support for EWS (Mentor, Daisy, Valid) interface

Note: 1. HG29M100 only

Hitachi semiconductor

HG29 Series

Product Line Up

Series		HG29A32	HG29M100
Internal gate count (equivalent to 2 inputs NAND)		3,210 gates	10,125 gates
I/O buffers		102 pins	220 pins
Enhanced I/O	Schmitt-trigger input buffer	For all input buffers	
	I_{OL} = 24 mA output buffer	For all output buffers	
	I_{OL} = 48 mA output buffer*1	For all output buffers	
SRAM		—	Variable bit-word configuration { 9 bits × 512 words 18 bits × 256 words 36 bits × 128 words 3-port, partial-write
Package (figures in parentheses are usable I/O pin count)	FPG132	Available (102)	—
	QFP136	Available (102)	—
	PGA120	Available (102)	—
	PGA257	—	Available (220)
Power pin count (standard spec)		4 V_{CC} 6 GND	14 V_{CC} 22 GND

Absolute Maximum Ratings (Ta = 25°C)

Item	Symbol	Ratings	Unit
Supply voltage	V_{CC}	0 to +7.0	V
Input voltage	V_I	–0.6 to +5.5	V
Output voltage	Vo	–0.6 to +5.5	V
Storage temperature	Tstg	–65 to +150	°C

Recommended Operating Conditions

Item		Symbol	Min	Typ	Max	Unit
Supply voltage		V_{CC}	4.75	5.0	5.25	V
Output current	I_{OL} = 12 mA buffer	I_{OH}	—	—	–400	µA
	I_{OL} = 24 mA buffer				–15	mA
	I_{OL} = 12 mA buffer	I_{OL}	—	—	12	mA
	I_{OL} = 24 mA buffer				24	mA
Operating temperature		Topr	0	25	70	°C

Terminal Capacitance (Ta = 25°C, f = 1 MHz)

Item	Symbol	Min	Typ	Max	Unit
Terminal capacitance	C_T	—	—	10	pF

Note: This parameter is a sampled value and is not measured for all devices.

Electrical Characteristics

DC Characteristics (Ta = 0 to +70°C)

Item		Symbol	Min	Typ	Max	Unit	Test conditions
Input voltage		V_{IH}	2.2	—	—	V	V_{CC} = 4.75 to 5.25 V
		V_{IL}	—	—	0.8		V_{CC} = 4.75 to 5.25 V
		V_T+*1	—	1.6	2.2		V_{CC} = 5 V
		V_T-*1	0.5	0.7	—		V_{CC} = 5 V
		ΔV_T*1	0.4	0.9	—		V_{CC} = 5 V
Input clamp voltage		V_I	—	—	–1.5	V	V_{CC} = 4.75 V, I_{IN} = –18m A
Output voltage	I_{OL} = 12 mA buffer	V_{OH}	2.7	—	—	V	V_{CC} = 4.75 V, I_{OH} =–0.4mA
	I_{OL} = 24 mA buffer		2.0				V_{CC} = 4.75 V, I_{OH} = -15mA
	I_{OL} = 48 mA buffer*2		2.0				V_{CC} = 4.75 V, I_{OH} = -30mA
	I_{OL} = 12 mA buffer	V_{OL}	—	—	0.5	V	V_{CC} = 4.75 V, I_{OL} = 12 mA
	I_{OL} = 24 mA buffer				0.5		V_{CC} = 4.75 V, I_{OL} = 24 mA
	I_{OL} = 48 mA buffer*2				0.5		V_{CC} = 4.75 V, I_{OL} = 48 mA

DC Characteristics (Ta = 0 to +70°C) (cont)

Item		Symbol	Min	Typ	Max	Unit	Test conditions
Input current		I_I	—	—	1	mA	V_{CC} = 5.25 V, V_I = 5.5 V
		I_{IH}	—	—	20	µA	V_{CC} = 5.25 V, V_I = 2.7 V
		I_{IL}	—	—	–400	µA	V_{CC} = 5.25 V, V_I = 0.4 V
Output current		I_{OH}*3	—	—	100	µA	V_{CC} = 5.25 V, V_{OH} = 5.5 V
Output short-circuit current	I_{OL} = 12 mA buffer	I_{OS}	–40	—	–140	mA	V_{CC} = 5.25 V
	I_{OL} = 24 mA buffer		–40	—	–140		V_{CC} = 5.25 V
	I_{OL} = 48 mA buffer*2		–80	—	–280		V_{CC} = 5.25 V
Off-state output current		I_{OZH}*4	—	—	20	µA	V_{CC} = 5.25 V, V_O = 2.7 V
		I_{OZL}*4	—	—	-20		V_{CC} = 5.25 V, V_O = 0.4 V
Supply current		I_{CC}	—	*5	typ × 1.5	mA	V_{CC} = 5.25 V

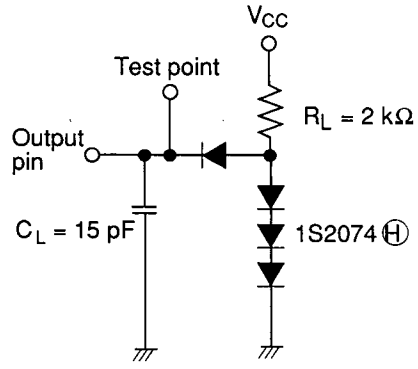
Notes: 1. Applies to schmitt input buffer
2. Using double-buffer technology
3. Applies to open-collector output buffer
4. Applies to three-state output buffer
5. Depends on the gate count

AC Characteristics (V_{CC} = 4.75 to 5.25 V, Ta = 0 to +70°C)

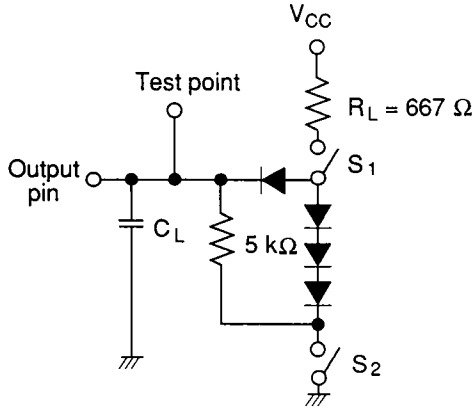
Item			Symbol	Min	Typ	Max	Unit	Test Circuit	Test conditions
Internal Gate Delay Time			t_{pd}	—	0.45	0.90	ns	—	F.O. = 2, Al = 2 mm
Input Buffer Delay Time			t_{pd}	—	0.7	1.4		—	F.O. = 2, Al = 2 mm
Output Buffer Delay Time	Totem-pole		t_{pd}	—	1.9	3.8		1	C_L = 15 pF, R_L = 2 kΩ
	Three-state	Normal input	t_{pd}	—	2.8	5.6		2	
		L, H to Z	t_{PLZ}, t_{PHZ}	—	5.8	11.6			
		Z, to L, H	t_{PZL}, t_{PZH}	—	4.0	8.0			
	Open-collector		t_{pd}	—	7.1	14.2		3	C_L = 15 pF, R_L = 2 kΩ

Test circuts

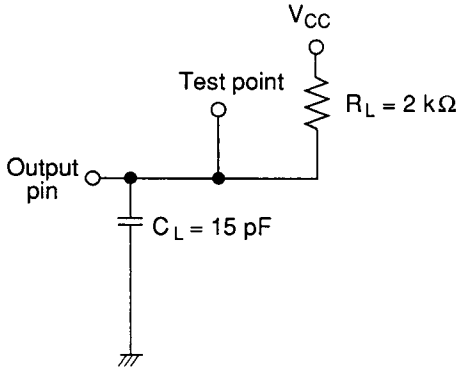
1.



2.

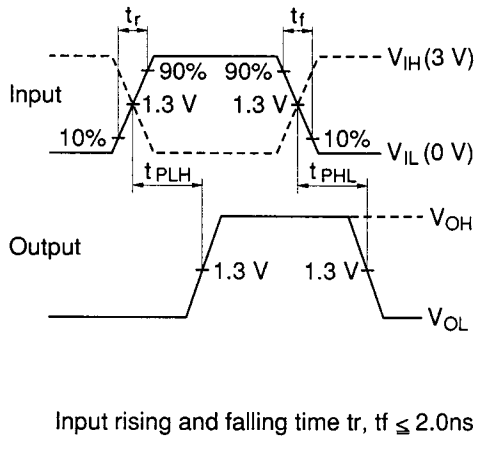


3.

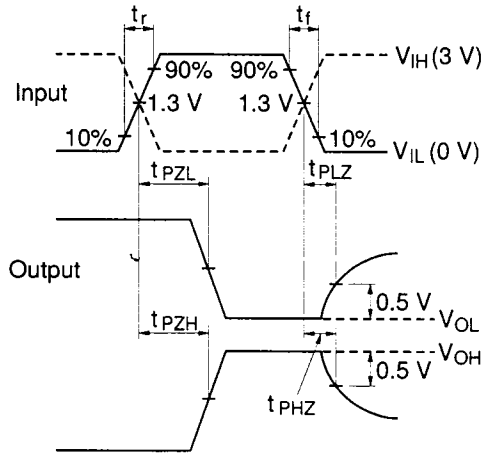


	t_{pd}	t_{PLZ}	t_{PHZ}	t_{PZL}	t_{PZH}
C_L	45pF	5pF	5pF	45pF	45pF
S_1	ON	ON	ON	ON	OFF
S_2	ON	ON	ON	OFF	ON

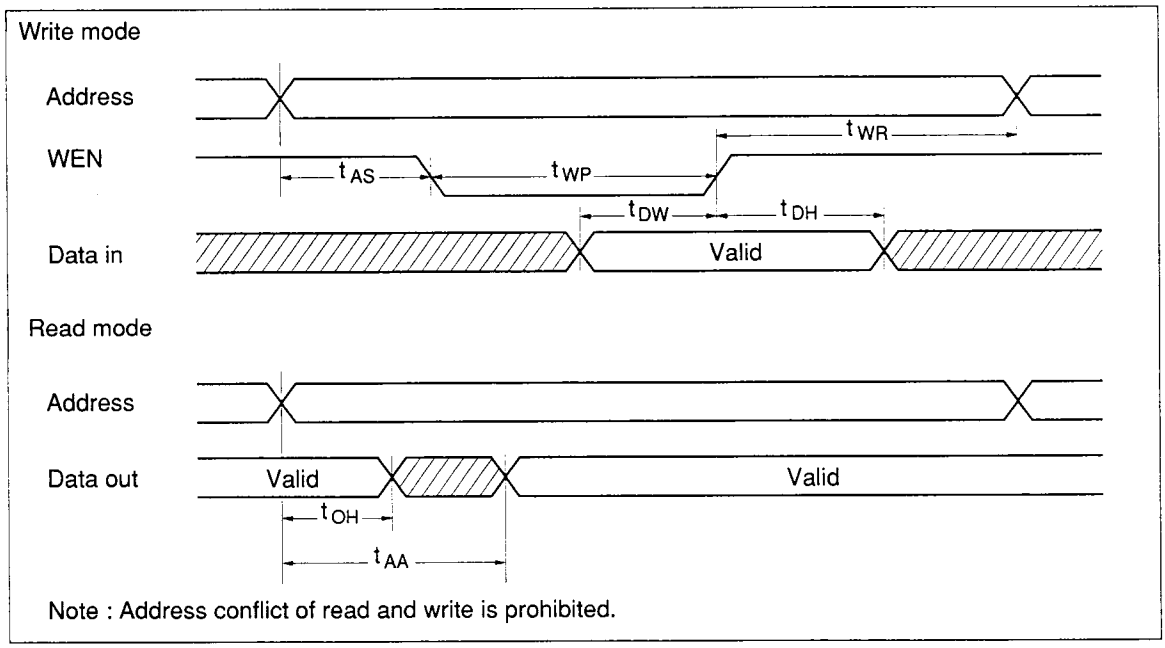
Input/output Waveforms



Input rising and falling time tr, tf ≦ 2.0ns



RAM Characteristics (Applies to HG29M100 only)

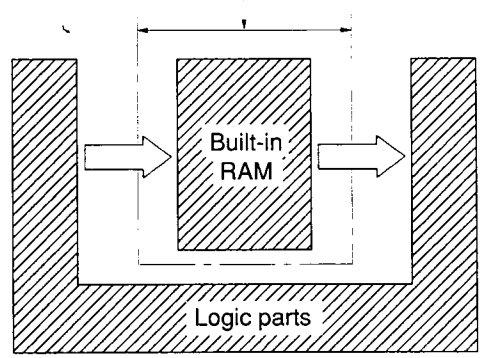


Note : Address conflict of read and write is prohibited.

Specifications

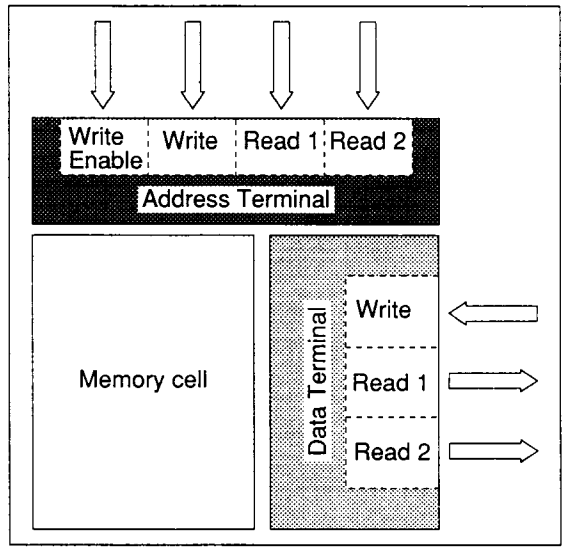
	Parameter	Symbol	Min	Max	Unit
Write mode	Address setup time	t_{AS}	9	—	ns
	Write pulse width	t_{WP}	4	—	
	Address hold time	t_{WR}	7	—	
	Data setup time	t_{DW}	5	—	
	Data hold time	t_{DH}	7	—	
Read Mode	Address access time	t_{AA}	—	20	
	Data valid time	t_{OH}	0	—	

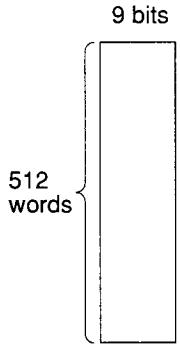
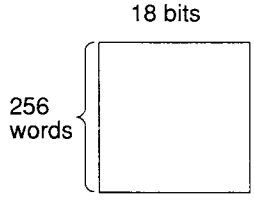
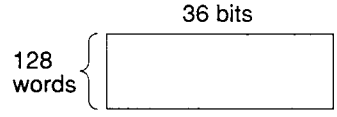
(Note) The above timing & spec are those of between terminals of a RAM cell, as well as another macrocell.



Built-in RAM

The HG29M100 has a 3-port RAM as shown in right on a chip. Since the READ port and the WRITE port are independently structured, it's possible to READ and WRITE in a cycle with the timing in page 5. The bit-word structure is variable and the following three types are selectable.



Macrocell Name		RAM09	RAM18	RAM36
Bits × Words		9 bits × 512 words	18 bits × 256 words	36 bits × 128 words
Total Bits		4,608 bits	4,608 bits	4,608 bits
Cell Structure				
Terminal Counts	Address	9 terminals × 3 = 27	8 terminals × 3 = 24	7 terminals × 3 = 21
	Data	9 terminals × 3 = 27	18 terminals × 3 = 54	36 terminals × 3 = 108
	Write-enable	1 terminal	2 terminals	4 terminals
Remarks		—	Partial-write available	Partial-write available

Allowable Package Power Dissipation

To guarantee operating characteristics, the device power dissipation must be less than the specified rated value. The table below gives the maximum allowable power dissipation ratings for device packages used in the HG29 series. These values may vary depending on supply voltage, ambient temperature, and cooling conditions. In the event of the LSI power dissipation exceeding the stipulated values, please contact Hitachi for remedial consultation.

HG29 Series Package Maximum Allowable Power Dissipation

Wind Speed (m/s)			No wind	1	2	3	5
Maximum allowable power dissipation (mW)	HG29A32	FPG-132	1,800	2,400	2,700	2,900	3,250
		QFP-136	1,280	1,570	1,830	2,030	2,390
		PGA-120	2,100	2,600	3,000	3,250	3,600
	HG29M100	PGA-257	2,550	3,500	4,050	4,450	4,750

Development Flow

Customer-manufacturer interfacing can be carried out via the following standard methods.

Logic-Schematic Interface (Figure 1)

In this method of interfacing, the customer provides the logic schematics and test pattern vectors in Hitachi-readable format. The user-defined design data is input to a workstation capable of generating a schematic output, which is then used to inspect and verify logic circuitry. A logic simulator and timing checker are used to check device operation, supported by a fault simulator that searches out undetectable faults. The next step is the automatic placement and routing of the logic, followed by verification of critical path propagation delay times based on the results of the post-layout routing data. After the user-defined design has been confirmed error free, Hitachi prepares the photomasks and test magnetic tapes used to manufacture the working samples.

Since only the metal wiring need be implemented on the pre-prepared uncommitted wafer samples, device engineering samples can be developed in very quick turn around times. Once checked and verified against the user-defined test patterns, the finished samples are shipped to the user for approval.

Logic File Interface

In the logic file interfacing method, the customer performs various simulations on in-house EWS or simulators, or on Hitachi DA workstations, and then submits the completed logic file to one of Hitachi's design plazas (DESCs). After the device operation has been validated at the DA plaza, the tasks remaining are similar to those of the logic schematic interface, right up to shipment of the working samples to the customer.

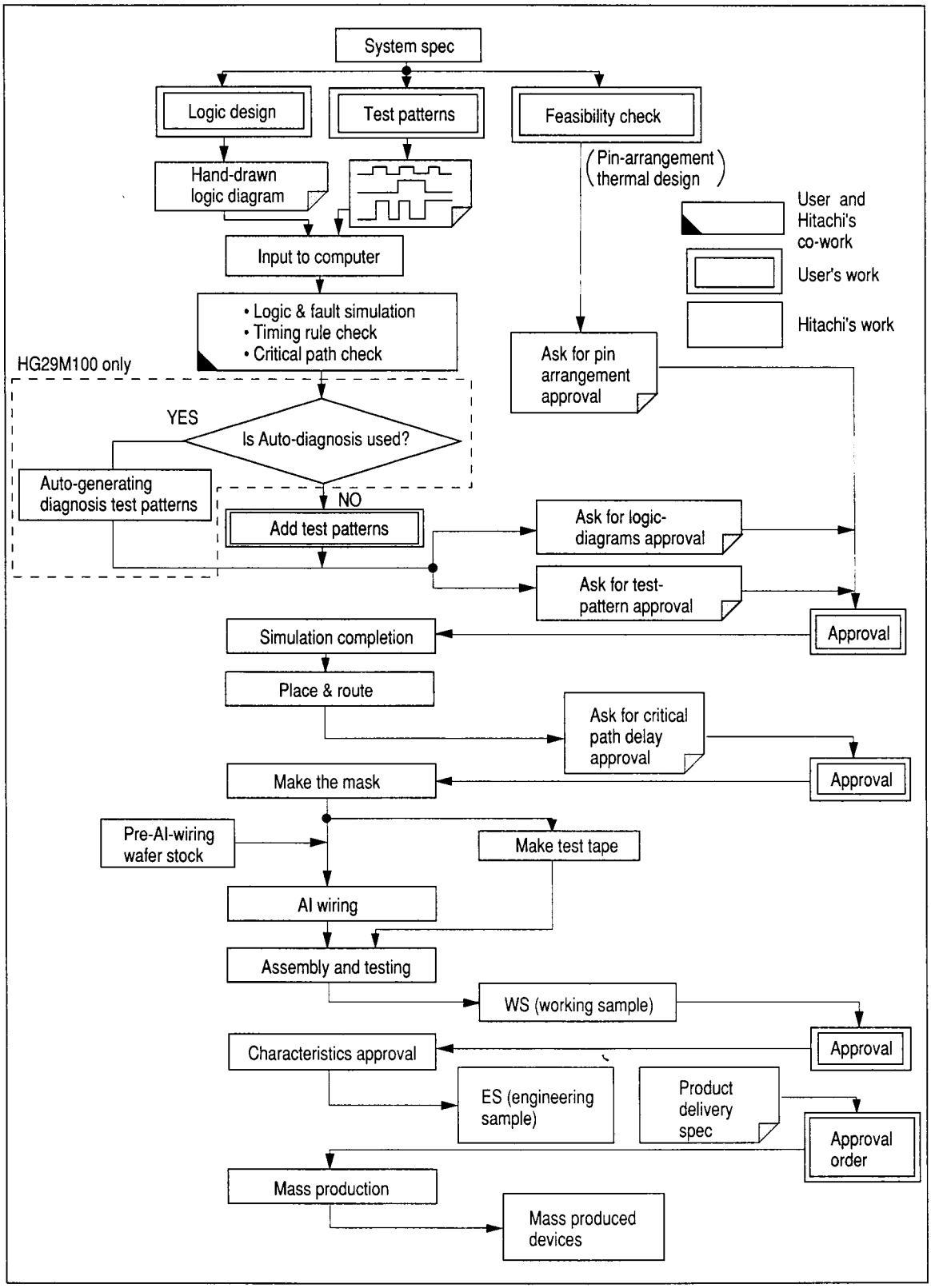


Figure 1 Logic Diagrams Interface

Power Dissipation Calculation

The power dissipation of an HG29 series gate array device is determined by used internal gates, input buffers, output buffers RAMs, load capacitance and operating frequency. Using the values defined in the macrocell library, the typical power dissipation is calculated as follows.

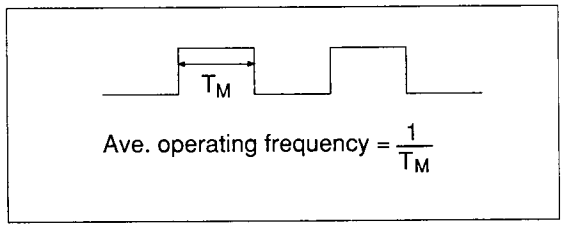
Internal Gate

Macro power dissipation = operating frequency (MHz) × ($P_O + P_{\Delta C} \times C_L$)
Where the loading capacitance, C_L, calculated as the same way as delay time, is given by

C_L = standard wiring capacitance*1 × ΣFanOut + 0.11 × ΣLV

Note: 1. 0.19/Fan out for HG29A32
0.27/Fan out for HG29M100

Here, the operating frequency is the frequency at the output of each respective macro, and is given as twice the clock frequency.



Input Buffer

Macro power dissipation = P_{DC} + operating frequency (MHz) × ($P_O + P_{\Delta C} \times C_L$)

Output Buffer

Macro power dissipation = P_{DC} + operating frequency (MHz) × ($P_O + P_{\Delta C} \times C_L$) + $V_{OL} \times I_{OL}$ × Duty (L) + ($V_{CC} - V_{OH}$) × I_{OH} × Duty (H)

Where the Duty(L) and Duty(H) denote the percentage of output level being low and high respectively.

RAM (HG29M100 only)

RAM power dissipation = operating frequency (MHz) × ($P_O + P_{\Delta C} \times C_L$)

The total power dissipation is given as sum of the dissipated power of each macro. The maximum value can be estimated 1.5 times of typical value roughly.

Delay Time Calculations

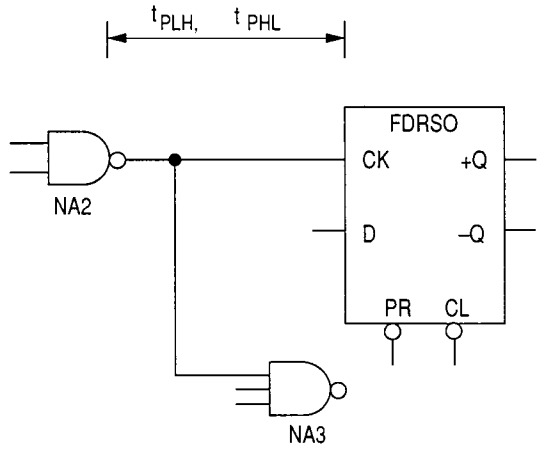
When designing logic circuitry, it is necessary to calculate signal propagation times through the circuit to verify that critical path delay times are within the desired values. The propagation delay time for the HG29 series is calculated using the following equations based on the t_{OLH}, t_{OHL}, R_{SLH}, R_{SHL}, and LV parameters as defined in the macrocell library.

t_{PLH} (typ.) = $t_{OLH} + R_{SLH} \times (\Sigma Ci + \Sigma Cl)$
t_{PHL} (typ.) = $t_{OHL} + R_{SHL} \times (\Sigma Ci + \Sigma Cl)$

Where, ΣCi (ΣCi = 0.11 pF × ΣLV) is the total input capacitance, and ΣCl is the total wiring capacitance, calculated on the basis of 0.19 pF per fanout for HG29A32 or 0.27 pF per fanout for HG29M100. The DA software tools provided should be used to calculate the pre- and post-layout delay times. Figure 2 shows an example of a delay time calculation.

For AC characteristics, the following maximum and minimum values are guaranteed using the typical calculated values:

Maximum value = typical value × 2.0
Minimum value = typical value × 0.5



NA2 t_{OLH} = 0.31 ns, t_{OHL} = 0.33 ns

R_{SLH} = 0.22 kΩ , R_{SHL} = 0.22 kΩ

NA3 (C_I = 0.11 pF × 1)

→ LV of NA3

FDRS0 (C_I = 0.11 pF × 2)

→ LV of FDRS0 (CK terminal)

(HG29A32)

Output rise time t_{PLH} = 0.31 ns + 0.22 kΩ × $\left(\frac{0.11\text{ pF} \times (1+2)}{\Sigma C_I} + \frac{0.19\text{ pF} \times 2}{\Sigma C_I}\right)$ = 0.47 ns

Output fall time t_{PHL} = 0.33 ns + 0.22 kΩ × (0.11 pF × (1 + 2) + 0.19 pF × 2) = 0.49 ns

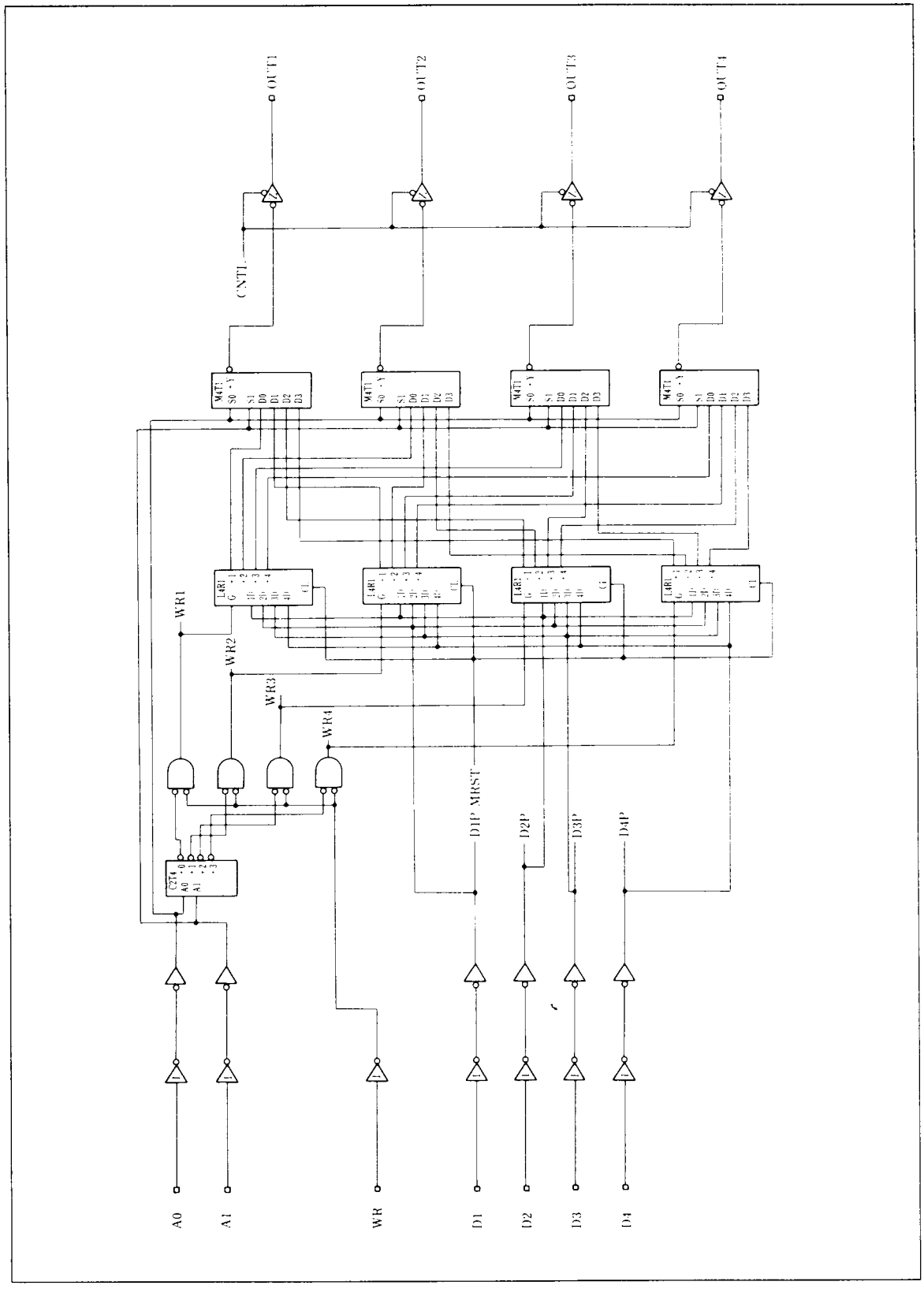
(HG29M100)

Output rise time t_{PLH} = 0.31 ns + 0.22 kΩ × $\left(\frac{0.11\text{ pF} \times (1+2)}{\Sigma C_I} + \frac{0.27\text{ pF} \times 2}{\Sigma C_I}\right)$ = 0.50 ns

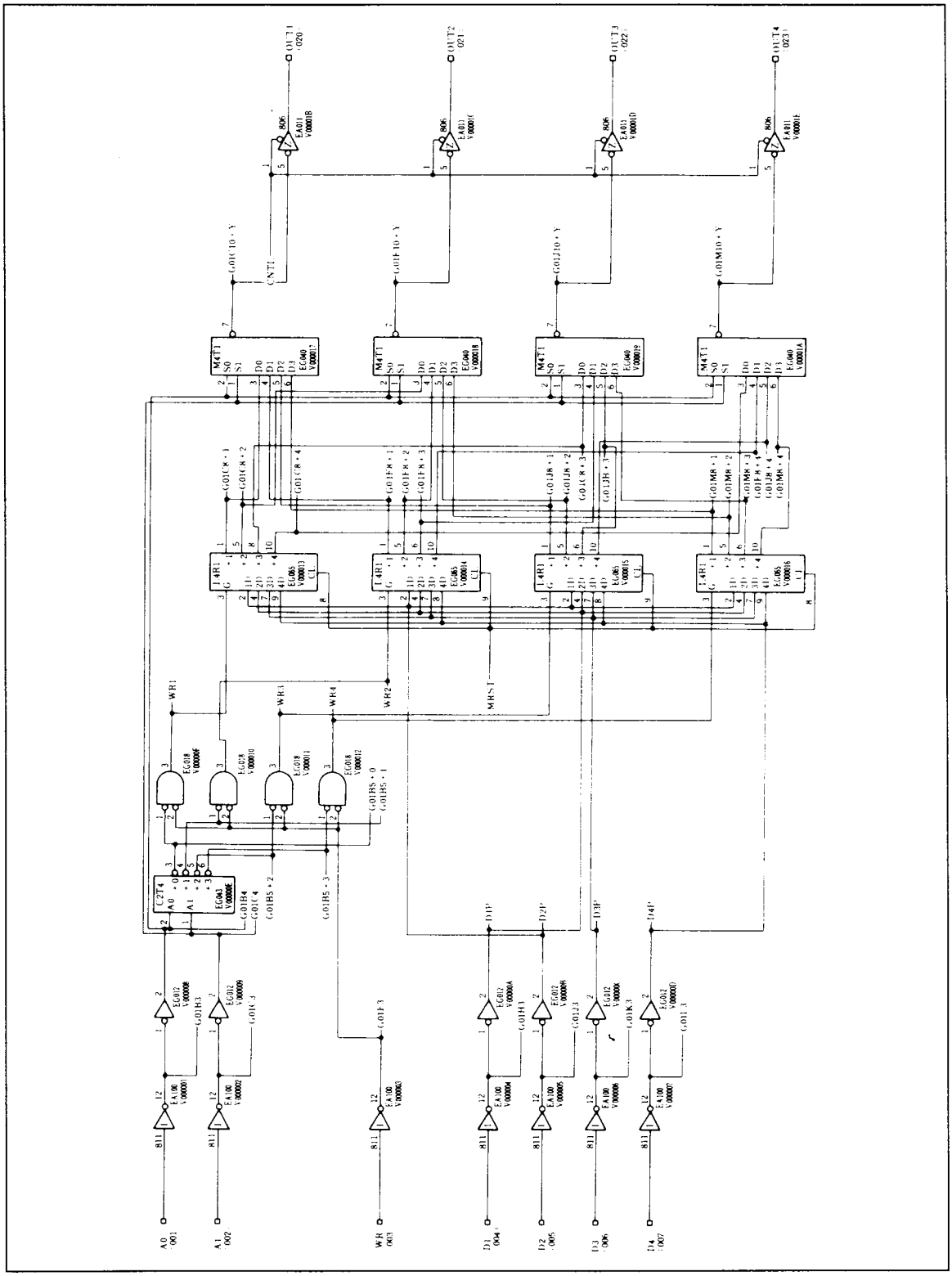
Output fall time t_{PHL} = 0.33 ns + 0.22 kΩ × (0.11 pF × (1 + 2) + 0.27 pF × 2) = 0.52 ns

Figure 2 Delay Time Calulation

Template Drawn Schematic (CLIF)



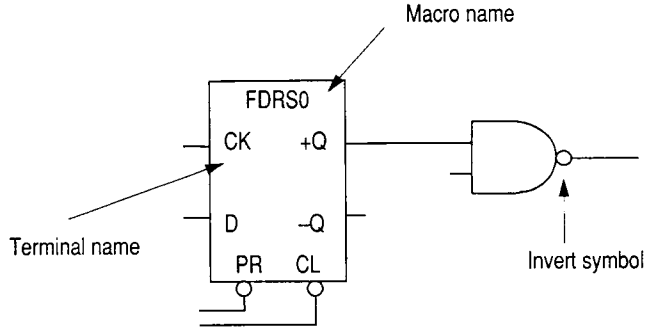
Computer-Generated Schematic (CLIF)



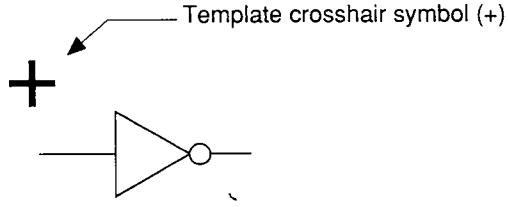
Logic Schematic Entry

No.	Item	Rules
1	Standard schematic drafting form	The standard A3 Hitachi shematic drafting form should be used as the circuit logic drawing medium
2	Usable characters	1. A total of 38 alphanumeric characters, including the uppercase letters A–Z, numeric characters 0–9, and plus (+) and minus (–) signs, should be used in schematic naming conventions. Character heights should be 2 to 3 mm or larger. 2. Care should be taken regarding the annotation of the more easily misinterpreted characters, indicated as follows:
3	Logic symbols	1. Logic symbols should be drawn using the logic template provided by Hitachi. 2. Each schematic logic symbol should include the following information, as required: a. Macro name (FDRS0, etc.) b. Terminal name (CK, D, PR, CL, etc.) c. Invert symbol (o)

Alphanumerics	D	I	J	O	U	Z	7
Notaton	Ð	*i*	*j*	Ō	*u*	Z̄	7



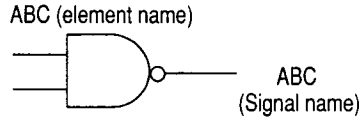
3. Schematic logic symbols should be drawn by first aligning the template crosshairs with the drawing sheet coordinate intersections.



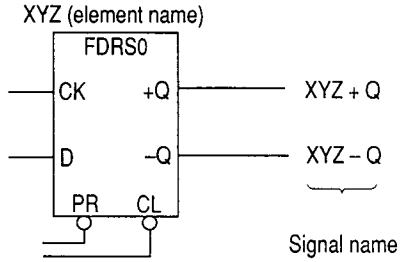
4. Logic symbols should be drawn with inputs to the left and outputs to the right. Signals should propagate in a left to right direction.

Table 3 Drawing Logic Diagrams (cont)

No.	Item	Rules
4	Signal and element naming conventions	1. LSI input/output signal names must begin with an alphabetic letter, and not exceed 8 characters in length. 2. Similarly, element and internal signal names must begin with an alphabetic letter, and not exceed 14 characters in length. 3. Different naming conventions can be used for the element name and output signal name of a macrocell. The following naming conventions, however, make it easier in searching for signal names during fault simulations. a. For macrocells with only one output, the name of the element should be assigned to the output signal (see figure 1).



b. For macrocells with two or more outputs, the element name with suffixed output name should be assigned to the output signal (see figure 2).



4. For macrocells not easily defined, the combined use of the logic symbol cell coordinates and schematic page number provide a convenient method of pinpointing the position of a symbol within a complex logic circuit schematic. In the example shown in figure 3, the logic symbol in the cell at schematic coordinates P2, C3 (that is, logic symbol at coordinate intersection C, 3 on Page 2), is assigned the element name C0302, and the output signal name C0302.

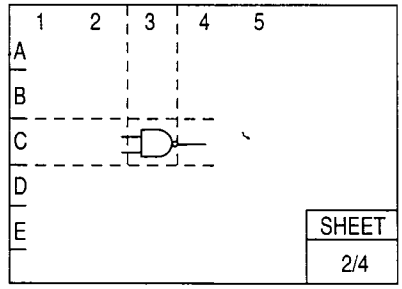


Table 3 Drawing Logic Diagrams (cont)

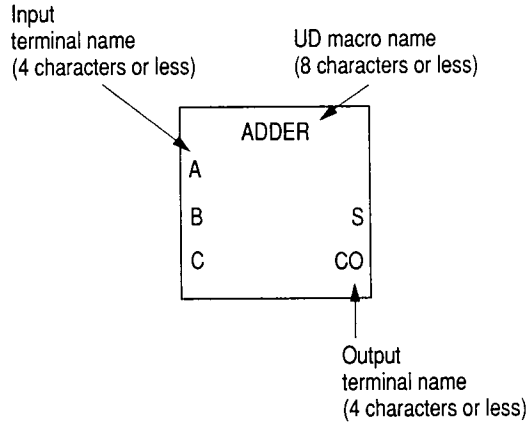
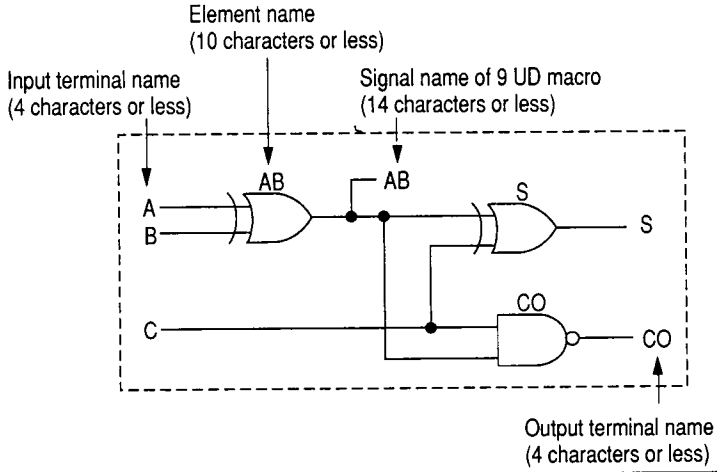
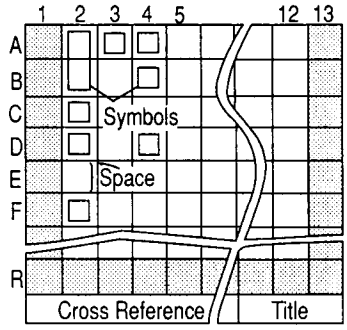
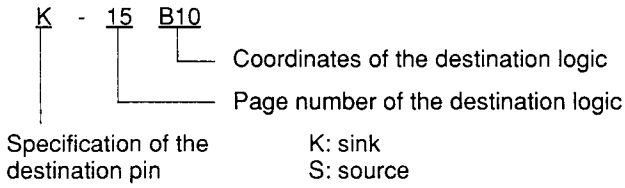
No.	Item	Rules
5	Hierarchical design (UD macro)	Logic blocks required for repeated use should be defined by the customer. These blocks are termed user-defined (UD) macros. 1. Names applicable to UD macro inputs and outputs should not exceed 4 characters in length. 2. The signal names applicable to normal macros forming UD macros should be defined within a naming field of 14 characters, and element names defined within 10 characters. 3. UD macro names should be defined within a naming field of 8 characters. The alphanumeric minus sign (–), however, must not be used in the UD naming definition. 4. The width of a UD macro symbol is determined by the A-size designation marked on the template, and its height is drawn in proportion to the number of input or output lines (whichever is the greater) applicable to the logic function. The UD macros described above can be used in exactly the same way as the standard logic primitives and macros defined in the Hitachi macrocell library. The deeper a macro is located within a hierarchically-structured block, the longer its signal names become. Therefore, it is recommended that element and signal names described within each hierarchical level be limited to 8 characters or less.  

Table 3 Drawing Logic Diagrams (cont)

No.	Item	Rules
6	Signal lines	1. LSI input and output signals should be represented using small graphical boxes, with the pin numbers defined in square brackets. 2. The number of signals connecting at a single node must not exceed three lines. 
7	Symbol placement	1. Signal flow should propagate through the logic from left to right. 2. The placement of logic symbols in columns 1 and 13, and row R (shaded areas) is prohibited. 3. To guarantee a path for signal routing, avoid placing symbols in five or more consecutive rows. 4. Placement of symbols that extend into row R is prohibited. 
8	Cross Reference	1. If a signal line extends over two or more computer-generated logic schematics, the following information is automatically provided in the lower left of the schematic: 

Test Patterns

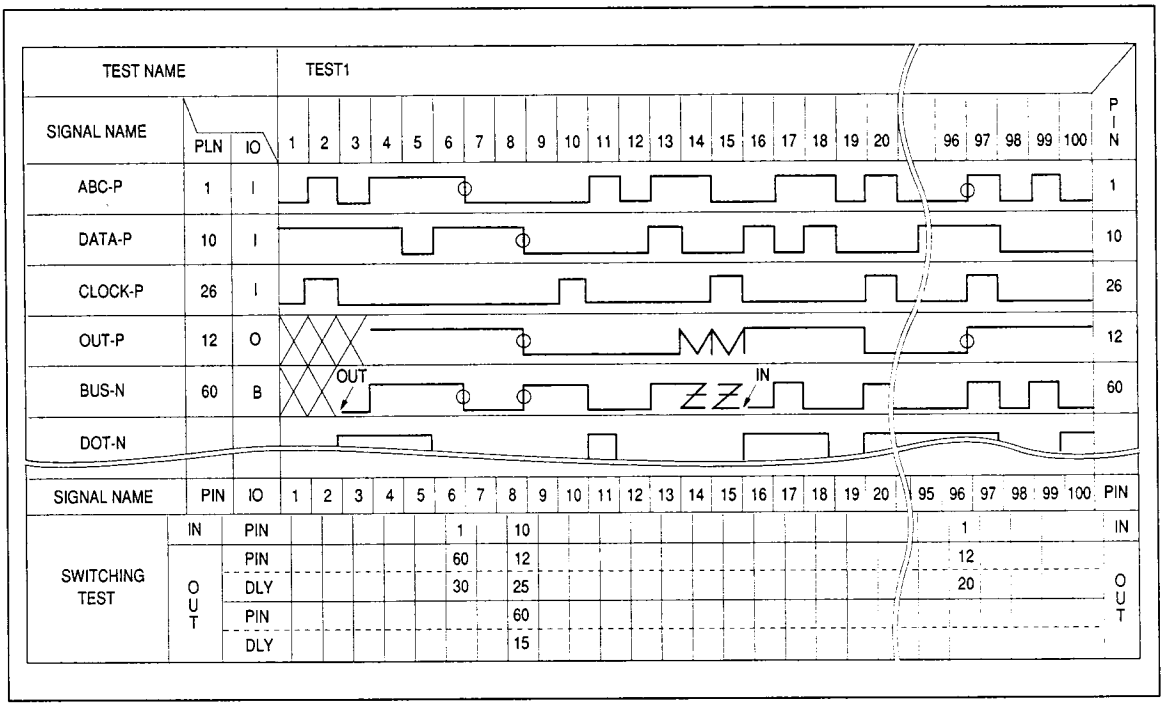
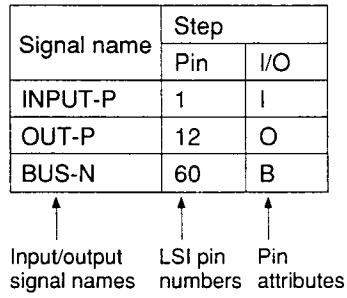
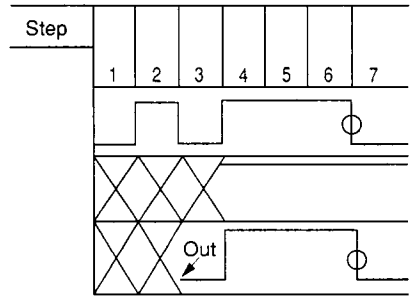


Figure 4 Test Pattern Extract

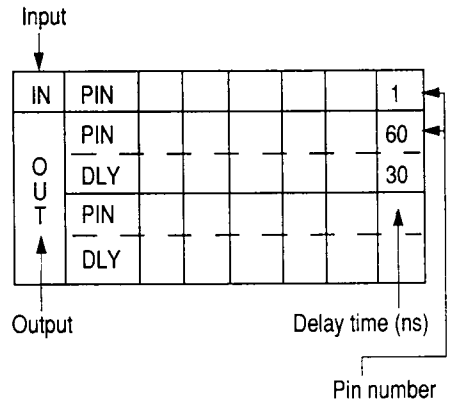
Table 4 Test Pattern Descriptions

No.	Item	Rules	Example of Description
1	Partitioning test patterns	Test patterns should be partitioned in accordance with the contents of the tests, and a unique name suitably assigned to each group Note. Flip-flops should be initialized first in the group which enables the simulation to start at the beginning of each test group.	Note: Dividing test patterns into partitioned groups makes it easier to analyze any inconsistencies that may exist between the logic schematics and test patterns via the results of logic simulation.
2	Entering test pattern names, sequence numbers, and page numbers	Enter test pattern names, sequence numbers, and page numbers in the designated columns at the top of the test pattern form.	TEST - F - 1/0 The first field TEST1 refers to the test pattern name (Up to 8 alphanumeric characters). The second field F refers to the sequence number (Up to 34 pin names can be entered on a single test pattern coding sheet. If more than 34 signal names are required, then depending on the number of sheets used, assign the letter F, S, T, U, or H to the first, second, third, fourth or fifth sheets, respectively). The final field 1/10 refers to the form page number (Slashed page numbering is required if the number test patterns for one block extends over several form sheets. If one page is used to complete the set of test patterns, number the page 1/E).

Table 4 Test Pattern Descriptions (cont)

No.	Item	Rules	Example of Description
3	Entering I/O signal names, pin numbers, and pin attributes	Enter input/output signal names, pin numbers, input, output, and bidirectional I/O attributes in the designated column on the left-hand side of the test pattern coding form. 1. I/O signal names and pin numbers should conform with those in the logic schematic. 2. Input, output and bidirectional I/O attributes are classified by the letters I, O, and B, respectively. I = input O = output B = input and output 3. If the test patterns sequence takes up more than one page, make sure that the I/O signal names are kept consistent throughout all additional pages.	
4	Signal waveforms	Draw signal waveforms using the blue guide lines provided on the test pattern form. 1. Waveforms should be described in the NRZ (non-return-to-zero) format. An X indicates an indefinite state, and an M a don't care output. 2. Enter input and output waveforms with zero time delays between them. If, however, a time delay is required between the data signal and the clock signal, for example, as in the flip-flop setup time requirements, change the clock signal one step after the data signal. 3. Indicate the attributes of input and output pins using IN and OUT in the step where the waveform begins. 4. Enter the letter Z to indicate the high impedance state of a three-state output.	

Test Pattern Descriptions (cont)

No.	Item	Rules	Example of Description
5	Logic simulation	The user-defined test pattern coding sequences are also used for logic simulation. When the internal LSI signals need to be output for simulation results, draw up a list of all signal names.	
6	Precautions on test pattern coding	1. The total number of independent test patterns, containing initialization routines in the test pattern header, should not exceed 10. 2. The total number of steps for a complete set of test patterns, including the number of iterations of partitioned test pattern loops, should not exceed 10,000 steps.	
7	Entering propagation delay time	1. To indicate that the I/O is a test pin, tick the waveform with a check mark (√), and enter the input/output pin numbers in the designated columns at the bottom of the test pattern form. 2. Enter the propagation delay time in the designated column. 3. Signal switching (toggling) tests should not exceed 50 test transactions. If the number of applied tests should exceed 50 items, contact Hitachi prior to carrying out switching tests. 4. In a step where a switching test is defined, change only the input pin defined as a switching test pin.	

Logic Design Precautions

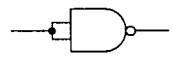
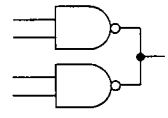
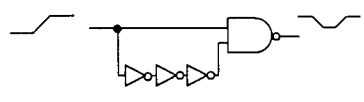
No.	Item	Rules	Example of Description
1	Prohibited structure	Strapping multiple inputs belonging to the same macro is prohibited.	
		Strapping multiple outputs belonging to similar gate species is prohibited.	
		Pulse-edge detection circuits, constructed using gated-delay macros, are prohibited.	

Table 5 Logic Design Precautions (cont)

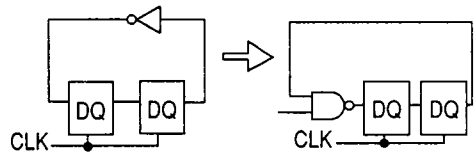
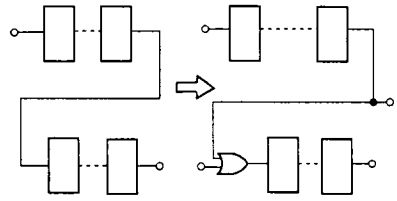
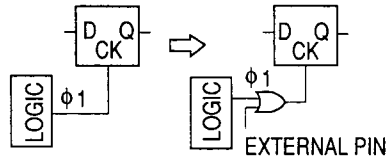
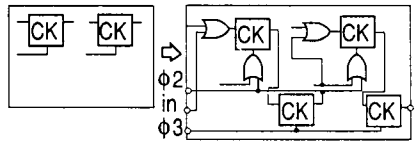
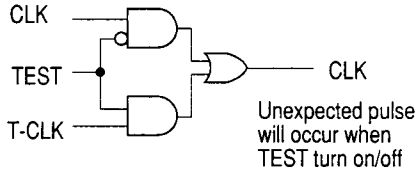
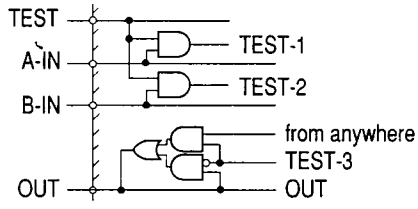
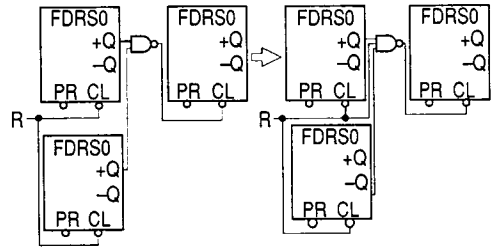
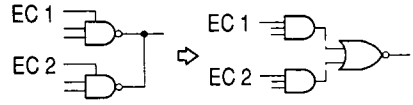
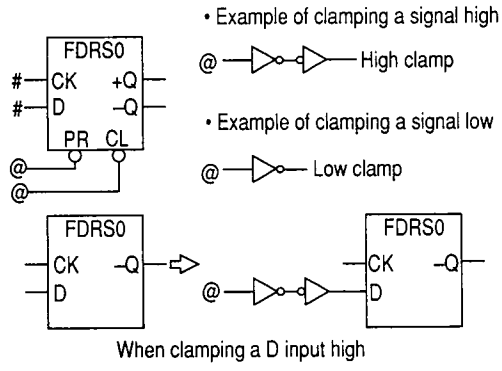
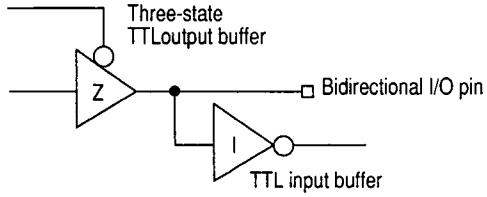
No.	Item	Rules	Example of Description
2	Suggestions for improved fault coverage	Use only logic circuits capable of being initialized via an external signal; circuits that have undefined initial states incapable of initialization must not be used.	
		Externally controllable pins should be inserted at suitable connection points in multistage concatenated shift registers and counters.	
		Externally controllable pins should be provided for circuits that use an input clock (f1) signal with a pulse width longer than that of the system clock.	
		The addition of test circuits*1 (such as LSSD) should be considered so that the state of internal latches can be set and detected via externally applied test signals and clocks. Note 1: Such as the Level Sensitive Scan Design Method (LSSD).	
		Signal timing sequences should be designed with due consideration given to the added test circuits. It is important to confirm that test circuits have sufficient switching speeds, and that no unexpected logic glitches occur during mode changeover. If the switching speed of the test circuit is insufficient, it may be necessary to temporally mask any output signals affected as a consequence.	
		The additional test circuits may mean a shortage of available test pins. The figure shows an example of additional test logic that generates several internally different test signals from a single test pin. Also, locations deep within the logic, as viewed from the output pin, are not easily checked from the outside. The figure shows how testing can be achieved by means of a normal output while in the test mode.	

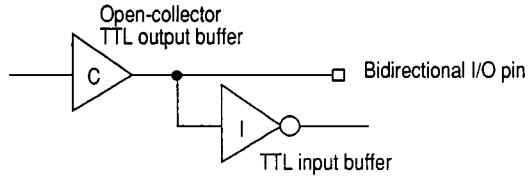
Table 5 Logic Design Precautions (cont)

No.	Item	Rules	Example of Description
3	Restriction on number of fanouts	FO ≤ 20 LV ≤ 40 FO: Number of load fanouts LV: Number of load gates connected to the input of the load macro (library defined)	
4	Precautions on the elimination of hazards	Circuits susceptible to the generation of hazard conditions (glitches and spikes) when reset signals are applied to flip-flops, for example, can give rise to system malfunction. To ensure error-free system operation, hazard-free circuit logic should be designed.	
5	Internal bus line design	Since Bi-CMOS gate arrays have no internal three-state elements, circuits should be designed using equivalent logic.	
6	Clamping floating and unused pins	Unused inputs must be clamped to the appropriate level designated by the symbol at each macrocell pin (@ indicates a high level, and # indicates a low level). Input pins designated with the & symbol, should not be left in an unused state. When clamping unused pins to levels that differ from the macrocell library signal level definitions, connect the pin to the required level via inverters.	
7	Simultaneously switching outputs	The number of simultaneously switching output buffers is given under the following standard specification: HG29A32: 24 pins max. HG29M100: 96 pins max.	If the number of simultaneously switching outputs exceeds the above specified limits, it may be necessary to add extra GND pins. Should this be deemed necessary, contact Hitachi for consultation on the addition of extra pins.

Macrocell Library Precautions

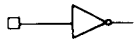
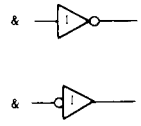
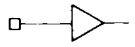
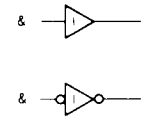
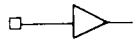
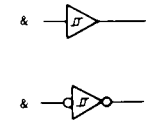
No.	Item	Instructions
1	Maximum packing density	For optimum placement and routing during automatic layout, the number of gates usable by the customer should be set at about 90% of the total gate density.
2	Macrocells	Logic should be designed in accordance with the predefined format using only the macros provided.
3	Bidirectional I/O pins	Input and output buffers may be combined to form a bidirectional pad. To construct a bidirectional I/O buffer, a three - state output buffer or an open - collector output buffer is used.



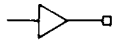
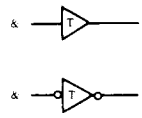
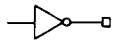
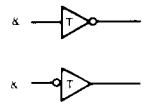
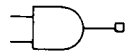
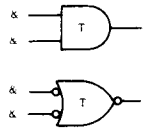
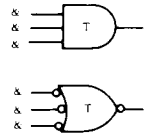
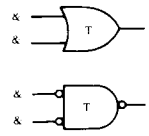
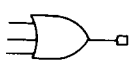
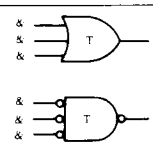
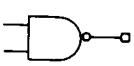
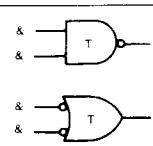
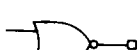
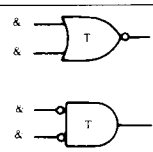


MACROCELL LIBRARY

1. Input Buffer

INPUT/OUTPUT	Macro: Function / Macro Name	Equivalent Circuit	Symbol	Propagation Delay Time: Output Rising t_{OLH} (ns)	Output Rising R_{SLH} (kΩ)	Output Falling t_{OHL} (ns)	Output Falling R_{SHL} (kΩ)	Power Dissipation: DC P_{DC} (mW)	AC (@ 1 MHz) P_O (mW)	AC (@ 1 MHz) $P_{\Delta C}$ (mW/pF)
INPUT	Inverter NA1I			0.53	0.13	0.70	0.15	1.81	0.013	0.012
	Buffer AN1I			0.79	0.13	0.66	0.15	1.81	0.023	0.012
	Schmitt input AN1S			1.28	0.13	1.22	0.15	1.32	0.029	0.012

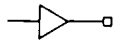
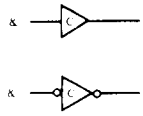
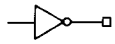
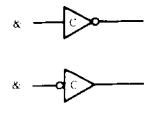
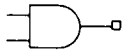
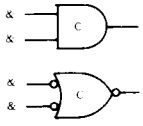
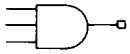
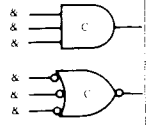
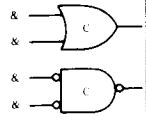
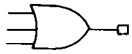
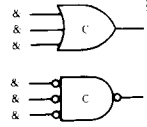
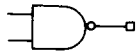
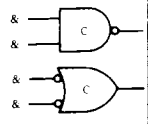
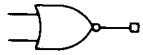
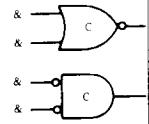
2. Output Buffer

Input/Output	Output Type	Macro: Function / Macro Name	Equivalent Circuit	Symbol		Propagation Delay Time: Output Rising t_{OLH} (ns)	Output Rising R_{SLH} (kΩ)	Output Falling t_{OHL} (ns)	Output Falling R_{SHL} (kΩ)	LV	Power Dissipation: DC P_{DC} (mW)	AC (@ 1 MHz) P_O (mW)	AC (@ 1 MHz) $P_{\Delta C}$ (mW/pF)
Output	Totem-pole	Buffer AN1OT			–	1.20	0.016	2.30	0.020	3	3.5	0.195	0.0068
		Inverter NA1OT			–	1.10	0.016	2.10	0.020	2	3.5	0.625	0.0068
		2 input AND AN2OT			–	1.40	0.016	2.30	0.020	2	3.5	0.285	0.0068
		3 input AND AN3OT			–	1.60	0.016	2.30	0.020	2	3.5	0.315	0.0068
		2 input OR OR2OT			–	1.35	0.016	2.70	0.020	2	3.5	0.175	0.0068
		3 input OR OR3OT			–	1.35	0.016	3.30	0.020	2	3.5	0.175	0.0068
		2 input NAND NA2OT			–	1.45	0.016	2.60	0.020	2	3.5	0.175	0.0068
		2 input NOR NR2OT			–	1.75	0.016	2.55	0.020	2	3.5	0.175	0.0068

Output Buffer (Continued)

Input/Output	Output Type	Macro: Function / Macro Name	Equivalent Circuit	Symbol		Propagation Delay Time: Output Rising t_{OLH} (ns)	Output Rising R_{SLH} (kΩ)	Output Falling t_{OHL} (ns)	Output Falling R_{SHL} (kΩ)	LV	Power Dissipation: DC P_{DC} (mW)	AC (@ 1 MHz) P_O (mW)	AC (@ 1 MHz) $P_{\Delta C}$ (mW/pF)
Output	3-state	Buffer AN1OZ			t_{pd}	1.39	0.016	2.93	0.021	3	3.5	0.295	0.0068
					t_{PZH}	2.05	0.018	–	–	1			
					t_{PZL}	–	–	3.85	0.025				
					t_{PLZ}	3.00	0.092	–	–				
					t_{PHZ}	–	–	7.00	0.825				
		Inverter NA1OZ			t_{pd}	1.26	0.016	2.53	0.021	2	3.5	0.675	0.0068
					t_{PZH}	2.05	0.018	–	–	1			
					t_{PZL}	–	–	3.90	0.025				
					t_{PLZ}	3.00	0.092	–	–				
					t_{PHZ}	–	–	7.00	0.825				
		2 input AND AN2OZ			t_{pd}	1.66	0.016	2.90	0.021	2	3.5	0.375	0.0068
					t_{PZH}	2.10	0.018	–	–	1			
					t_{PZL}	–	–	3.90	0.025				
					t_{PLZ}	3.00	0.092	–	–				
					t_{PHZ}	–	–	7.00	0.825				
		3 input AND AN3OZ			t_{pd}	1.85	0.016	2.86	0.021	2	3.5	0.430	0.0068
					t_{PZH}	2.10	0.018	–	–	1			
					t_{PZL}	–	–	3.87	0.025				
					t_{PLZ}	3.00	0.092	–	–				
					t_{PHZ}	–	–	7.00	0.825				
		2 input OR OR2OZ			t_{pd}	1.45	0.016	3.30	0.021	2	3.5	0.290	0.0068
					t_{PZH}	2.10	0.018	–	–	1			
					t_{PZL}	–	–	3.80	0.025				
					t_{PLZ}	3.00	0.092	–	–				
					t_{PHZ}	–	–	7.00	0.825				
		3 input OR OR3OZ			t_{pd}	1.52	0.016	3.80	0.021	2	3.5	0.290	0.0068
					t_{PZH}	2.10	0.018	–	–	1			
					t_{PZL}	–	–	3.85	0.025				
					t_{PLZ}	3.00	0.092	–	–				
					t_{PHZ}	–	–	7.00	0.825				
		2 input NAND NA2OZ			t_{pd}	1.60	0.016	3.16	0.021	2	3.5	0.290	0.0068
					t_{PZH}	2.05	0.018	–	–	1			
					t_{PZL}	–	–	3.90	0.025				
					t_{PLZ}	3.00	0.092	–	–				
					t_{PHZ}	–	–	7.00	0.825				
		2 input NOR NR2OZ			t_{pd}	1.80	0.016	3.00	0.021	2	3.5	0.290	0.0068
					t_{PZH}	2.05	0.018	–	–	1			
					t_{PZL}	–	–	3.90	0.025				
					t_{PLZ}	3.00	0.092	–	–				
					t_{PHZ}	–	–	7.00	0.825				

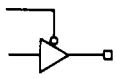
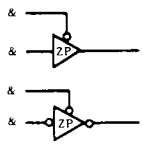
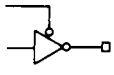
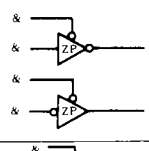
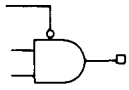
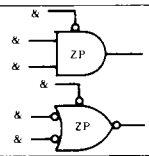
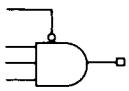
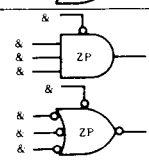
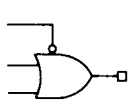
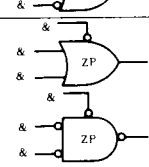
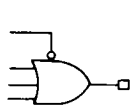
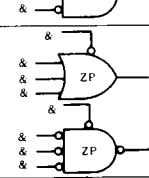
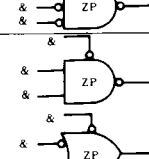
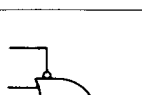
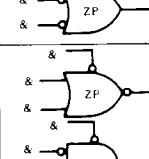
Output Buffer (Continued)

Input/Output	Output Type	Macro: Function / Macro Name	Equivalent Circuit	Symbol		Propagation Delay Time: Output Rising t_{OLH} (ns)	Output Rising R_{SLH} (kΩ)	Output Falling t_{OHL} (ns)	Output Falling R_{SHL} (kΩ)	LV	Power Dissipation: DC P_{DC} (mW)	AC (@ 1 MHz) P_O (mW)	AC (@ 1 MHz) $P_{\Delta C}$ (mW/pF)
Output	Open Collector	Buffer AN1OC			–	4.05	0.50	2.26	0.024	3	3.5	0.375	0.0095
		Inverter NA1OC			–	5.80	0.50	2.10	0.024	2	3.5	0.415	0.0095
		2 input AND AN2OC			–	4.57	0.50	2.27	0.024	2	3.5	0.375	0.0095
		3 input AND AN3OC			–	5.21	0.50	2.28	0.024	2	3.5	0.375	0.0095
		2 input OR OR2OC			–	4.12	0.50	2.59	0.024	2	3.5	0.375	0.0095
		3 input OR OR3OC			–	4.19	0.50	3.12	0.024	2	3.5	0.375	0.0095
		2 input NAND NA2OC			–	4.30	0.50	2.47	0.024	2	3.5	0.385	0.0095
		2 input NOR NR2OC			–	4.51	0.50	2.43	0.024	2	3.5	0.385	0.0095

Output Buffer (Continued)

Input/Output	Output Type	Macro: Function / Macro Name	Equivalent Circuit	Symbol		Propagation Delay Time: Output Rising t_{OLH} (ns)	Output Rising R_{SLH} (kΩ)	Output Falling t_{OHL} (ns)	Output Falling R_{SHL} (kΩ)	LV	Power Dissipation: DC P_{DC} (mW)	AC (@ 1 MHz) P_O (mW)	AC (@ 1 MHz) $P\Delta_C$ (mW/pF)
Output	Totem-pole	Buffer (I_{OL} = 24 mA) ANP1OT			–	1.40	0.016	2.30	0.020	3	7.0	0.275	0.0068
		Inverter (I_{OL} = 24 mA) NAP1OT			–	1.10	0.016	2.10	0.020	3	7.0	0.390	0.0068
		2 input AND (I_{OL} = 24 mA) ANP2OT			–	1.40	0.016	2.30	0.020	2	7.0	0.250	0.0068
		3 input AND (I_{OL} = 24 mA) ANP3OT			–	1.60	0.016	2.30	0.020	2	7.0	0.250	0.0068
		2 input OR (I_{OL} = 24 mA) ORP2OT			–	1.35	0.016	2.70	0.020	2	7.0	0.175	0.0068
		3 input OR (I_{OL} = 24 mA) ORP3OT			–	1.35	0.016	3.30	0.020	2	7.0	0.175	0.0068
		2 input NAND (I_{OL} = 24 mA) NAP2OT			–	1.45	0.016	2.60	0.020	2	7.0	0.175	0.0068
		2 input NOR (I_{OL} = 24 mA) NRP2OT			–	1.75	0.016	2.55	0.020	2	7.0	0.175	0.0068

Output Buffer (Continued)

Input/Output	Output Type	Macro: Function / Macro Name	Equivalent Circuit	Symbol		Propagation Delay Time: Output Rising t_{OLH} (ns)	Output Rising R_{SLH} (kΩ)	Output Falling t_{OHL} (ns)	Output Falling R_{SHL} (kΩ)	LV	Power Dissipation: DC P_{DC} (mW)	AC (@ 1 MHz) P_O (mW)	AC (@ 1 MHz) $P_{\Delta C}$ (mW/pF)
Output	3-state	Buffer (I_{OL} = 24 mA) ANP1OZ			t_{pd}	1.39	0.016	2.93	0.021	3	7.0	0.295	0.0068
					t_{PZH}	2.05	0.018	–	–	1			
					t_{PZL}	–	–	3.85	0.025				
					t_{PLZ}	3.00	0.092	–	–				
					t_{PHZ}	–	–	7.00	0.825				
		Inverter (I_{OL} = 24 mA) NAP1OZ			t_{pd}	1.26	0.016	2.53	0.021	3	7.0	0.675	0.0068
					t_{PZH}	2.05	0.018	–	–	1			
					t_{PZL}	–	–	3.90	0.025				
					t_{PLZ}	3.00	0.092	–	–				
					t_{PHZ}	–	–	7.00	0.825				
		2 input AND (I_{OL} = 24 mA) ANP2OZ			t_{pd}	1.66	0.016	2.90	0.021	2	7.0	0.375	0.0068
					t_{PZH}	2.10	0.018	–	–	1			
					t_{PZL}	–	–	3.90	0.025				
					t_{PLZ}	3.00	0.092	–	–				
					t_{PHZ}	–	–	7.00	0.825				
		3 input AND (I_{OL} = 24 mA) ANP3OZ			t_{pd}	1.85	0.016	2.86	0.021	2	7.0	0.430	0.0068
					t_{PZH}	2.10	0.018	–	–	1			
					t_{PZL}	–	–	3.87	0.025				
					t_{PLZ}	3.00	0.092	–	–				
					t_{PHZ}	–	–	7.00	0.825				
		2 input OR (I_{OL} = 24 mA) ORP2OZ			t_{pd}	1.45	0.016	3.30	0.021	2	7.0	0.290	0.0068
					t_{PZH}	2.10	0.018	–	–	1			
					t_{PZL}	–	–	3.80	0.025				
					t_{PLZ}	3.00	0.092	–	–				
					t_{PHZ}	–	–	7.00	0.825				
		3 input OR (I_{OL} = 24 mA) ORP3OZ			t_{pd}	1.52	0.016	3.80	0.021	2	7.0	0.290	0.0068
					t_{PZH}	2.10	0.018	–	–	1			
					t_{PZL}	–	–	3.85	0.025				
					t_{PLZ}	3.00	0.092	–	–				
					t_{PHZ}	–	–	7.00	0.825				
		2 input NAND (I_{OL} = 24 mA) NAP2OZ			t_{pd}	1.60	0.016	3.16	0.021	2	7.0	0.290	0.0068
					t_{PZH}	2.05	0.018	–	–	1			
					t_{PZL}	–	–	3.90	0.025				
					t_{PLZ}	3.00	0.092	–	–				
					t_{PHZ}	–	–	7.00	0.825				
		2 input NOR (I_{OL} = 24 mA) NRP2OZ			t_{pd}	1.80	0.016	3.00	0.021	2	7.0	0.290	0.0068
					t_{PZH}	2.05	0.018	–	–	1			
					t_{PZL}	–	–	3.90	0.025				
					t_{PLZ}	3.00	0.092	–	–				
					t_{PHZ}	–	–	7.00	0.825				

Output Buffer (Continued)

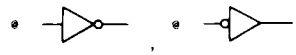
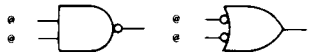
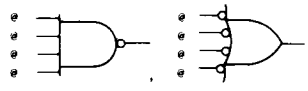
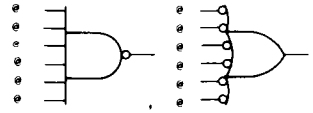
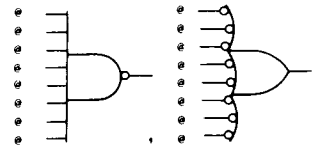
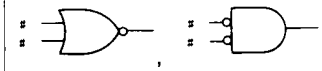
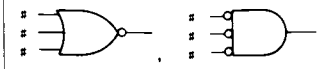
Input/Output	Output Type	Macro: Function / Macro Name	Equivalent Circuit	Symbol		Propagation Delay Time: Output Rising t_{OLH} (ns)	Output Rising R_{SLH} (kΩ)	Output Falling t_{OHL} (ns)	Output Falling R_{SHL} (kΩ)	LV	Power Dissipation: DC P_{DC} (mW)	AC (@ 1 MHz) P_O (mW)	AC (@ 1 MHz) $P_{\Delta C}$ (mW/pF)
Output	Open Collector	Buffer (I_{OL} = 24 mA) ANP1OC			–	4.05	0.50	2.26	0.024	3	7.0	0.375	0.0095
		Inverter (I_{OL} = 24 mA) NAP1OC			–	5.80	0.50	2.10	0.024	3	7.0	0.371	0.0095
		2 input AND (I_{OL} = 24 mA) ANP2OC			–	4.57	0.50	2.27	0.024	2	7.0	0.375	0.0095
		3 input AND (I_{OL} = 24 mA) ANP3OC			–	5.21	0.50	2.28	0.024	2	7.0	0.375	0.0095
		2 input OR (I_{OL} = 24 mA) ORP2OC			–	4.12	0.50	2.59	0.024	2	7.0	0.375	0.0095
		3 input OR (I_{OL} = 24 mA) ORP3OC			–	4.19	0.50	3.12	0.024	2	7.0	0.375	0.0095
		2 input NAND (I_{OL} = 24 mA) NAP2OC			–	4.30	0.50	2.47	0.024	2	7.0	0.385	0.0095
		2 input NOR (I_{OL} = 24 mA) NRP2OC			–	4.51	0.50	2.43	0.024	2	7.0	0.385	0.0095

Output Buffer (Continued)

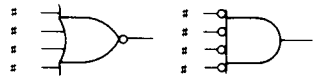
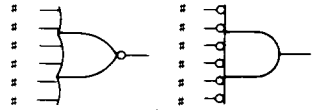
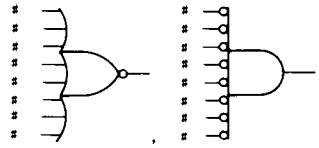
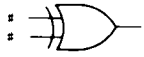
Input/Output	Output Type	Macro: Function / Macro Name	Equivalent Circuit	Symbol		Propagation Delay Time: Output Rising t_{OLH} (ns)	Output Rising R_{SLH} (kΩ)	Output Falling t_{OHL} (ns)	Output Falling R_{SHL} (kΩ)	LV	Power Dissipation: DC P_{DC} (mW)	AC (@ 1 MHz) P_O (mW)	AC (@ 1 MHz) $P_{\Delta C}$ (mW/pF)
Output	Totem-pole	Buffer * (I_{OL} = 48 mA) ANW1OT			—	1.40	0.008	2.30	0.010	6	14.0	0.550	0.0068
		Inverter * (I_{OL} = 48 mA) NAW1OT			—	1.10	0.008	2.10	0.010	6	14.0	0.780	0.0068
	3-state	Buffer * (I_{OL} = 48 mA) ANW1OZ			t_{ad}	1.39	0.008	2.93	0.011	6	14.0	0.590	0.0068
					t_{PZH}	2.05	0.009	—	—	2			
					t_{PZL}	—	—	3.85	0.013				
					t_{PLZ}	3.00	0.092	—	—				
					t_{PHZ}	—	—	7.00	0.825				
		Inverter * (I_{OL} = 48 mA) NAW1OZ			t_{ad}	1.26	0.008	2.53	0.011	6	14.0	1.350	0.0068
					t_{PZH}	2.05	0.009	—	—	2			
					t_{PZL}	—	—	3.90	0.013				
					t_{PLZ}	3.00	0.092	—	—				
					t_{PHZ}	—	—	7.00	0.825				
	Open Collector	Buffer * (I_{OL} = 48 mA) ANW1OC			—	4.05	0.50	2.26	0.012	6	14.0	0.750	0.0095
		Inverter * (I_{OL} = 48 mA) NAW1OC			—	5.80	0.50	2.10	0.012	6	14.0	0.742	0.0095

*On using these double buffers; refer to the HG29M100 design manual

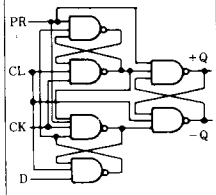
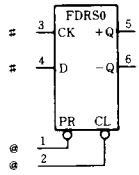
3. Gate

Macro			No. of equiv-alent gates	Propagation Delay Time				LV	Power Dissipation (@ 1 MHz)	
				Output Rising		Output Falling				
Function / Macro Name	Equivalent Circuit	Symbol		t_{OLH} (ns)	R_{SLH} (kΩ)	t_{OHL} (ns)	R_{SHL} (kΩ)		P_D (mW)	$P_{\Delta C}$ (mW/pF)
Inverter NA1			1	0.31	0.22	0.30	0.20	1	0.015	0.012
2 input NAND NA2			1	0.31	0.22	0.33	0.22	1	0.017	0.012
3 input NAND NA3			2	0.37	0.22	0.45	0.26	1	0.024	0.012
4 input NAND NA4			2	0.39	0.22	0.65	0.30	1	0.027	0.012
6 input NAND NA6			4	1.37	0.22	1.44	0.23	1	0.022	0.012
8 input NAND NA8			5	1.48	0.22	1.63	0.23	1	0.024	0.012
2 input NOR NR2			1	0.50	0.24	0.42	0.22	1	0.029	0.012
3 input NOR NR3			2	0.78	0.28	0.45	0.22	1	0.045	0.012

Gate (Continued)

Function / Macro Name	Macro: Equivalent Circuit	Macro: Symbol	No. of equivalent gates	Propagation Delay Time: Output Rising t_{OLH} (ns)	Output Rising R_{SLH} (kΩ)	Output Falling t_{OHL} (ns)	Output Falling R_{SHL} (kΩ)	LV	Power Dissipation (@ 1 MHz): P_Q (mW)	$P_{\Delta C}$ (mW/pF)
4 input NOR NR4			2	1.17	0.29	0.47	0.22	1	0.059	0.012
6 input NOR NR6			4	1.86	0.22	1.09	0.23	1	0.022	0.012
8 input NOR NR8			5	2.31	0.22	1.11	0.23	1	0.024	0.012
2 input EOR XR2			3	0.82	0.24	1.21	0.25	2	0.037	0.012
2 input ENOR XN2			3	0.82	0.23	1.23	0.24	2	0.048	0.012
Buffer Anl			2	0.65	0.17	0.55	0.18	2	0.029	0.012

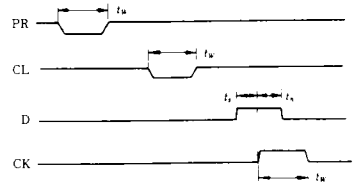
4. Flip-Flop

Function / Macro Name	Equivalent Circuit	Symbol	No. of equiva-lent gates	Terminal Name: Input	Terminal Name: Output	Propagation Delay Time: Output Rising t_{OLH} (ns)	Output Rising R_{SLH} (kΩ)	Output Falling t_{OHL} (ns)	Output Falling R_{SHL} (kΩ)	LV	Power Dissipation (@ 1 MHz): P_D (mW)	$P_{\Delta C}$ (mW/pF)
D Type Edge Triggered Flip-Flop			7	D		–	–	–	–	1	0.078	0.012
				PR	+Q	0.73	0.22	–	–			
					−Q	(CK = low)		1.06	0.27	3		
						(CK = high)		1.47	0.27			
				CL	+Q	(CK = low)		1.26	0.27			
						(CK = high)		1.74	0.27	3		
					−Q	0.78	0.22	–	–			
				CK	+Q	1.31	0.22	1.76	0.27	2		
					−Q	1.28	0.22	1.64	0.27			

Truth Table

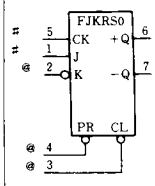
Input PR	CL	CK	D	Output +Q	−Q
L	H	×	×	H	L
H	L	×	×	L	H
L	L	×	×	H	H
H	H	↑	H	H	L
H	H	↑	L	L	H
H	H	L	×	$+Q_0$	$-Q_0$

Restriction in using



where
$t_W \geqq 2.5$ ns
$t_S \geqq 2.0$ ns
$t_H \geqq 0.4$ ns

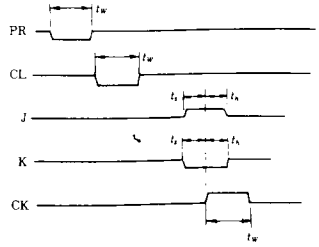
FDRS0

Function / Macro Name	Equivalent Circuit	Symbol	No. of equiva-lent gates	Terminal Name: Input	Terminal Name: Output	Propagation Delay Time: Output Rising t_{OLH} (ns)	Output Rising R_{SLH} (kΩ)	Output Falling t_{OHL} (ns)	Output Falling R_{SHL} (kΩ)	LV	Power Dissipation (@ 1 MHz): P_D (mW)	$P_{\Delta C}$ (mW/pF)
J-K Type Edge Triggered Flip-Flop			8	J		–	–	–	–	1	0.070	0.012
				K		–	–	–	–	1		
				PR	+Q	0.72	0.22	–	–			
					−Q	(CK = low)		1.24	0.27	3		
						(CK = high)		1.76	0.27			
				CL	+Q	(CK = low)		1.10	0.27			
						(CK = high)		1.90	0.27	3		
					−Q	0.80	0.22	–	–			
				CK	+Q	1.46	0.22	1.69	0.27	2		
					−Q	1.35	0.22	1.85	0.27			

Truth Table

Input PR	CL	CK	J	K	Output +Q	−Q
L	H	×	×	×	H	L
H	L	×	×	×	L	H
L	L	×	×	×	H	H
H	H	↑	L	H	$+Q_0$	$-Q_0$
H	H	↑	L	L	L	H
H	H	↑	H	H	H	L
H	H	↑	H	L	Toggle	
H	H	L	×	×	$+Q_0$	$-Q_0$

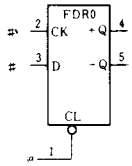
Restriction in using



where
$t_W \geqq 2.5$ ns
$t_S \geqq 3.0$ ns
$t_H \geqq 0.4$ ns

FJKRS0

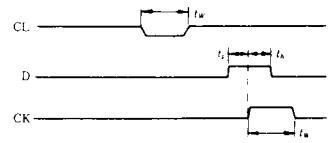
Flip-Flop (Continued)

Function / Macro Name	Equivalent Circuit	Symbol	No. of equivalent gates	Terminal Name		Propagation Delay Time: Output Rising t_{OLH} (ns)	Output Rising R_{SLH} (kΩ)	Output Falling t_{OHL} (ns)	Output Falling R_{SHL} (kΩ)	LV	Power Dissipation (@ 1 MHz) P_O (mW)	$P_{\Delta C}$ (mW/pF)
D Type Edge Triggered Flip-Flop			6	D		–	–	–	–	1	0.078	0.012
				CL	+Q	(CK = low)		1.26	0.27	3		
						(CK = high)		1.74	0.27			
					–Q	0.78	0.22	–	–			
				CK	+Q	1.31	0.22	1.63	0.27	2		
					–Q	1.12	0.22	1.64	0.27			

Restriction in using

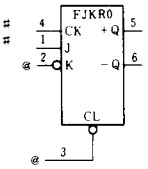
Truth Table

Input			Output	
CL	CK	D	+Q	–Q
L	x	x	L	H
H	↑	H	H	L
H	↑	L	L	H
H	L	x	$+Q_0$	$-Q_0$



where
$t_w \geqq 2.5$ ns
$t_s \geqq 2.0$ ns
$t_h \geqq 0.4$ ns

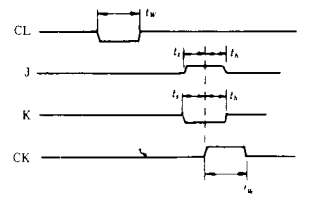
FDR0

Function / Macro Name	Equivalent Circuit	Symbol	No. of equivalent gates	Terminal Name		Propagation Delay Time: Output Rising t_{OLH} (ns)	Output Rising R_{SLH} (kΩ)	Output Falling t_{OHL} (ns)	Output Falling R_{SHL} (kΩ)	LV	Power Dissipation (@ 1 MHz) P_O (mW)	$P_{\Delta C}$ (mW/pF)
J-K Type Edge Triggered Flip-Flop			7	J		–	–	–	–	1	0.070	0.012
				K		–	–	–	–	1		
				CL	+Q	(CK = low)		1.10	0.27	3		
						(CK = high)		1.90	0.27			
					–Q	0.80	0.22	–	–			
				CK	+Q	1.46	0.22	1.63	0.27	2		
					–Q	1.19	0.22	1.85	0.27			

Restriction in using

Truth Table

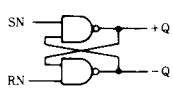
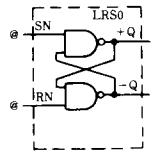
Input				Output	
CL	CK	J	K	+Q	–Q
L	x	x	x	L	H
H	↑	L	H	$+Q_0$	$-Q_0$
H	↑	L	L	L	H
H	↑	H	H	H	L
H	↑	H	L	Toggle	
H	L	x	x	$+Q_0$	$-Q_0$



where
$t_w \geqq 2.5$ ns
$t_s \geqq 3.0$ ns
$t_h \geqq 0.4$ ns

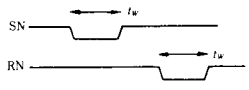
FJKR0

5. Latch

Function / Macro Name	Equivalent Circuit	Symbol	No. of equivalent gates	Terminal Name		Propagation Delay Time: Output Rising t_{OLH} (ns)	Output Rising R_{SLH} (kΩ)	Output Falling t_{OHL} (ns)	Output Falling R_{SHL} (kΩ)	LV	Power Dissipation (@ 1 MHz) P_D (mW)	$P_{\Delta C}$ (mW/pF)
Latch with Set/Reset			2	Input	Output							
				SN	+Q	0.55	0.22	–	–	1	0.038	0.012
					−Q	–	–	0.97	0.27			
				RN	+Q	–	–	0.97	0.27	1		
					−Q	0.55	0.22	–	–			

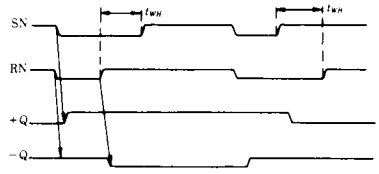
Restriction in using

1.



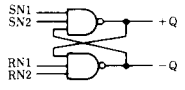
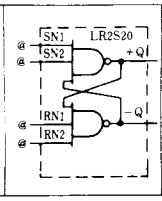
where
$t_W \geqq 2.5$ ns

2.



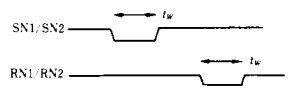
where
$t_{WH} \geqq 2.0$ ns

LRS0

Latch with Set/Reset												
			2	SN1/ SN2	+Q	0.66	0.22	–	–	1	0.050	0.012
					−Q	–	–	1.25	0.29			
				RN1/ RN2	+Q	–	–	1.25	0.29	1		
					−Q	0.66	0.22	–	–			

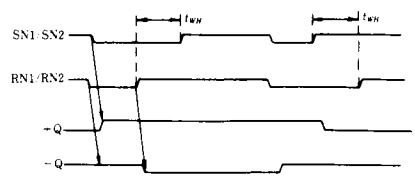
Restriction in using

1.



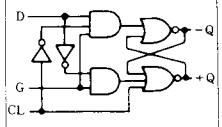
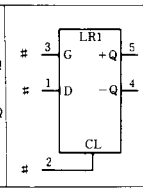
where
$t_W \geqq 2.5$ ns

2.



where
$t_{WH} \geqq 2.0$ ns

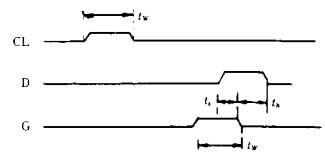
LR2S20

D Type Latch												
			5	D	+Q	2.08	0.28	1.22	0.24	2	0.128	0.012
					−Q	2.12	0.24	1.02	0.26			
				CL	+Q	–	–	0.60	0.24	2		
					−Q	1.66	0.24	–	–			
				G	+Q	2.07	0.28	0.88	0.24	2		
					−Q	1.84	0.24	0.79	0.26			

Truth Table

Input			Output	
CL	G	D	+Q	−Q
H	×	×	L	H
L	H	L	L	H
L	H	H	H	L
L	L	×	$+Q_0$	$-Q_0$

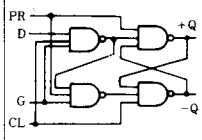
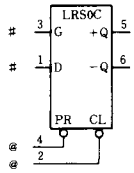
Restriction in using



where
$t_W \geqq 2.5$ ns
$t_S \geqq 3.0$ ns
$t_H \geqq 0.4$ ns

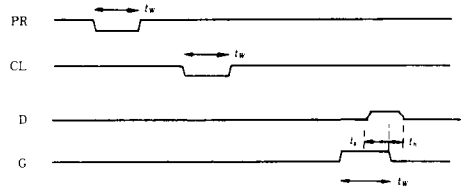
LR1

Latch (Continued)

Function / Macro Name	Macro: Equivalent Circuit	Macro: Symbol	No. of equivalent gates	Propagation Delay Time: Terminal Name Input	Terminal Name Output	Output Rising t_{OLH} (ns)	Output Rising R_{SLH} (kΩ)	Output Falling t_{OHL} (ns)	Output Falling R_{SHL} (kΩ)	LV	Power Dissipation (@ 1 MHz) P_D (mW)	Power Dissipation (@ 1 MHz) $P_{\Delta C}$ (mW/pF)
D Type Latch with Set/Reset			4	D	+Q	1.30	0.22	2.23	0.27	1	0.061	0.012
				PR	+Q	0.70	0.22	–	–	2		
				CL	+Q	–	–	1.10	0.27	2		
				G	+Q	1.23	0.22	1.51	0.27	2		

Note) In the machine-drawn diagram '–Q' output is also drawn. But there are restrictions in using, so consult to Hitachi in using.

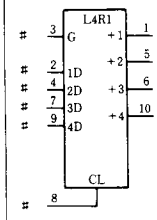
Restriction in using



Truth Table

Input				Output
PR	CL	G	D	+Q
L	H	x	x	H
H	L	x	x	L
H	H	H	L	L
H	H	H	H	H
H	H	L	x	$+Q_0$

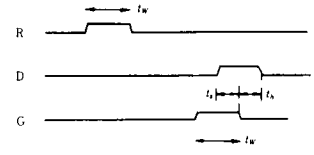
LRS0C

4 Bit Latch with Reset	Macro: Equivalent Circuit	Macro: Symbol	No. of equivalent gates	Propagation Delay Time: Terminal Name Input	Terminal Name Output	Output Rising t_{OLH} (ns)	Output Rising R_{SLH} (kΩ)	Output Falling t_{OHL} (ns)	Output Falling R_{SHL} (kΩ)	LV	Power Dissipation (@ 1 MHz) P_D (mW)	Power Dissipation (@ 1 MHz) $P_{\Delta C}$ (mW/pF)
			12	D	+n	1.11	0.23	1.81	0.23	1	0.110	0.012
				CL	+n	–	–	1.63	0.23	1		
				G	+n	2.32	0.23	2.02	0.23	1		

Truth Table

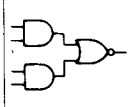
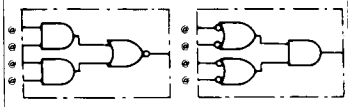
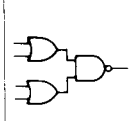
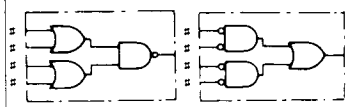
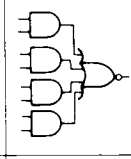
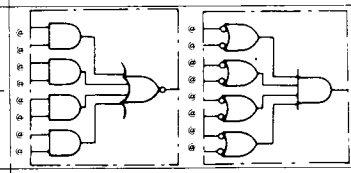
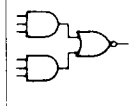
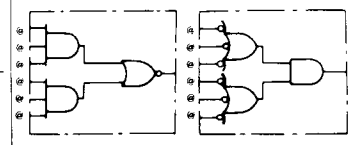
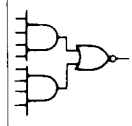
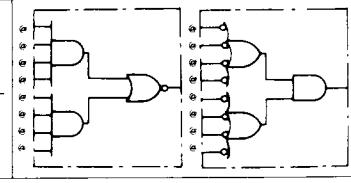
Input			Output
CL	D	G	+n
H	x	x	L
L	L	H	L
L	H	H	H
L	x	L	+n

Restriction in using

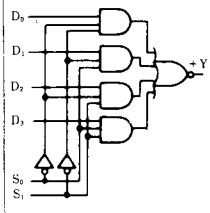
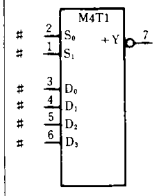
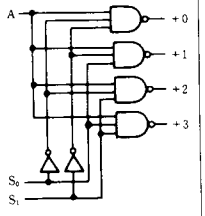
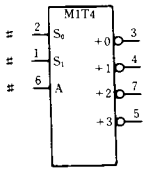


L4R1

6. AND-NOR/OR-NAND Gate

Macro: Function / Macro Name	Equivalent Circuit	Symbol	No. of equiv-alent gates	Propagation Delay Time: Output Rising t_{OLH} (ns)	Output Rising R_{SLH} (kΩ)	Output Falling t_{OHL} (ns)	Output Falling R_{SHL} (kΩ)	LV	Power Dissipation (@ 1 MHz) P_O (mW)	$P_{\Delta C}$ (mW/pF)
2 wide 2 input AND-NOR NR2A2			2	0.65	0.23	0.52	0.26	1	0.042	0.012
2 wide 2 input OR-NAND NA2R2			2	0.69	0.23	0.61	0.26	1	0.046	0.012
4 wide 2 input AND-NOR NR4A2			3	1.64	0.25	0.75	0.25	1	0.083	0.012
2 wide 3 input AND-NOR NR2A3			3	0.85	0.22	0.73	0.25	1	0.057	0.012
2 wide 4 input AND-NOR NR2A4			3	0.88	0.23	1.20	0.28	1	0.067	0.012

7. Multiplexer/Demultiplexer

Function / Macro Name	Macro: Equivalent Circuit	Macro: Symbol	No. of equivalent gates	Propagation Delay Time: Terminal Name Input	Terminal Name Output	Output Rising t_{OLH} (ns)	Output Rising R_{SLH} (kΩ)	Output Falling t_{OHL} (ns)	Output Falling R_{SHL} (kΩ)	LV	Power Dissipation (@ 1 MHz) P_O (mW)	$P_{\Delta C}$ (mW/pF)
4 Input Multiplexer			7	Sn	+Y	1.66	0.24	1.98	0.22	3	0.112	0.012
				Dn	+Y	1.46	0.24	1.32	0.22	1		
M4T1	Truth Table											
Demulti-plexer			5	Sn	+n	0.76	0.22	1.15	0.27	3	0.100	0.012
				A	+n	0.44	0.22	0.66	0.27	4		
M1T4	Truth Table											

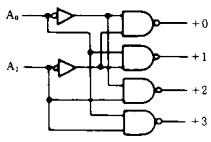
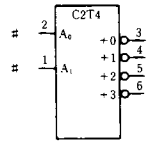
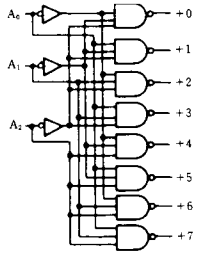
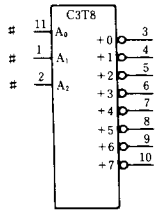
Truth Table (M4T1)

Input S_1	Input S_0	Output +Y
L	L	$\bar{D}_0$
L	H	$\bar{D}_1$
H	L	$\bar{D}_2$
H	H	$\bar{D}_3$

Truth Table (M1T4)

Input S_1	Input S_0	Output +3	+2	+1	+0
L	L	H	H	H	$\bar{A}$
L	H	H	H	$\bar{A}$	H
H	L	H	$\bar{A}$	H	H
H	H	$\bar{A}$	H	H	H

8. Decoder

Function / Macro Name	Equivalent Circuit	Symbol	No. of equivalent gates	Propagation Delay Time: Output Rising t_{OLH} (ns)	Output Rising R_{SLH} (kΩ)	Output Falling t_{OHL} (ns)	Output Falling R_{SHL} (kΩ)	LV	Power Dissipation (@ 1 MHz) P_O (mW)	$P_{\Delta C}$ (mW/pF)
2 Bit Decoder C2T4			5	0.73	0.22	1.13	0.25	3	0.069	0.012
3 Bit Decoder C3T8			10	1.03	0.22	1.69	0.27	5	0.115	0.012

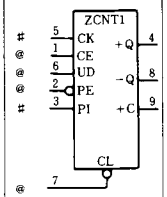
Truth Table

Input		Output			
A_1	A_0	+3	+2	+1	+0
L	L	H	H	H	L
L	H	H	H	L	H
H	L	H	L	H	H
H	H	L	H	H	H

Truth Table

Input			Output							
A_2	A_1	A_0	+7	+6	+5	+4	+3	+2	+1	+0
L	L	L	H	H	H	H	H	H	H	L
L	L	H	H	H	H	H	H	H	L	H
L	H	L	H	H	H	H	H	L	H	H
L	H	H	H	H	H	H	L	H	H	H
H	L	L	H	H	H	L	H	H	H	H
H	L	H	H	H	L	H	H	H	H	H
H	H	L	H	L	H	H	H	H	H	H
H	H	H	L	H	H	H	H	H	H	H

9. Others

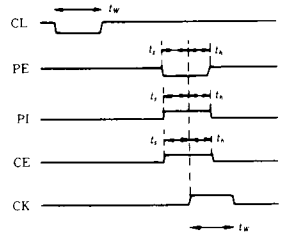
Function / Macro Name	Equivalent Circuit	Symbol	No. of equivalent gates	Terminal Name: Input	Terminal Name: Output	Propagation Delay Time: Output Rising t_{OLH} (ns)	Propagation Delay Time: Output Rising R_{SLH} (kΩ)	Propagation Delay Time: Output Falling t_{OHL} (ns)	Propagation Delay Time: Output Falling R_{SHL} (kΩ)	LV	Power Dissipation (@ 1 MHz): P_Q (mW)	Power Dissipation (@ 1 MHz): $P_{\Delta C}$ (mW/pF)
1 Bit Counter			16	CK	+Q	1.35	0.22	1.80	0.25	2	0.144	0.012
					−Q	1.20	0.22	1.99	0.25			
					+C	2.58	0.22	3.20	0.24			
				CL	+Q	(CK = low)		1.26	0.25	4		
						(CK = high)		1.92	0.25			
					−Q	0.69	0.22	–	–			
					+C	2.27	0.22	(UD = low)				
						(UD = high)		2.95	0.24			
				CE	+C	1.26	0.22	1.08	0.24	2		
				UD	+C	1.50	0.22	1.22	0.24	2		
				PE						2		
				PI						1		

Truth Table

Input					Output	
CL	PE	PI	CE	CK	+Q	−Q
L	×	×	×	×	L	H
H	L	L	×	↑	L	H
H	L	H	×	↑	H	L
H	H	×	L	↑	+Qn-1	−Qn-1
H	H	×	H	↑	−Qn-1	+Qn-1

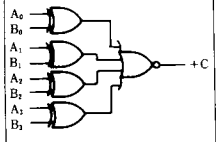
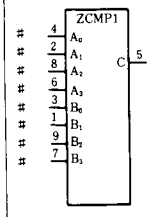
Input		Output
UD	CE	+C
×	L	L
L	H	−Q
H	H	+Q

Restriction in using

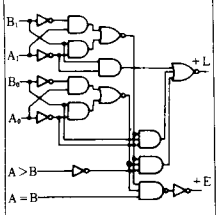
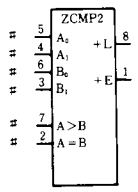


where
$t_w \geqq 2.5$ ns
$t_s \geqq 3.0$ ns
$t_h \geqq 0.4$ ns

ZCNT1

4 Bit Equivalent Comparator			12			2.19	0.29	1.44	0.23	2	0.064	0.012

ZCMP1

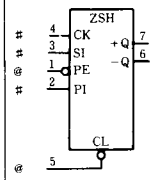
2 Bit Comparator			11	An/Bn	+L	2.26	0.26	2.86	0.26	2	0.068	0.012
				A > B	+L	0.82	0.26	1.25	0.26	1		
				An/Bn	+E	2.15	0.22	2.01	0.22	2		
				A = B	+E	0.74	0.22	0.96	0.22	1		

Truth Table

Input						Output	
A_1	A_0	B_1	B_0	A > B	A = B	+L	+E
A > B				×	×	H	L
A = B				L	L	L	L
				L	H	L	H
				H	L	H	L
				H	H	H	H
A < B				×	×	L	L

ZCMP2

Others (Continued)

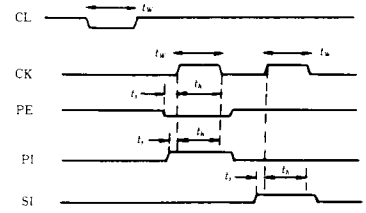
Macro: Function / Macro Name	Equivalent Circuit	Symbol	No. of equivalent gates	Propagation Delay Time: Terminal Name Input	Terminal Name Output	Output Rising t_{OLH} (ns)	Output Rising R_{SLH} (kΩ)	Output Falling t_{OHL} (ns)	Output Falling R_{SHL} (kΩ)	LV	Power Dissipation (@ 1 MHz) P_O (mW)	Power Dissipation (@ 1 MHz) $P_{\Delta C}$ (mW/pF)
1 Bit Shift Register			7	CK	+Q	1.28	0.22	1.48	0.27	2	0.061	0.012
					−Q	1.22	0.22	1.75	0.27			
				CL	+Q	(CK = low)		1.01	0.25	3		
						(CK = high)		1.79	0.25			
					−Q	0.70	0.22	–	–			
				SI		–	–	–	–	1		
				PE		–	–	–	–	2		
				PI		–	–	–	–	1		

ZSH

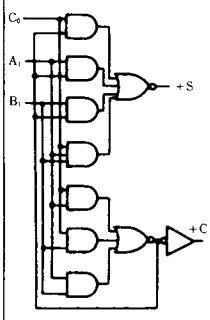
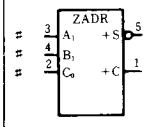
Truth Table

Input CL	PE	PI	SI	CK	Output +Q	−Q
L	×	×	×	×	L	H
H	L	L	×	↑	L	H
H	L	H	×	↑	H	L
H	H	×	L	↑	L	H
H	H	×	H	↑	H	L

Restriction in using



where
$t_w \geqq 2.5$ ns
$t_s \geqq 3.0$ ns
$t_h \geqq 0.4$ ns

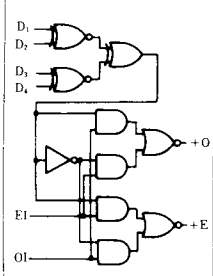
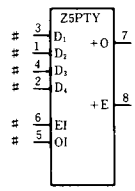
1 Bit Full Adder			6	A_1/B_1	+S	2.60	0.23	3.97	0.22	4	0.143	0.012
					+C	1.17	0.23	3.23	0.27			
				C_0	+S	2.55	0.23	3.54	0.22	4		
					+C	1.16	0.23	3.12	0.27			

ZADR

Truth Table

Input A_1	B_1	C_0	Output +S	+C
L	L	L	H	L
L	L	H	L	L
L	H	L	L	L
L	H	H	H	H
H	L	L	L	L
H	L	H	H	H
H	H	L	H	H
H	H	H	L	H

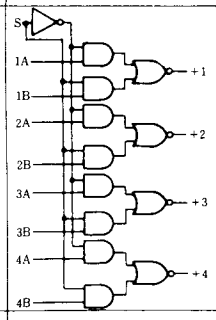
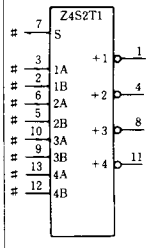
Others (Continued)

Function / Macro Name	Macro: Equivalent Circuit	Macro: Symbol	No. of equivalent gates	Propagation Delay Time: Terminal Name Input	Terminal Name Output	Output Rising t_{OLH} (ns)	Output Rising R_{SLH} (kΩ)	Output Falling t_{OHL} (ns)	Output Falling R_{SHL} (kΩ)	LV	Power Dissipation (@ 1 MHz) P_O (mW)	Power Dissipation (@ 1 MHz) $P_{\Delta C}$ (mW/pF)
5 Bit Parity			12	Dn	+O	3.87	0.24	3.84	0.24	2	0.110	0.012
					+E	3.85	0.24	3.89	0.24			
				EI	+O	0.58	0.24	0.53	0.24	2		
					+E	0.82	0.24	0.77	0.24			
				OI	+O	0.81	0.24	0.74	0.24	2		
					+E	0.56	0.24	0.60	0.24			

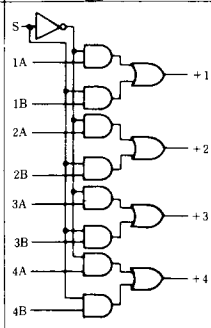
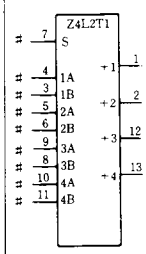
Truth Table

Input D_4	D_3	D_2	D_1	EI	OI	Output +E	+O
Odd-numbered				L	H	H	L
H				H	L	L	H
Even-numbered				L	H	L	H
H				H	L	H	L

Z5PTY

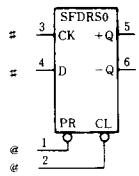
Function / Macro Name	Equivalent Circuit	Symbol	No. of equivalent gates	Terminal Name Input	Terminal Name Output	Output Rising t_{OLH} (ns)	Output Rising R_{SLH} (kΩ)	Output Falling t_{OHL} (ns)	Output Falling R_{SHL} (kΩ)	LV	Power Dissipation (@ 1 MHz) P_O (mW)	Power Dissipation (@ 1 MHz) $P_{\Delta C}$ (mW/pF)
Quad 2-1 Selector			9	S	+n	1.08	0.24	1.65	0.25	5	0.196	0.012
				A/B	+n	0.76	0.24	0.64	0.25	1		

Z4S2T1

Function / Macro Name	Equivalent Circuit	Symbol	No. of equivalent gates	Terminal Name Input	Terminal Name Output	Output Rising t_{OLH} (ns)	Output Rising R_{SLH} (kΩ)	Output Falling t_{OHL} (ns)	Output Falling R_{SHL} (kΩ)	LV	Power Dissipation (@ 1 MHz) P_O (mW)	Power Dissipation (@ 1 MHz) $P_{\Delta C}$ (mW/pF)
Quad 2-1 Selector			11	S	+n	1.91	0.22	1.98	0.24	5	0.120	0.012
				A/B	+n	1.06	0.22	1.76	0.24	1		

Z4L2T1

10 Diagnosis Cell (HG29M100 only)

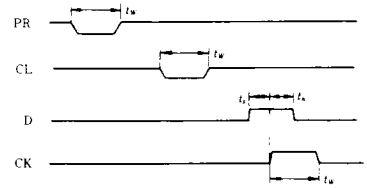
Function / Macro Name	Equivalent Circuit	Symbol	No. of equivalent gates	Terminal Name Input	Terminal Name Output	Propagation Delay Time: Output Rising t_{OLH} (ns)	Output Rising R_{SLH} (kΩ)	Output Falling t_{OHL} (ns)	Output Falling R_{SHL} (kΩ)	LV	Power Dissipation (@ 1 MHz) P_Q (mW)	$P_{\Delta C}$ (mW/pF)
D Type Edge Triggered Flip-Flop with diagnosis			10	D		–	–	–	–	1	0.078	0.012
				PR	+Q	0.73	0.22	–	–	3		
					−Q	(CK = low)		1.16	0.27			
						(CK = high)		1.47	0.27			
				CL	+Q	(CK = low)		1.36	0.27	3		
						(CK = high)		1.74	0.27			
					−Q	0.88	0.22	–	–			
				CK	+Q	1.31	0.22	1.96	0.27	2		
					−Q	1.38	0.22	1.74	0.27			

SFDRS0

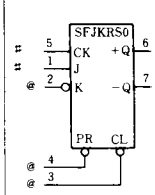
Truth Table

Input PR	CL	CK	D	Output +Q	−Q
L	H	×	×	H	L
H	L	×	×	L	H
L	L	×	×	H	H
H	H	↑	H	H	L
H	H	↑	L	L	H
H	H	L	×	$+Q_0$	$-Q_0$

Restriction in using



where
$t_w \geqq 2.5$ ns
$t_s \geqq 2.0$ ns
$t_h \geqq 0.4$ ns

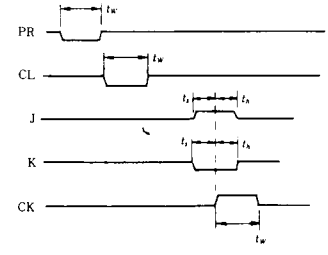
J-K Type Edge Triggered Flip-Flop with diagnosis			11	J		–	–	–	–	1	0.070	0.012
				K		–	–	–	–	1		
				PR	+Q	0.72	0.22	–	–	3		
					−Q	(CK = low)		1.34	0.27			
						(CK = high)		1.86	0.27			
				CL	+Q	(CK = low)		1.30	0.27	3		
						(CK = high)		1.90	0.27			
					−Q	0.90	0.22	–	–			
				CK	+Q	1.46	0.22	1.89	0.27	2		
					−Q	1.45	0.22	1.95	0.27			

SFJKRS0

Truth Table

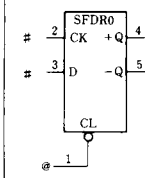
Input PR	CL	CK	J	K	Output +Q	−Q
L	H	×	×	×	H	L
H	L	×	×	×	L	H
L	L	×	×	×	H	H
H	H	↑	L	H	$+Q_0$	$-Q_0$
H	H	↑	L	L	L	H
H	H	↑	H	H	H	L
H	H	↑	H	L	Toggle	
H	H	L	×	×	$+Q_0$	$-Q_0$

Restriction in using

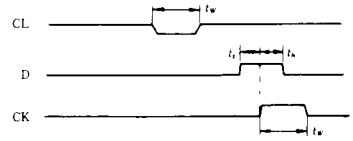


where
$t_w \geqq 2.5$ ns
$t_s \geqq 3.0$ ns
$t_h \geqq 0.4$ ns

Diagnosis Cell (Continued)

Function / Macro Name	Equivalent Circuit	Symbol	No. of equivalent gates	Terminal Name Input	Terminal Name Output	Propagation Delay Time: Output Rising t_{OLH} (ns)	Output Rising R_{SLH} (kΩ)	Output Falling t_{OHL} (ns)	Output Falling R_{SHL} (kΩ)	LV	Power Dissipation (@ 1 MHz) P_O (mW)	$P_{\Delta C}$ (mW/pF)
D Type Edge Triggered Flip-Flop with diagnosis			9	D		–	–	–	–	1	0.078	0.012
				CL	+Q	(CK = low)		1.46	0.27	3		
						(CK = high)		1.74	0.27			
					−Q	0.88	0.22	–	–			
				CK	+Q	1.31	0.22	1.83	0.27	2		
					−Q	1.22	0.22	1.74	0.27			

Restriction in using

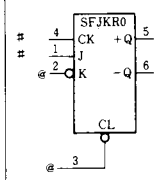


where
$t_w \geqq 2.5$ ns
$t_s \geqq 2.0$ ns
$t_h \geqq 0.4$ ns

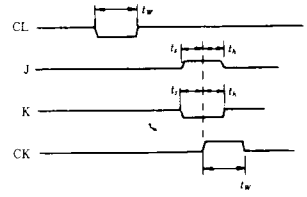
Truth Table

Input			Output	
CL	CK	D	+Q	−Q
L	x	x	L	H
H	↑	H	H	L
H	↑	L	L	H
H	L	x	$+Q_0$	$-Q_0$

SFDR0

Function / Macro Name	Equivalent Circuit	Symbol	No. of equivalent gates	Terminal Name Input	Terminal Name Output	Propagation Delay Time: Output Rising t_{OLH} (ns)	Output Rising R_{SLH} (kΩ)	Output Falling t_{OHL} (ns)	Output Falling R_{SHL} (kΩ)	LV	Power Dissipation (@ 1 MHz) P_O (mW)	$P_{\Delta C}$ (mW/pF)
J-K Type Edge Triggered Flip-Flop with diagnosis			10	J		–	–	–	–	1	0.070	0.012
				K		–	–	–	–	1		
				CL	+Q	(CK = low)		1.30	0.27	3		
						(CK = high)		1.90	0.27			
					−Q	0.90	0.22	–	–			
				CK	+Q	1.46	0.22	1.83	0.27	2		
					−Q	1.29	0.22	1.95	0.27			

Restriction in using



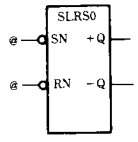
where
$t_w \geqq 2.5$ ns
$t_s \geqq 3.0$ ns
$t_h \geqq 0.4$ ns

Truth Table

Input				Output	
CL	CK	J	K	+Q	−Q
L	x	x	x	L	H
H	↑	L	H	$+Q_0$	$-Q_0$
H	↑	L	L	L	H
H	↑	H	H	H	L
H	↑	H	L	Toggle	
H	L	x	x	$+Q_0$	$-Q_0$

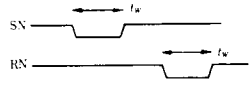
SFJKR0

Diagnosis Cell (Continued)

Macro: Function / Macro Name	Equivalent Circuit	Symbol	No. of equivalent gates	Propagation Delay Time: Terminal Name Input	Terminal Name Output	Output Rising t_{OLH} (ns)	Output Rising R_{SLH} (kΩ)	Output Falling t_{OHL} (ns)	Output Falling R_{SHL} (kΩ)	LV	Power Dissipation (@ 1 MHz) P_O (mW)	$P_{\Delta C}$ (mW/pF)
Latch with Set/Reset With diagnosis SLRS0			5	SN	+Q	0.55	0.22	–	–	1	0.038	0.012
					−Q	–	–	1.07	0.27			
				RN	+Q	–	–	1.17	0.27	1		
					−Q	0.65	0.22	–	–			

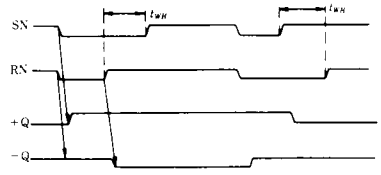
Restriction in using

1.

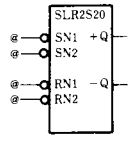


where
$t_W \geqq 2.5$ ns

2.

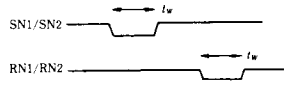


where
$t_{WH} \geqq 2.0$ ns

Macro: Function / Macro Name	Equivalent Circuit	Symbol	No. of equivalent gates	Terminal Name Input	Terminal Name Output	Output Rising t_{OLH} (ns)	Output Rising R_{SLH} (kΩ)	Output Falling t_{OHL} (ns)	Output Falling R_{SHL} (kΩ)	LV	Power Dissipation (@ 1 MHz) P_O (mW)	$P_{\Delta C}$ (mW/pF)
Latch with Set/Reset With diagnosis SLR2S20			5	SN1/ SN2	+Q	0.66	0.22	–	–	1	0.050	0.012
					−Q	–	–	1.35	0.29			
				RN1/ RN2	+Q	–	–	1.45	0.29	1		
					−Q	0.76	0.22	–	–			

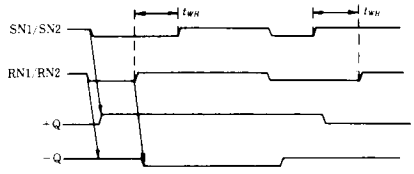
Restriction in using

1.

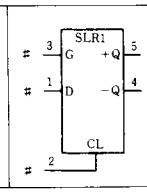


where
$t_W \geqq 2.5$ ns

2.



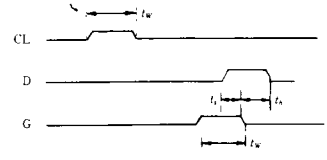
where
$t_{WH} \geqq 2.0$ ns

Macro: Function / Macro Name	Equivalent Circuit	Symbol	No. of equivalent gates	Terminal Name Input	Terminal Name Output	Output Rising t_{OLH} (ns)	Output Rising R_{SLH} (kΩ)	Output Falling t_{OHL} (ns)	Output Falling R_{SHL} (kΩ)	LV	Power Dissipation (@ 1 MHz) P_O (mW)	$P_{\Delta C}$ (mW/pF)
D Type Latch With diagnosis SLR1			8	D	+Q	2.28	0.28	1.22	0.24	2	0.128	0.012
					−Q	2.22	0.24	1.12	0.26			
				CL	+Q	–	–	0.60	0.24	2		
					−Q	1.76	0.24	–	–			
				G	+Q	2.27	0.28	0.88	0.24	2		
					−Q	1.94	0.24	0.89	0.26			

Truth Table

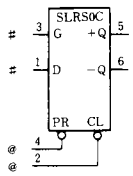
Input			Output	
CL	G	D	+Q	−Q
H	x	x	L	H
L	H	L	L	H
L	H	H	H	L
L	L	x	$+Q_0$	$-Q_0$

Restriction in using



where
$t_W \geqq 2.5$ ns
$t_S \geqq 3.0$ ns
$t_h \geqq 0.4$ ns

Diagnosis Cell (Continued)

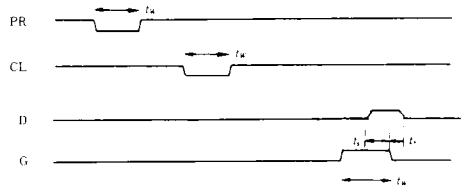
Function / Macro Name	Macro: Equivalent Circuit	Macro: Symbol	No. of equivalent gates	Propagation Delay Time: Terminal Name Input	Terminal Name Output	Output Rising t_{OLH} (ns)	Output Rising R_{SLH} (kΩ)	Output Falling t_{OHL} (ns)	Output Falling R_{SHL} (kΩ)	LV	Power Dissipation (@ 1 MHz) P_Q (mW)	Power Dissipation (@ 1 MHz) $P_{\Delta C}$ (mW/pF)
D Type Latch with Set/Reset With diagnosis			7	D	+Q	1.30	0.22	2.43	0.27	1		
				PR	+Q	0.70	0.22	–	–	2		
				CL	+Q	–	–	1.30	0.27	2	0.061	0.012
				G	+Q	1.23	0.22	1.71	0.27	2		

Note) In the machine-drawn diagram '−Q' output is also drawn. But there are restrictions in using, so consult to Hitachi in using.

Truth Table

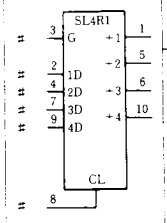
Input PR	Input CL	Input G	Input D	Output +Q
L	H	×	×	H
H	L	×	×	L
H	H	H	L	L
H	H	H	H	H
H	H	L	×	$+Q_0$

Restriction in using



where
$t_w \geqq 2.5$ ns
$t_s \geqq 2.5$ ns
$t_h \geqq 0.4$ ns

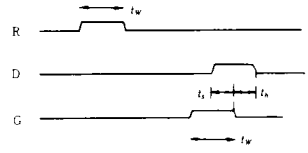
SLRS0C

Function / Macro Name	Macro: Equivalent Circuit	Macro: Symbol	No. of equivalent gates	Propagation Delay Time: Terminal Name Input	Terminal Name Output	Output Rising t_{OLH} (ns)	Output Rising R_{SLH} (kΩ)	Output Falling t_{OHL} (ns)	Output Falling R_{SHL} (kΩ)	LV	Power Dissipation (@ 1 MHz) P_Q (mW)	Power Dissipation (@ 1 MHz) $P_{\Delta C}$ (mW/pF)
4 Bit Latch with Reset With diagnosis			24	D	+n	1.31	0.23	2.01	0.23	1		
				CL	+n	–	–	1.83	0.23	1	0.110	0.012
				G	+n	2.52	0.23	2.22	0.23	1		

Truth Table

Input CL	Input D	Input G	Output +n
H	×	×	L
L	L	H	L
L	H	H	H
L	×	L	+n

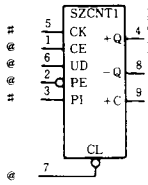
Restriction in using



where
$t_w \geqq 2.5$ ns
$t_s \geqq 2.5$ ns
$t_h \geqq 0.4$ ns

SL4R1

Diagnosis Cell (Continued)

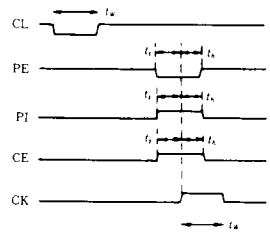
Function / Macro Name	Macro: Equivalent Circuit	Macro: Symbol	No. of equivalent gates	Propagation Delay Time: Input	Output	Output Rising: t_{OLH} (ns)	Output Rising: R_{SLH} (kΩ)	Output Falling: t_{OHL} (ns)	Output Falling: R_{SHL} (kΩ)	LV	Power Dissipation (@ 1 MHz): P_O (mW)	Power Dissipation (@ 1 MHz): $P_{\Delta C}$ (mW/pF)
1 Bit Counter With Diagnosis			19	CK	+Q	1.35	0.22	2.00	0.25	2	0.144	0.012
					−Q	1.30	0.22	2.09	0.25			
					+Q	2.58	0.22	3.20	0.24			
				CL	+Q	(CK = low)		1.46	0.25	4		
						(CK = high)		1.92	0.25			
					−Q	0.79	0.22	–	–			
					+C	2.27	0.22	(UD = low)				
						(UD = high)		2.95	0.24			
				CE	+C	1.26	0.22	1.08	0.24	2		
				UD	+C	1.50	0.22	1.22	0.24	2		
				PE						2		
				PI						1		

Truth Table

Input					Output	
CL	PE	PI	CE	CK	+Q	−Q
L	x	x	x	x	L	H
H	L	L	x	↑	L	H
H	L	H	x	↑	H	L
H	H	x	L	↑	$+Q_{n-1}$	$-Q_{n-1}$
H	H	x	H	↑	$-Q_{n-1}$	$+Q_{n-1}$

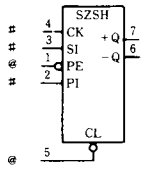
Input		Output
UD	CE	+C
x	L	L
L	H	−Q
H	H	+Q

Restriction in using



where
$t_w \geqq 2.5$ ns
$t_s \geqq 3.0$ ns
$t_h \geqq 0.4$ ns

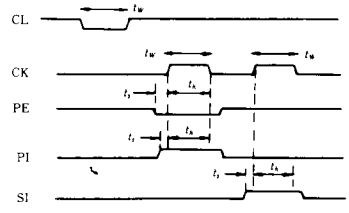
SZCNTI

Function / Macro Name	Macro: Equivalent Circuit	Macro: Symbol	No. of equivalent gates	Propagation Delay Time: Input	Output	Output Rising: t_{OLH} (ns)	Output Rising: R_{SLH} (kΩ)	Output Falling: t_{OHL} (ns)	Output Falling: R_{SHL} (kΩ)	LV	Power Dissipation (@ 1 MHz): P_O (mW)	Power Dissipation (@ 1 MHz): $P_{\Delta C}$ (mW/pF)
1 Bit Shift Register With Diagnosis			10	CK	+Q	1.28	0.22	1.68	0.27	2	0.061	0.012
					−Q	1.32	0.22	1.85	0.27			
				CL	+Q	(CK = low)		1.21	0.25	3		
						(CK = high)		1.79	0.25			
					−Q	0.80	0.22	–	–			
				SI		–	–	–	–	1		
				PE		–	–	–	–	2		
				PI		–	–	–	–	1		

Truth Table

Input					Output	
CL	PE	PI	SI	CK	+Q	−Q
L	x	x	x	x	L	H
H	L	L	x	↑	L	H
H	L	H	x	↑	H	L
H	H	x	L	↑	L	H
H	H	x	H	↑	H	L

Restriction in using



where
$t_w \geqq 2.5$ ns
$t_s \geqq 3.0$ ns
$t_h \geqq 0.4$ ns

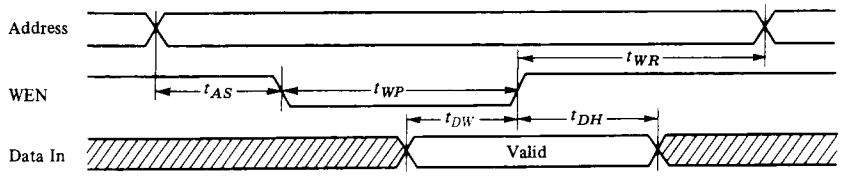
SZSH

RAM Cell (HG29M100 only)

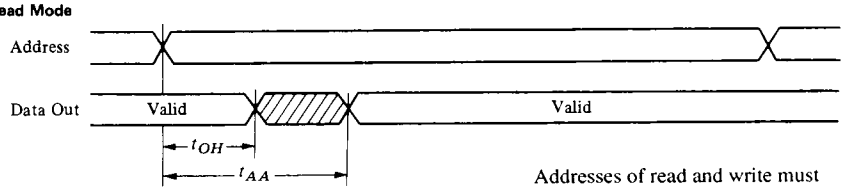
Macro: Function / Macro Name	Equivalent Circuit	Symbol	No. of equivalent gates	Propagation Delay Time: Terminal Name Input	Terminal Name Output	Output Rising t_{OLH} (ns)	Output Rising R_{SLH} (kΩ)	Output Falling t_{OHL} (ns)	Output Falling R_{SHL} (kΩ)	LV	Power Dissipation (@ 1 MHz) P_O (mW)	Power Dissipation (@ 1 MHz) $P_{\Delta C}$ (mW/pF)
3 Port RAM RAM 36		RAM36 WEN0 WEN1 WEN2 WEN3 $DR1_{35-0}$ $DR2_{35-0}$ AW_{6-0} $AR1_{6-0}$ $AR2_{6-0}$ DW_{35-0} Floating pin prohibited	0	WEN		–	–	–	–	4	9.8	0.012
				AW		–	–	–	–			
				AR1	DR1	8.5	0.12	10.0	0.16	5		
				AR2	DR2	8.5	0.12	10.0	0.16			
				DW		–	–	–	–	3		
3 Port RAM RAM 18		RAM18 WEN0 WEN1 $DR1_{17-0}$ $DR2_{17-0}$ AW_{7-0} $AR1_{7-0}$ $AR2_{7-0}$ DW_{17-0} Floating pin prohibited	0	WEN		–	–	–	–	4	9.8	0.012
				AW		–	–	–	–			
				AR1	DR1	8.5	0.12	10.0	0.16	5		
				AR2	DR2	8.5	0.12	10.0	0.16			
				DW		–	–	–	–	3		
3 Port RAM RAM 09		RAM09 WEN0 $DR1_{8-0}$ $DR2_{8-0}$ AW_{8-0} $AR1_{8-0}$ $AR2_{8-0}$ DW_{8-0} Floating pin prohibited	0	WEN		–	–	–	–	4	0.8	0.012
				AW		–	–	–	–			
				AR1	DR1	8.5	0.12	10.0	0.16	5		
				AR2	DR2	8.5	0.12	10.0	0.16			
				DW		–	–	–	–	3		

RAM Timing & Spec

• **Write Mode**



• **Read Mode**



Addresses of read and write must not be conflicted.

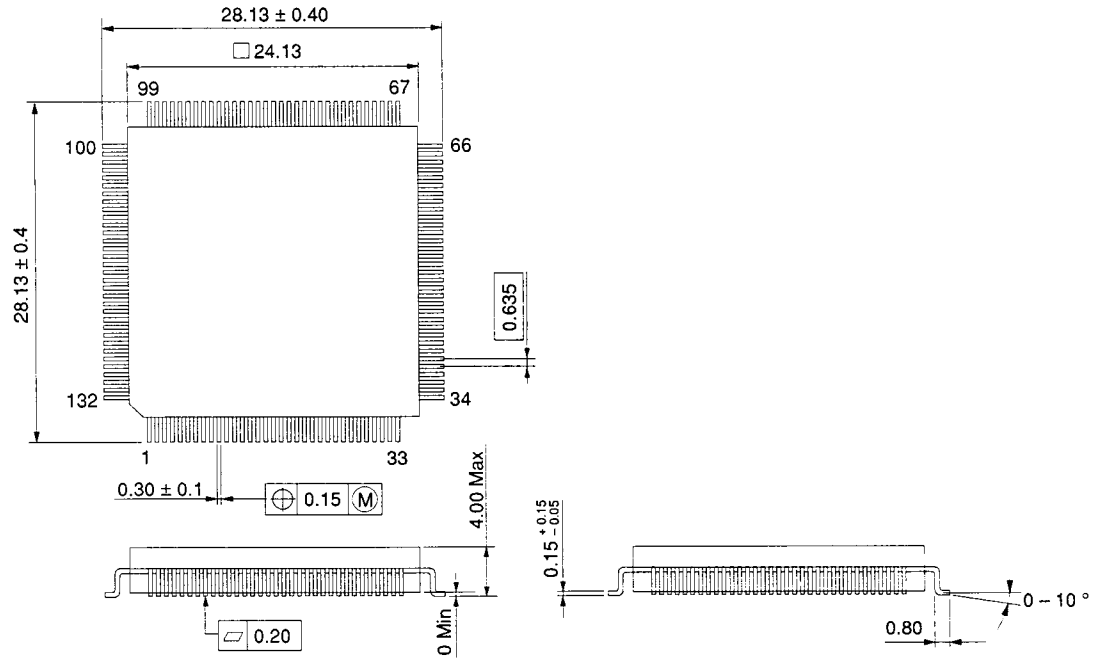
• **Specification**

	Parameter	Symbol	Min.	Max.	Unit
Write Mode	Address Setup Time	t_{AS}	9	–	ns
	Write Pulse Width	t_{WP}	4	–	
	Address Hold Time	t_{WR}	7	–	
	Data Setup	t_{DW}	5	–	
	Data Hold	t_{DH}	7	–	
Read Mode	Address Access Time	t_{AA}	–	20	
	Data Setup	t_{OH}	0	–	

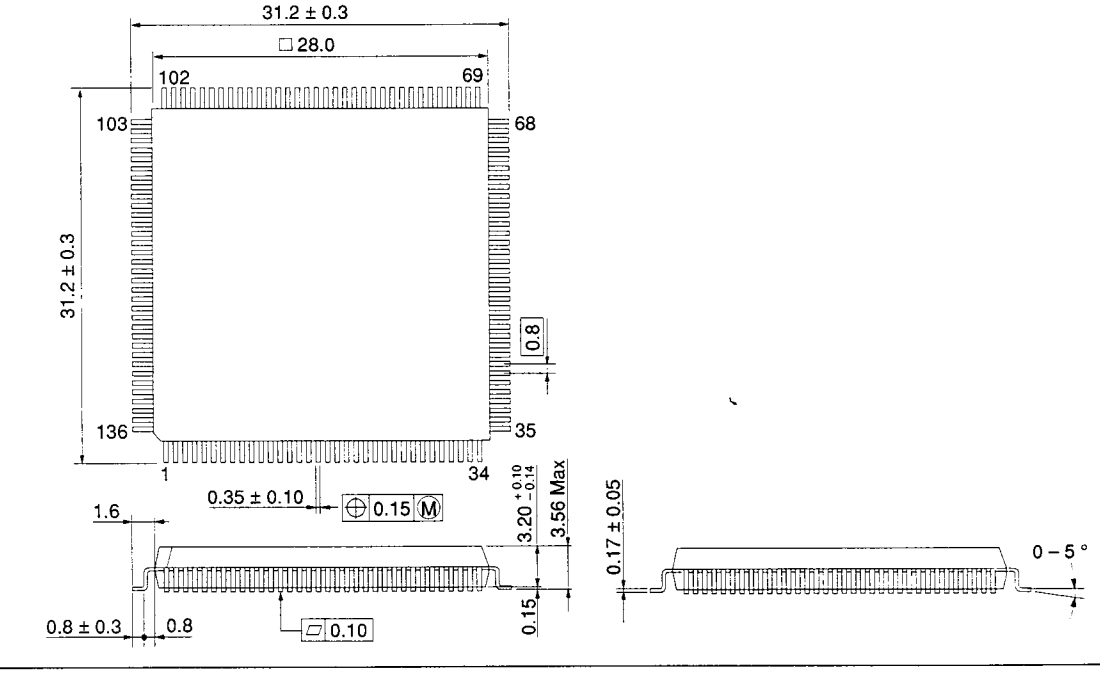
Package Dimensions

Unit: mm

FPG-132



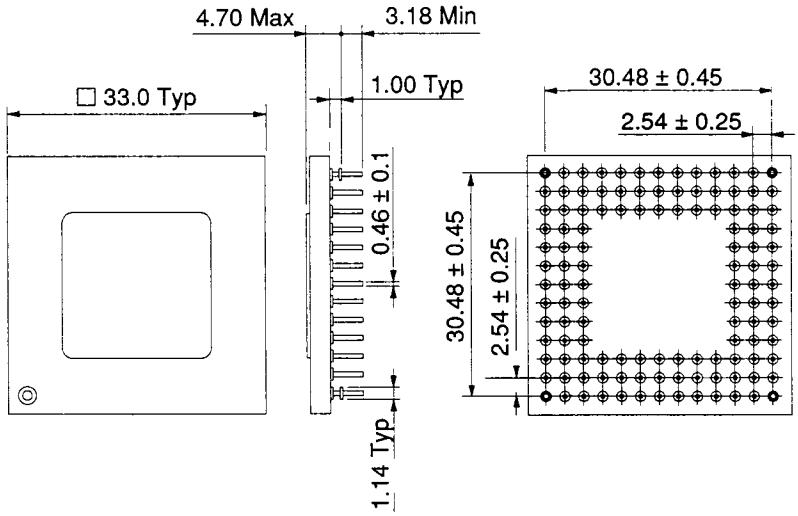
QFP-136



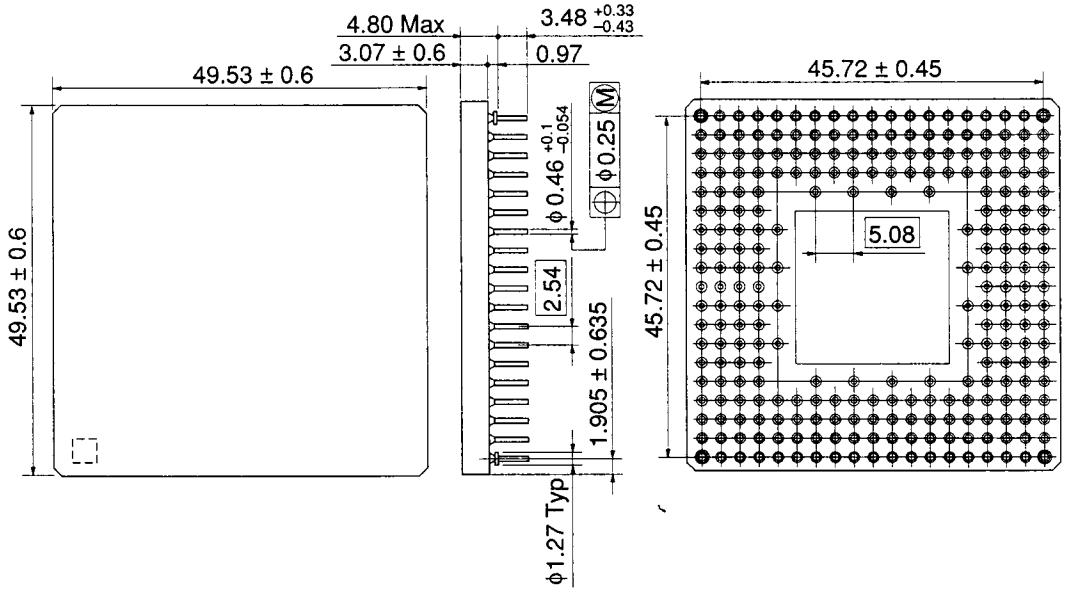
Package Dimensions (cont)

Unit: mm

PGA-120



PGA-257



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