PRODUCT BRIEF*

T-52-33-15

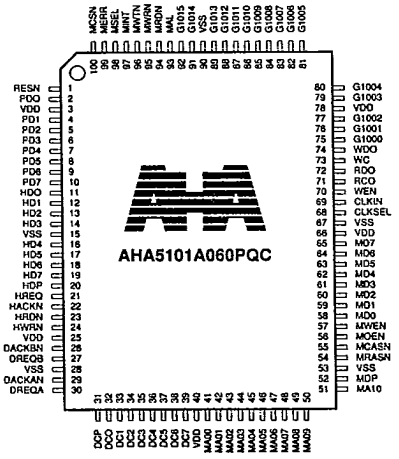
AHA5101 (SINGLE)
AHA5121 (DUAL)

PROGRAMMABLE TAPE FORMATTER/CONTROLLER IC

PRODUCT DESCRIPTION

The AHA5101 and AHA5121 Tape Formatter/Controllers provide functions not previously available in one package. Fully programmable tape format generation and control is integrated with sophisticated buffer and data management and "on-the-fly" error detection and correction. These functions are accomplished under firmware control with minimal real-time intervention. In addition, DMA ports are provided for use with a data compression or encryption coprocessor.

The AHA5101 (single channel controller) and AHA5121 (dual channel controller) implement physical recording formats standardized by Quarter Inch Cartridge Drive Standards, Inc. (QIC™), or may optionally be configured to produce non-standard tape formatting. Buffer/Data management is accomplished by hardware DMA channels and sophisticated control techniques which enable all I/O processes to be simultaneous. Thus, high host data rates may be sustained concurrently with ECC, Data Compression, and tape accesses. The AHA5101 is firmware and interface compatible with the AHA5121 Dual-Channel Tape Controller. The AHA5121 comes in a larger single chip package and may be cascaded for multichannel applications.



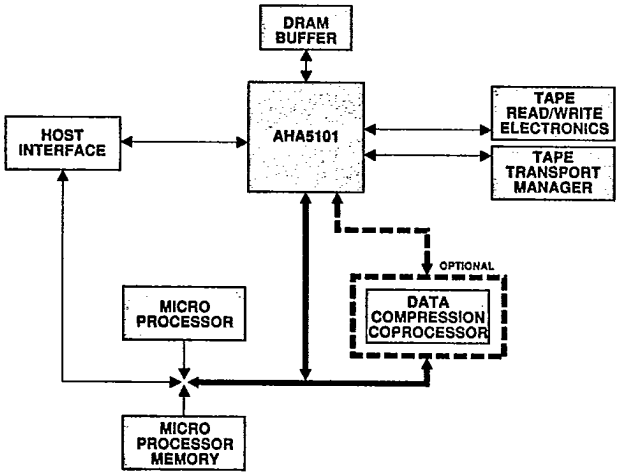
FEATURES AND BENEFITS

- Provides format control, buffer/data management, and "On-the-fly" Reed-Solomon Error Correction.
- Writes QIC™ 1350, 525, 150, and 120 recording formats.
- Reads QIC™ 1350, 525, 150, 120, and 24 recording formats.
- Optionally performs QIC™ 1350 Write Equalization.
- Optimizes data throughput for tape streaming under adverse system conditions. Correction of errors will not interrupt streaming.
- May be programmed to read and/or write non-standard formatting.
- READ-WHILE-WRITE verification for data integrity.
- Programmable 16 bit GIO for control and monitoring of external functions (e.g. tape transport mechanism).
- Dedicated DMA port for optimum performance with AHA3101* (or other) Data Compression Coprocessor.
- Individually maskable and resetable interrupts for control, status, and event detection.
- Manages up to 4 Megabytes of standard 80 ns DRAM.
- Provides optional even or odd parity checking.
- Programmable clock outputs for timer/counter functions.
- Common interface with AHA5121 dual channel tape controller.
- Flexible Microprocessor Data/Address interface.
- Firmware compatibility between single and dual channel architectures.
- Single channel chip (AHA5101) available in 100 pin PQFP (standard).

Advanced Hardware Architectures™

*See the *AHA5101* Product Specification for complete details.

TYPICAL SUBSYSTEM DIAGRAM



SYSTEM OVERVIEW

The block diagram shows a typical tape controller sub-system architecture using the AHA5101. The sub-system has seven major components:

1. The microprocessor together with its associated ROM and RAM monitors and controls sub-system activity.
2. The AHA5101 coordinates the operation of the other sub-system components under the direction of the microprocessor.
3. The host system interface controller transmits and receives host system data and control information.
4. The sub-system memory buffers data on its way to and from tape.
5. The tape transport performs all electro-mechanical functions associated with tape movement.
6. The tape READ/WRITE channel performs all operations associated with magnetic recording and playback.
7. Optional Data Compression/Decompression Coprocessor.

TAPE FORMATTER

The AHA5101 and AHA5121 are more than formatters and controllers. They can READ or WRITE QIC™ 1350, 525, 150, or 120 physical recording formats, and can READ QIC™ 24 format. In addition, these devices can be configured to implement non-standard formatting, provided standard modulation (GCR 4,5 or RLL 1,7) encoding is used.

Automatic READ-WHILE-WRITE verification and rewrite is provided, as well as the CRC protection specified in the QIC™ standards.

Optional QIC™ 1350 Write Equalization is provided.

INTEGRATED HARDWARE ECC

The AHA5101 and AHA5121 have fully integrated Reed-Solomon error detection and correction modules, which perform all encoding and decoding without firmware intervention. The time required to encode or decode a frame of data is less than the time required to WRITE/READ the corresponding data to/from tape. Hence, the ECC process has no impact on tape streaming regardless of the error conditions encountered. Full ECC syndromes are always generated, so errors may be corrected even though undetected by CRC. In addition, all corrections provide "unusual event notification" interrupts.

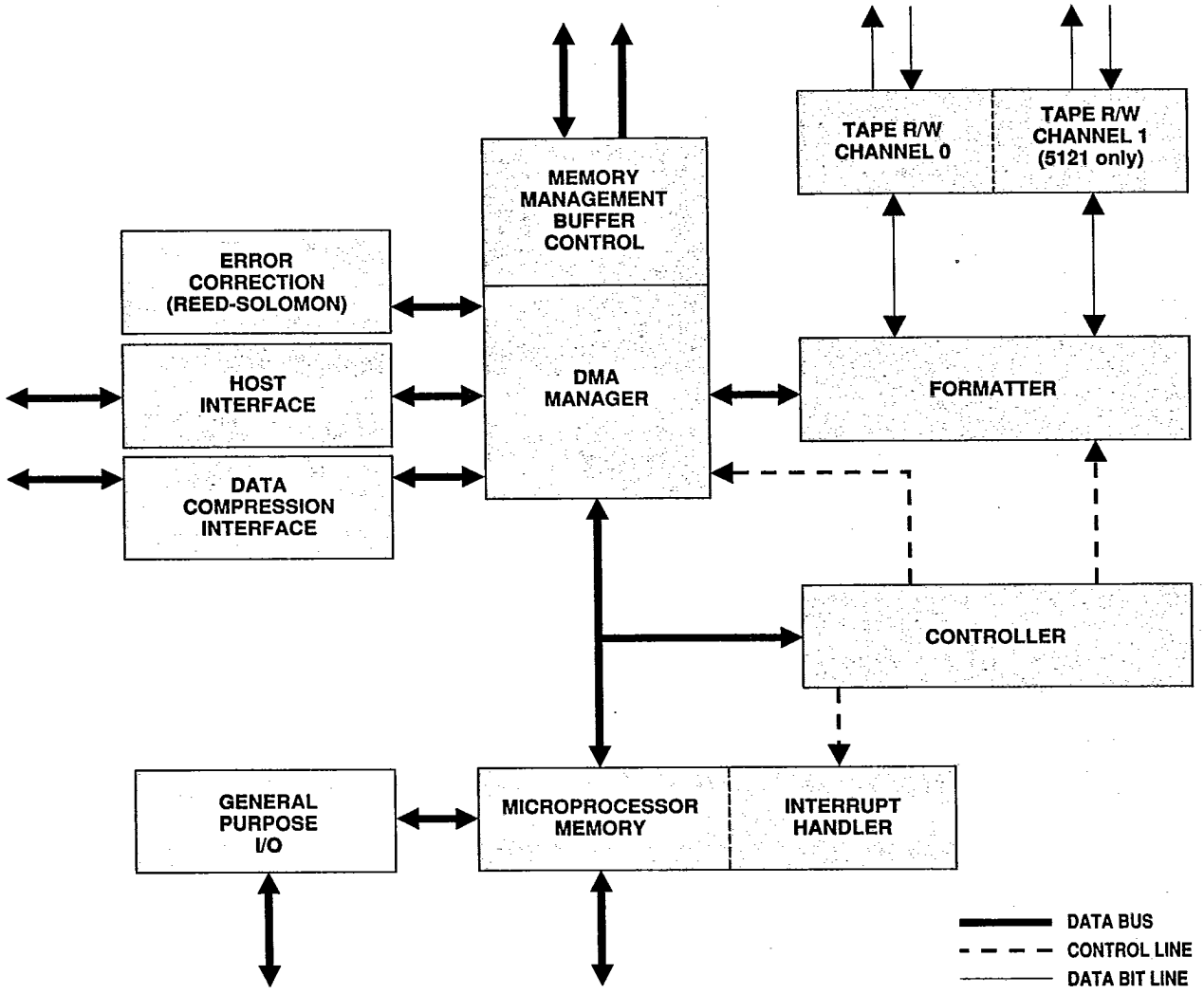
DATA/BUFFER MANAGEMENT

The AHA5101 and AHA5121 control all accesses to buffer memory and are capable of addressing up to 4 Megabytes of Dynamic Random Access Memory (DRAM). The buffer manager can fully utilize standard DRAMs with a specified access time of 80 n, and provides all necessary timing and control signals including those needed for automatic refresh. The refresh rate is selectable (fast or normal) to allow the use of a slow system clock.

Data is transported and manipulated by means of powerful and very flexible DMA channels. DMA processes may be constructed to move any regularly occurring data structures to, from or within memory, skipping over unwanted data or data structures. This allows easy manipulation of control bytes, ECC matrices, data frames and logical blocks.

Memory arbitration among DMA processes is handled in hardware, and DRAM Page Mode is utilized to optimize memory bandwidth to over 11 Megabytes per second. Thus, all processes may run concurrently without impact to tape streaming.

INTERNAL BLOCK DIAGRAM



HOST INTERFACE

The AHA5101 and AHA5121 interface to the host via DMA, so direct compatibility with most SCSI chips, e.g. the NCR 53C94 family, is achieved without external hardware. Data rates up to 10 Megabytes per second may be supported over the system bus if Burst Mode is used. When tape is streaming, host bus data rates up to approximately 7 Megabytes per second can be supported.

For hosts that transfer data at slower rates, a programmable feature is provided which allows wait state insertion to memory accesses via the Host DMA channel. Sub-system synchronization is thus enabled with the host to maximize data transfer efficiency.

MICROPROCESSOR INTERFACE

Microprocessor connection to the AHA5101 or AHA5121 is made by means of an address bus, a data bus and a control bus. The formatter/controller may be placed in the memory or I/O space of the microprocessor, depending on the derivation of the CHIP SELECT signal. The AHA5101 is architecturally identical to its sister part, the AHA5121 except for the second channel. The two are fully firmware compatible.

The microprocessor may read or write locations in the sub-system buffer, but these accesses are treated as DMA operations. Single access operations are permitted, but string accesses are more efficient. If the locations to be accessed are not contiguous (e.g. control bytes in a particular frame), but occur with regularity, the DMA can be set up to access a number of locations, followed by an offset, and the process repeated until the byte count is satisfied. The data may be placed in contiguous locations in the destination space.

The microprocessor reads and writes internal AHA5101 or AHA5121 locations by both direct and indirect access. Additionally, simple commands may be used to substitute for some frequently occurring functions which would otherwise require extensive firmware programming.

The AHA5101 or AHA5121 may be programmed to provide up to 24 separately maskable and resetable interrupts. Interrupts may be programmed to be pulses or levels, and the GIO interrupt in particular, may be programmed to provide up to 16 additional individually maskable and resetable external event detectors.

GIO INTERFACE

Both the AHA5101 and AHA5121 provide a 16-bit General Input/Output Bus (GIO), which may be used to control and monitor the tape transport or other hardware functions. All bits on the GIO may be programmed as inputs or outputs. If programmed as inputs, they may be further programmed as maskable pulse or level interrupts, which may, among other uses, be implemented to detect rising or falling edges of external signals.

INTERFACE TO DATA COMPRESSION OR ENCRYPTION

The AHA5101 and AHA5121 provide a dedicated port for interface to the AHA3101 (or other) data compression coprocessor. The port consists of two DMA channels which utilize the same byte-wide data bus and separate control lines for concurrent input and output operations. The dedicated port enables the use of "look-aside" mode to simplify data management. No external hardware is needed beyond the SRAM required for dictionary storage by the coprocessor.

TECHNICAL PUBLICATIONS AVAILABLE

The following may be obtained by calling or faxing the AHA Technical Applications Department.

- **Technical Support and Theory of Operations documents for:**
  - —AHA5101/5121 detailed Product Specification
  - —AHA3101 Data Compression Coprocessor IC
  - —AHA4310, AHA4510, AHA4810, AHA4010

ORDERING INFORMATION

PART NUMBER	*DESCRIPTION*
AHA5101A060PQC	Tape Formatter/Controller–single channel
AHA5121A060PQC	Tape Formatter/Controller–dual channel

Advanced Hardware Architectures

The Data Coding Leader

P.O. Box 9669
Moscow, Idaho 83843
Phone: 208.883.8000
FAX: 208.883.8001
BBS: 208.883.8002

PB51X1-1090

11903M