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PRELIMINARY
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ACE1202T
Data Encryption Standard (DES) Transmitter

General Description

The ACE1202T is a customizable transmitter implementing the DES algorithm to encrypt a pulse-width-modulated (PWM) signal transmitted through a radio frequency (RF) module. The ACE1202T together with the ACE1202R[1] form an encoder/decoder chip-set used in high-security applications.

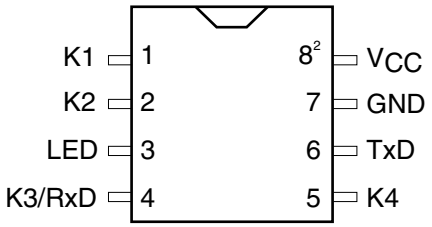
- Remote Keyless Entry (RKE)
- Burglar alarms / Garage door openers
- Individualized recognition / transmission systems.
- Game protection

The ACE1202T is a member of the ACE1202 (Arithmetic Controller Engine) family of microcontrollers. The ACE1202 product family is a dedicated programmable monolithic integrated circuit for applications requiring high performance, low power, and small size. It is a fully static part fabricated using CMOS technology. For additional information regarding the ACE1202 family of microcontrollers please see Fairchild Semiconductor's web site at www.fairchildsemi.com.

Features

- 32-bit DES Encoder
- RF or wired interface
- Up to 4 pushbutton keys
- Programming interface
- Low Power
- Single supply operation (2.2 – 5.5V)
- Low Power Halt Mode (100nA @ 3.3V)
- Integrated Power-on Reset
- Low Battery Voltage Detection
- Brown-out Reset
- Integrated RC oscillator
- Integrated EEPROM
  - 64 bytes of data EEPROM for data storage and options
  - 2K bytes of code EEPROM
  - 40-year data retention
  - 1,000,000 data writes
- 8-pin SOIC package

ACE1202TEM8 Device Pin-out



[1] See the ACE1202R datasheet at www.fairchildsemi.com for details.

[2] Pin 8 must be de-coupled with a 10nF ceramic capacitor to GND.

2.0 Pin Description

2.1 K1 – Pin 1

Transmitter Key 1 (K1) is an active low input with an internal weak pull-up. Pressing K1 sets Bit 7 of the Data Field to '1' keeping track of the active key (see Figure 7.) Once pressed, the ACE1202T exits the low-power HALT mode and sends a NORMAL frame. The NORMAL frame will be transmitted continuously as long as K1 is low or until the transmission timeout expires.

2.2 K2 – Pin 2

Transmitter Key 2 (K2) is an active low input with an internal weak pull-up. Pressing K2 sets Bit 6 of the Data Field to '1' keeping track of the active key (see Figure 7.) Once pressed, the ACE1202T exits the low-power HALT mode and sends a NORMAL frame. The NORMAL frame will be transmitted continuously as long as K2 is low or until the transmission timeout expires.

2.3 K3/RxD – Pin 4

Transmitter Key 3 (K3) is an active low input with an internal weak pull-up. Pressing K3 sets Bit 5 of the Data Field to '1' keeping track of the active key (see Figure 7.) Once pressed, the ACE1202T exits the low-power HALT mode and sends a NORMAL frame. The NORMAL frame will be transmitted continuously as long as K3 is low or until the transmission timeout expires.

If the K3 is pressed after a power-on reset and flag EnaKSync in the OPTION register is set, a SYNC_DES_KEY frame is transmitted transferring the internal DES Key into the ACE1202R EEPROM memory. This special frame will only be sent one time authorizing the transmission of only the NORMAL frames. (See Section 5.0)

In NRZ mode, K3 is used to receive serial information from an external programmer or from ACE1202R.

2.4 K4 – Pin 5

Transmitter Key 4 (K4) is an active low input with an internal weak pull-up. Pressing K4 sets Bit 4 of the Data Field to '1' keeping track of the active key (see Figure 7.) Once pressed, the ACE1202T exits the low-power HALT mode and sends a NORMAL frame. The NORMAL frame will be transmitted continuously as long as K4 is low or until the transmission timeout expires.

If the K4 is pressed after a power-on reset and flag EnaCSync in the OPTION register is set, a SYNC_DES_CNT frame is transmitted transferring the internal DES Counter into the ACE1202R EEPROM memory. This special frame will only be sent one time authorizing the transmission of only the NORMAL frames. (See Section 5.0)

2.5 LED – Pin 3

The LED output is driven in sink mode and is activate during the InterFrame time (with a pause between frames.) This output is also used to indicate a low battery condition (see Section 10.0) by turning on the LED once in a consecutive series of frames.

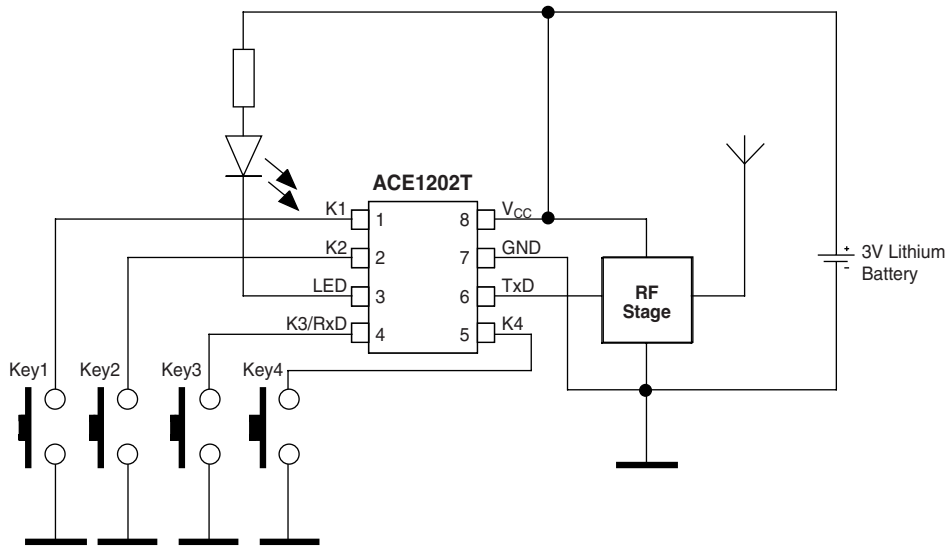
2.6 TxD – Pin 6

TxD is the transmitter output and is used in both the PWM and NRZ communication modes. In PWM mode, TxD is used to send encoded information to an external RF transmitter stage using the PWM coding scheme (1/3 or 2/3). In NRZ mode, TxD is used to transmit serial information to an external programmer or the ACE1202R.

2.7 V_{CC} and GND – Pins 8 and 7

V_{CC} and GND are the power supply lines. The ACE1202T is designed to work with a standard 3.0V lithium battery. It can also work with a 5.0V supply voltage; however, the low-battery threshold is calibrated for only a 3.0V operation.

Figure 2. Transmitter Block Diagram



3.0 Electrical Characteristics

Absolute Maximum Ratings

Ambient Storage Temperature	-65 ºC to +150ºC
Input Voltage	-0.3V to V_{CC}+0.3V
Lead Temperature (10s max)	+300ºC
Electrostatic Discharge on all pins	2000V

Operating Conditions

Ambient Operating Temperatures:	
ACE1202TEM8	-40ºC to +85ºC
Operating Supply Voltage:	
From -40ºC to +85ºC	2.2V to 5.5V
Relative Humidity (non-condensing)	95%
EEPROM write limits	See DC Electrical Characteristics

Preliminary ACE1202TEM8 DC Electrical Characteristics for V_{CC} = 2.2 to 5.5V

All measurements are valid for ambient operating temperature range unless otherwise stated.

Symbol	Parameter	Conditions	MIN	TYP	MAX	Unit
I_{CC}[3]	Supply Current - no data EEPROM write in progress	2.2V 2.7V 3.3V 5.5V		0.4 0.7 1.2 3.7	1.0 1.2 2.0 5.5	mA mA mA mA
I_{CCH}	HALT Mode Current	3.3V @ -40°C to 25°C 5.5V @ -40°C to 25°C 3.3V @ +85°C 5.5 @ +85°C		10 60 75 400	100 1000 1000 2500	nA nA nA nA
V_{CCW}	EEPROM Write Voltage	Data EEPROM in Operating Mode	2.4		5.5	V
S_{VCC}	Power Supply Slope		1µs/V		10ms/V	
V_{IL}	K1, K2, K3/RxD, K4 with Schmitt Trigger buffer	V_{CC} = 2.2 - 5.5V			0.2V_{CC}	V
V_{IH}	K1, K2, K3/RxD, K4 with Schmitt Trigger buffer	V_{CC} = 2..2 - 5.5V	0.8V_{CC}			V
I_{IP}	Input Pull-up Current	V_{CC} = 5.5V, V_{IN} = 0V	30	65	350	µA
I_{TL}	Tri-State Leakage	V_{CC} = 5.5V		2	200	nA
V_{OL}	Output Low Voltage:	V_{CC} = 2.2V - 3.3V				
	TxD	3.0 mA sink			0.2V_{CC}	V
	LED	5.0 mA sink			0.2V_{CC}	V
	Output Low Voltage:	V_{CC} = 3.3 - 5.5V				
	TxD	5.0 mA sink			0.2V_{CC}	V
	LED	10.0 mA sink			0.2V_{CC}	V
V_{OH}	Output High Voltage:	V_{CC} = 2.2V - 3.3V				
	TxD	0.4 mA source	0.8V_{CC}			V
	LED	0.8 mA source	0.8V_{CC}			V
	Output High Voltage:	V_{CC} = 3.3 - 5.5V				
	TxD	0.4 mA source	0.8V_{CC}			V
	LED	1.0 mA source	0.8V_{CC}			V

[3] See Figure 5 for or I_{CC} Active data with EEPROM writes.

Preliminary ACE1202TEM8 AC Electrical Characteristics for V_{CC} = 2.2 to 5.5V

All measurements are valid for ambient operating temperature range unless otherwise stated.

Parameter	Conditions	MIN	TYP	MAX	Unit
Instruction cycle time from internal clock - setpoint	5.0V at + 25°C	0.9	1.0	1.1	µs
Internal cycle voltage-dependent frequency variation	3.0V to 5.5V, constant temperature			±5	%
Internal clock temperature-dependent frequency variation	3.0V to 5.5V, full temperature range			±10	%
Internal clock frequency deviation for 0.5V drop	3.0V to 4.5V, constant temperature			±2	%
EEPROM write time			3	10	ms
Internal clock start up time	(Note 5)			2	ms
Oscillator start up time	(Note 5)			2400	cycles

Preliminary ACE1202TEM8 Low Battery Detect (LBD) Characteristics, V_{CC} = 2.2 to 5.5V

Parameter		Conditions	MIN	TYP	MAX	Unit
LowBattLev	Addr. 0x67	-40°C		2.45		V
EEWriteLev	Addr. 0x68	-40°C		2.2		V
LowBattLev	Addr. 0x67	0°C		2.63		V
EEWriteLev	Addr. 0x68	0°C		2.3		V
LowBattLev	Addr. 0x67	+25°C		2.67		V
EEWriteLev	Addr. 0x68	+25°C		2.44		V
LowBattLev	Addr. 0x67	+85°C		2.87		V
EEWriteLev	Addr. 0x68	+85°C		2.55		V

Preliminary ACE1202TEM8 Brown-out Reset (BOR) Characteristics, V_{CC} = 2.2 to 5.5V

Parameter	Conditions	MIN	TYP	MAX	Unit
BOR Trigger Threshold	-40°C		1.98		V
	0°C		2.06		V
	+25°C		2.12		V
	+85°C		2.27		V

3.1 Preliminary AC & DC Electrical Characteristic Graphs

Figure 3. Internal Oscillator Frequency

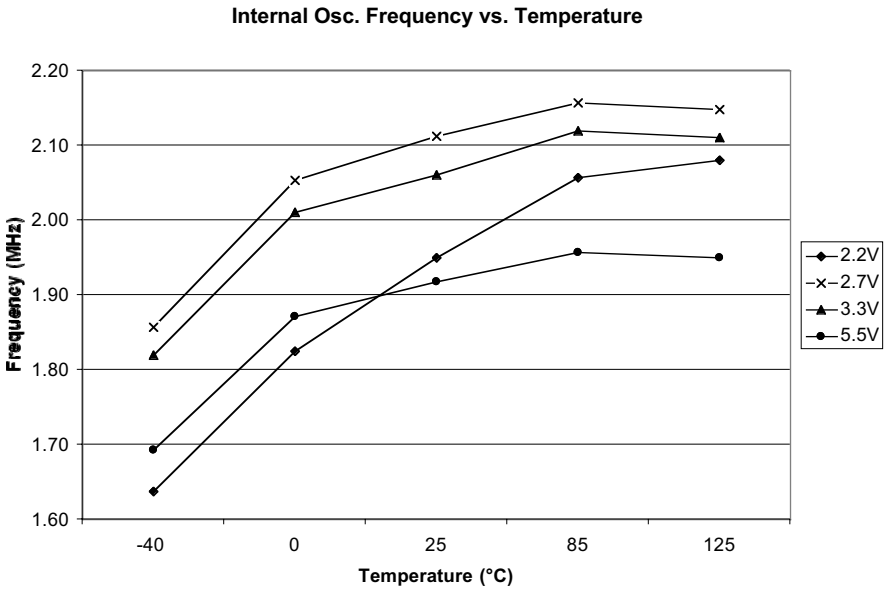
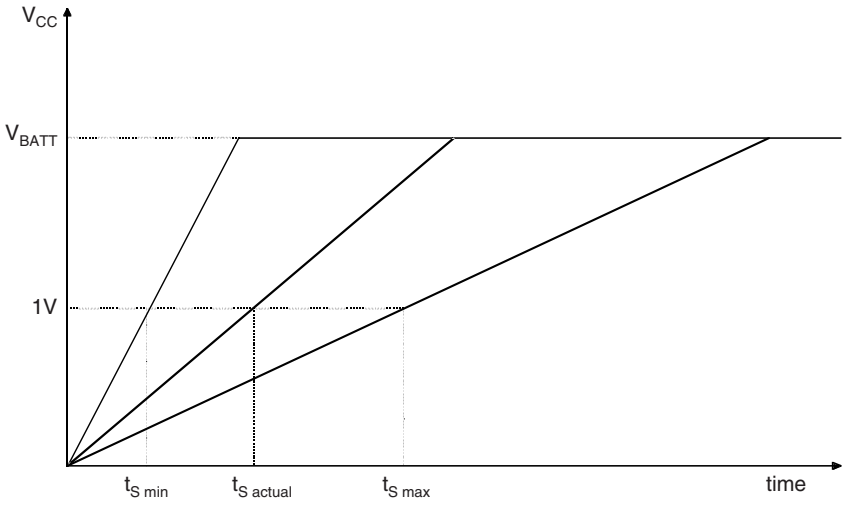
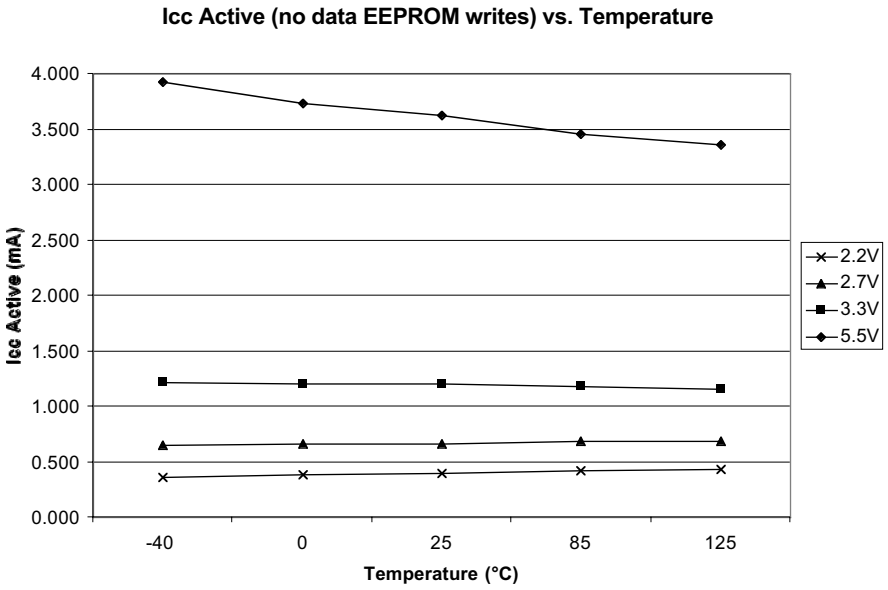


Figure 4. Power Supply Rise Time



Name	Parameter	Unit
V_{CC}	Supply Voltage	[V]
V_{BATT}	Battery Voltage (Nominal Operating Voltage)	[V]
$t_{S\ min}$	Minimum Time for V_{CC} to Rise by 1V	[ms]
$t_{S\ actual}$	Actual Time for V_{CC} to Rise by 1V	[ms]
$t_{S\ max}$	Maximum Time for V_{CC} to Rise by 1V	[ms]
S_{VCC}	Power Supply Slope	[ms/V]

Figure 5. I_{CC} Active



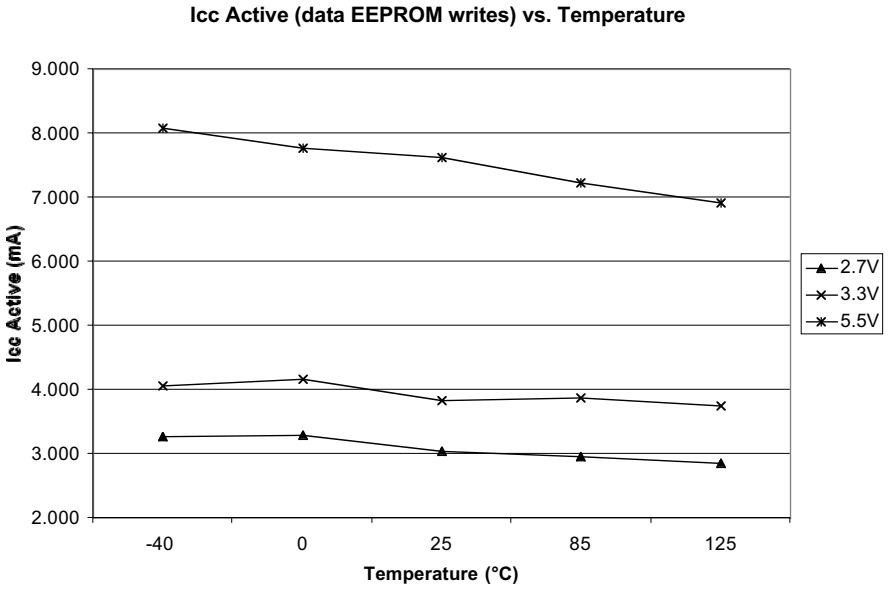
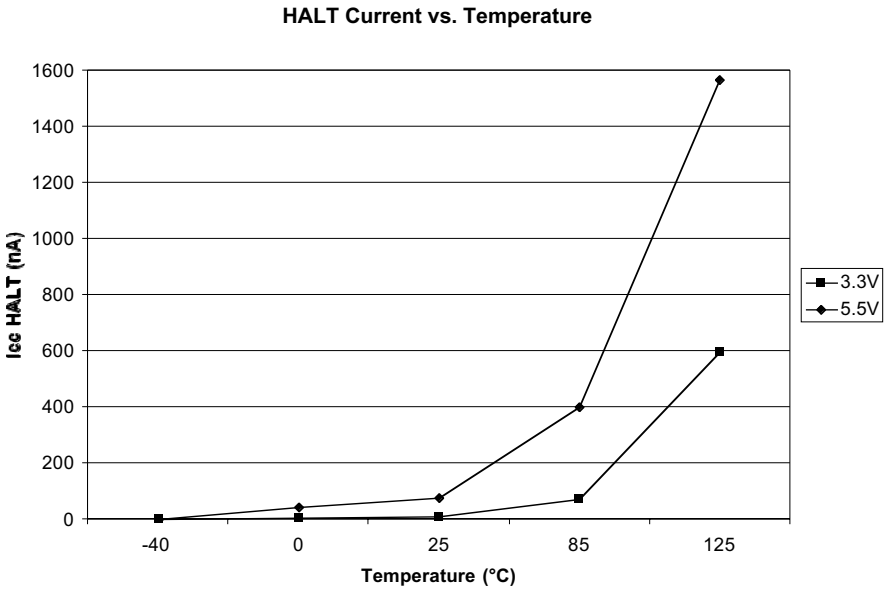


Figure 6. HALT Current



4.0 General Characteristics

The ACE1202T is intended for use with the ACE1202R product. This chip-set forms a secure and inexpensive system for a variety of applications that require a high level of security such as remote keyless entry or software protection.

The basic function of the ACE1202T is to transmit a DES coded frame containing a fixed identifier (24-bit), data field (8-bit), DES code (32-bit), a sequential counter (16-bit), and a parity field. This frame is received in a PWM coded format suitable for a RF system or a NRZ format used in a direct wire connection.[4] This frame will be compared with previously stored information in order to match the fixed and dynamic part of the code message.

4.1 Mode of Operations

The ACE1202T can be programmed to work in three different modes as indicated in Table 5 and as described in later sections.

Table 5 ACE1202T Operating Modes

Operating Modes	Description
PWM Mode	Indicated to work with a RF module
NRZ Mode	Indicated to work with wired connection
Programming mode	To select and program the user-defined area

[4] PWM coding is typically used for a RF transmission, but NRZ coding can also be used. However, the bit rate tolerance is a critical aspect to consider for extracting the correct information. We suggest adopting NRZ mode for wired direct connection.

5.0 DES Message Description

The DES coded message is 12-bytes wide and is divided into fields transmitted in the following order:

- **Preamble** – Sent only once as a continuous series of frames used to wake the receiver from HALT mode.
- **SYNC field** – 8 coded bits for the synchronization of the incoming data stream.
- **Data field** – Contains information about the channel selected and special transmitting modes: DES_KEY and DES_COUNTER. It is 8 bits wide.
- **Fixed field** – A unique 24-bit code that identifies the transmitter.
- **DES field** – The 32-bit DES generated code.
- **Counter field** – The lower 16 bits of the DES Counter.
- **Parity field** – Byte-wise exclusive-or from SYNC Field to DES Field.

The frame type selection bits of the Data field configures the DES field for one of three configurations. The three DES frame configurations are the NORMAL Frame, the SYNC_DES_KEY Frame, and the SYNC_DES_CNT Frame. (See Figure 7)

5.1 SYNC Field

The SYNC field is 8-bits wide and identifies the start of the DES frame.

5.2 Fixed Field

The Fixed Field is three bytes (24-bits) long and is used to identify the individual transmitter. If the Fixed Field is not found in the ACE1202R memory, the frame will be rejected. The ACE1202R must learn the Fixed Field while in a special operating mode.[5]

5.3 Data field

The Data field contains the current configuration of the transmission. Bits 7 to 4 decode the binary transmitter key configuration. The least significant nibble selects the frame type. See Table 6 for details.

Table 6 Data Field Bit Definition

Bit	Value	Description
Bit 7	'1'	KEY1 has been pressed
Bit 6	'1'	KEY2 has been pressed
Bit 5	'1'	KEY3 has been pressed
Bit 4	'1'	KEY4 has been pressed
Bit 3-0	Frame Type Selection:	
	'0000'	NORMAL
	'0010'	DES KEY SYNC
	'0011'	DES COUNTER SYNC
	'1111'	Low Battery

5.4 DES Code field

The DES Code field is the 32 most significant bits of the calculated DES algorithm using the known DES KEY and COUNTER. (See Section 6.0) This field is compared with the DES CODE calculated internally by the receiver. This field is only sent in the NORMAL frame.

5.5 Counter field

The Counter field is the 16 least significant bits of the internal 64-bit DES counter. The counter is used to synchronize the DES operation on the receiver side. This field is transmitted only in the NORMAL frame. This information helps track the current DES progression held in the linear DES COUNTER. Normally, only one calculation is needed to determine the current DES CODE.

5.6 Parity field

The Parity field is present in all the frames and contains the checksum for the frame transmitted. The checksum is the exclusive-or of all bytes received in the frames starting from SYNC field.

5.7 DES KEY field

The DES KEY field is the security DES KEY used in the algorithm to calculate the current DES Code. The four least significant bits in the Data Field indicate to the receiver that a SYNC_DES_KEY frame (0x02) will be received. The receiver will store the DES KEY in the internal register for future NORMAL frame decoding.

The true length of the DES KEY is 56-bits wide. The DES KEY field is 48 bits wide (addr. 0x45 to 0x4A duplicated in addr. 0x75 to 0x7A) and the remaining 8 bits of the DES KEY is a user defined value, stored in memory (addr. 0x4B, duplicated in addr. 0x7B) during factory programming, otherwise it is defaulted to 0x00.

If pin 1 of the ACE1202R is set to logic '0', the receiver will ignore any SYNC Frame requests.

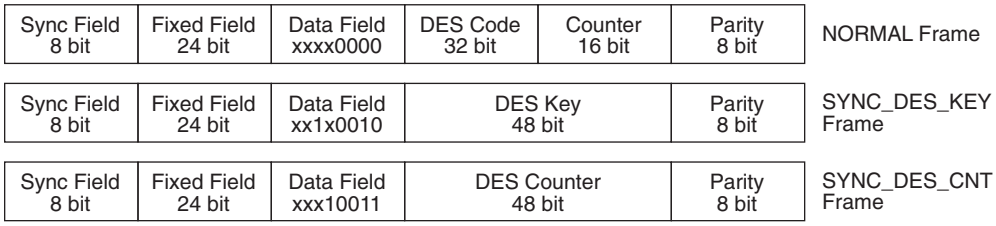
5.8 DES COUNTER field

The DES COUNTER field is the 48-bit DES COUNTER used in the algorithm to calculate the current DES Code. The four least significant bits in the Data Field indicate to the receiver that a SYNC_DES_CNT frame (0x03) will be received. The DES COUNTER will be stored in the internal registers for future NORMAL frame decoding.

The true length of the DES COUNTER is 64-bits long. The DES COUNTER field is 48-bits and the remaining 16 least significant bits are set to '0' every time a SYNC_DES_CNT frame is transmitted. If pin 1 of ACE1202R is set to logic '0', the receiver will ignore any SYNC Frame request.

[5] See Section 7.1 of the ACE1202R datasheet at www.fairchildsemi.com for details.

Figure 7. NORMAL and SYNC Frames



6.0 DES Algorithm

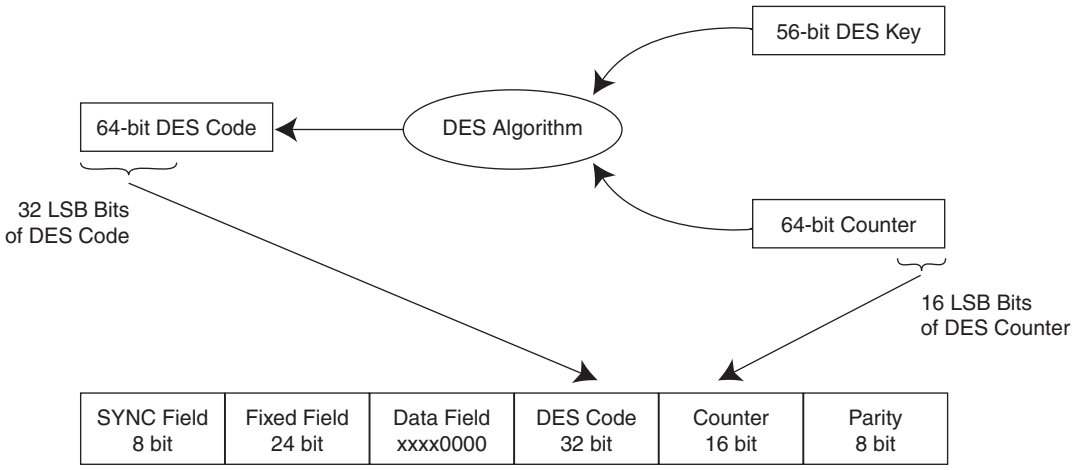
With the help of the National Security Agency the National Bureau of Standards certified the Data Encryption Standard (DES) in 1977 to be used in electronic devices for the protection of coded data during transmission and storage in a computer system or network.

The DES algorithm is different from other cryptographic algorithms in that it is not kept in secret like the others. The DES algorithm is public and the system security is based on a secret key (DES KEY) of 56-bits plus 8-bits of parity known only by the transmitter and receiver. The DES key must be transmitted or directly stored in the transmitter / receiver memory.

The implementation of the DES algorithm used in the ACE1202R and ACE1202T chip-set does not use the initial and final permutations normally used in DES, as there is no benefit in implementing these permutations where DES is used for authentication.

Figure 8 shows how the DES algorithm encodes a 64-bit counter using a 56-bit DES key to obtain the 64-bit DES code.

Figure 8. DES Algorithm data flow



7.0 USER Area:

It is possible to read, write, or protect the user-defined area using a two-wire programming interface. The programming interface operates as a half duplex asynchronous protocol with TxD (Pin 6) and RxD (Pin 4) dedicated lines with communications using the NRZ format. The NRZ format operates at a baud rate of 4800bps and a data frame format of 8 data bits, 1 start bit, and 1 stop bit.

In order to enter programming, mode pins 4 and 6 must be at logic '1' level during power-up. After 500ms the part is ready to accept command from an external programmer. The first message must be a character corresponding to the hex value 0x55 needed to calibrate the internal baud-rate register. Upon reception of the baud adjustment message, ACE1202T will respond with an acknowledge message to inform the external programmer to be ready to receive new messages.

The message structure is variable in length and follows the form:

a) [0x55]: Sent only to ACE1202T

b) Nbytes: The number of bytes to send – 1

c) OpCode: Op-code field

d) Data: Variable field from 1 to 15 bytes depending on op-code

e) Checksum: Logical byte-wise exclusive-or of the previous fields b) to c)

Characters are spaced by a delay of 5ms. Possible messages are:

EEPROM READ (Progr. to ACE1202T)

0x55 + Nbytes + READ_USR_AREA + Addr. + Checksum (To read any location in User Area)

Nbytes = 3
READ_USR_AREA = 0x38

This message is valid only if the **RD_PROTECT** bit is zero in **OPTIONS** address (0x60). If the operation is executed correctly, the **ACE1202R** will return the message:

Nbytes + READ_USR_AREA + Addr. + Read_Value + Checksum, otherwise the message UNKNOWN will be returned.

EEPROM WRITE (Progr. to ACE1202T)

0x55 + Nbytes + WRITE USR_AREA + Addr.+ Value + Checksum (To write any location in User *0x55 +* Area)

Nbytes = 4
WRITE_USR_AREA = 0x93

This message is valid only if the **WR_PROTECT** bit is zero in **OPTIONS** address (0x60). If the operation is executed correctly, the ACE1202R will return the message:

Nbytes + WRITE_USR_AREA + Addr. + Programmed_Value + Checksum, otherwise the message UNKNOWN will be returned.

DES FRAME (ACE1202R to ACE1202T)/DES VALID (ACE1202T to ACE1202R)

[0x55 +] Nbytes + DES_FRAME + FixedHigh + FixedMid + FixedLow + Data + Cnt0 + Cnt1 + DES3 + DES2 + DES1 + DES0 + Checksum (Represent the DES frame to be checked by the internal algorithm see Section 12.0 for more details)

Nbytes = 12
DES_FRAME = *DES_VALID* = 0x5A

If the message has the correct checksum and valid DES code, it will answer with the next DES Code generated by incrementing the DES COUNTER. If the message contains an invalid DES CODE ACE1202T will re-send the same message back to ACE1202R (See Section 12.0).

The 0x55 preamble is sent only from ACE1202R to ACE1202T (DES_FRAME).

DES KEY and COUNTER info (ACE1202R to ACE1202T)

0x55 + Nbytes + DES_PAR + SyncField + FixedHigh + FixedMid + FixedLow + DES_KEY0 + DES_KEY1 + DES_KEY2 + DES_KEY3 + DES_KEY4 + DES_KEY5 + DES_KEY6 + DES_CNT0 + DES_CNT1 + DES_CNT2 + DES_CNT3 + DES_CNT4 + DES_CNT5 + DES_CNT6 + DES_CNT7 + Checksum (See Figure 14a).

Nbytes = 18
DES_PAR = 0x44

This frame is sent when the ACE1202T is not in programmed state (BLANKED) and it is used to store the DES parameters, DES Key, DES Counter and fix code into ACE1202T user area.

STATUS REQUEST (ACE1202R or Progr. to ACE1202T)

0x55 + Nbytes + TX_STAT_REQ + ACE-T_STATE + SW_Revision + Checksum (This message is only sent after PC connection following the inquire (0x55) parameter.)

Nbytes = 4
TX_STAT_REQ = 0x80
ACE-T_STATE = 0x6D-> TX has no DES information stored in memory
ACE-T_STATE = 0xE2 -> TX has DES information stored in memory
SW_Revision: Bit0 to 3 = Data EEPROM revision
Bit4 to 7 = Code Revision

EXIT

0x55 + Nbytes + EXIT + Checksum (To exit from "Programming mode")

Nbytes = 2
EXIT = 0x2B

7.1 Message table

Table 7. NRZ Messages

Message	Byte Sent – 1	Op-Code	Meaning
READ_USR_AREA	3	0x38	Progr to ACE1202T - Read one location at specified address
WRITE_USR_AREA	4	0x93	Progr to ACE1202T – Write data at specified address
DES_FRAME	12	0x5A	ACE1202R to ACE1202T – Send current DES code
DES_PARAM	21	0x5A	ACE1202T to ACE1202R – Next calculated DES code
RX_STAT	3	0x80	ACE1202T to Progr. – Actual ACE1202T status
EXIT	2	0x2B	Progr to ACE1202T – Exit from Progr connection
UNKNOWN	2	0x55	ACE1202T response to invalid messages
DES_VALID	12	0x44	ACE1202R to ACE1202T – Send DES KEY and COUNTER

7.2 Programming recommendations:

ACE1202T and ACE1202R are delivered from the factory with default values loaded into USER Area allowing the designer to perform a test on the parts without data initialization. The programming interface is designed to allow easy in-circuit programming using the 4-wires interface. It is the responsibility of the user to load the appropriate value in the USER Area. It is recommended always to set the Read and Write protection bits prior to terminating the programming process.

If further programming is needed, the Read protection bit should be enabled to avoid external reading of DES information which need to remain secret to avoid system intrusion.

7.3 USER AREA Table

Table 8 USER Area Registers

Addr.	Label	Description	Note[6]
0x40	Free		
0x41-0x71	Sync Field	8 bit Synchronization field	Read/Write
0x42-0x72	FixHigh	24 bit fixed code – High Part	Read/Write
0x43-0x73	FixMid	24 bit fixed code – Mid Part	Read/Write
0x44-0x74	FixLow	24 bit fixed code – Low Part	Read/Write
0x45-0x75	DES_KEY0	56 bit DES KEY – byte 0	Read/Write
0x46-0x76	DES_KEY1	56 bit DES KEY – byte 1	Read/Write
0x47-0x77	DES_KEY2	56 bit DES KEY – byte 2	Read/Write
0x48-0x78	DES_KEY3	56 bit DES KEY – byte 3	Read/Write
0x49-0x79	DES_KEY4	56 bit DES KEY – byte 4	Read/Write
0x4A-0x7A	DES_KEY5	56 bit DES KEY – byte 5	Read/Write
0x4B-0x7B	DES_KEY6	56 bit DES KEY – byte 6 – User Defined.	Read/Write
0x4C-0x7C	DES_KEY_CHECK	DES _K+ FIXED checksum value	Read/Write
0x4D	DES_CNT0_A	64 bit DES Counter – Byte 0	Bank 0 - Read/Write
0x4E	DES_CNT1_A	64 bit DES Counter – Byte 1	Bank 0 - Read/Write
0x4F	DES_CNT2_A	64 bit DES Counter – Byte 2	Bank 0 - Read/Write
0x50	DES_CNT3_A	64 bit DES Counter – Byte 3	Bank 0 - Read/Write
0x51	DES_CNT4_A	64 bit DES Counter – Byte 4	Bank 0 - Read/Write
0x52	DES_CNT5_A	64 bit DES Counter – Byte 5	Bank 0 - Read/Write
0x53	DES_CNT6_A	64 bit DES Counter – Byte 6	Bank 0 - Read/Write
0x54	DES_CNT7_A	64 bit DES Counter – Byte 7	Bank 0 - Read/Write
0x55	DES_CNTA_CHECK	Counter A Checksum	Bank 0 - Read/Write
0x56	DES_CNT0_B	64 bit DES Counter – Byte 0	Bank 1 - Read/Write
0x57	DES_CNT1_B	64 bit DES Counter – Byte 1	Bank 1 - Read/Write
0x58	DES_CNT2_B	64 bit DES Counter – Byte 2	Bank 1 - Read/Write
0x59	DES_CNT3_B	64 bit DES Counter – Byte 3	Bank 1 - Read/Write
0x5A	DES_CNT4_B	64 bit DES Counter – Byte 4	Bank 1 - Read/Write
0x5B	DES_CNT5_B	64 bit DES Counter – Byte 5	Bank 1 - Read/Write
0x5C	DES_CNT6_B	64 bit DES Counter – Byte 6	Bank 1 - Read/Write
0x5D	DES_CNT7_B	64 bit DES Counter – Byte 7	Bank 1 - Read/Write
0x5E	DES_CNTB_CHECK	Counter B Checksum	Bank 1 - Read/Write
0x5F	EEPntr	DES counter pointer (CNT_A or CNT_B)	Read
0x60	OPTIONS	Operation options	Read/Write
0x61	TX_Preamble	Delay between Preamble field and Sync	Read/Write Step 1ms
0x62	TX_InterFrame	Pause between frames	Read/Write Step 1ms
0x63	TX_Timeout	Continuous transmission timeout	Read/Write Step 1s
0x64	LowBattCntr	No. of consecutive low battery samples	Read/Write
0x65	BAUD_ADJ	Adjusted Baud-rate value	Read
0x66	ACETX_STATE	Functional transmitter state	Read/Write
0x67	LowBattLev	Low Battery threshold level	Read[7]
0x68	EEWriteLev	Min. writing voltage	Read[7]
0x69	LowBattLED	LED duration in Low Battery state	Read/Write
0x6A	MaxLBattAct	No. of possible TX activation in Low Battery	Read/Write
0x6B	PWM_Time	Change PWM timing from 256 to 512µs	Read/Write. Step 1µs
0x6C	DataCode	Data Field Sent in NRZ mode	Red/Write
0x6D	Factory Data1	Free	Read/Write
0x6E	Factory Data2	Free	Read/Write
0x6F	Data Revision	Data EEPROM revision	Read
0x70	NumPreamble	Number of PWM bit sent in PREAMBLE	Read/Write

[6] Though some location are indicated as Read only it is still possible to change its contents, however, we recommend to not modify these values unless agreed with Fairchild.
[7] These locations are factory calibrated and must not be changed to avoid incorrect low-battery detection.

7.4 OPTIONS Register (Addr. 0x60)

Bit 0 – EnaKSync

If set to '1,' the DES KEY synchronization frame will never be sent. The ACE1202R must be factory-coupled with the ACE1202T or programmed with a wire connection. If set to '0,' the DES KEY is sent only one time after a power-up condition (pressing K3).

Bit 1 – EnaCSync

If set to '1,' the DES COUNTER synchronization frame will never be sent. The ACE1202R must be factory-coupled with the ACE1202T or programmed with a wire connection. If set to '0,' the DES COUNTER is sent only one time after a power-up condition (pressing K4).

Bit 2 – DisTimeOut

If set to '1,' no timeout condition exists when a key is continuously pressed. Tranmission will stop as soon as no key is pressed. If set to '0,' the timeout is determined by TX_Timout in seconds.

Bit 3 – SetPWMTime

If set to '1,' the PWM clock timing is defined by the PWM_Time register (0x6B) and can vary from 256 to 512µs. If set to '0,' the PWM timing is fixed to 500µs.

Bit 4 – ForceNRZ

When this bit is set to '1,' the ACE1202T enters the NRZ mode regardless the port level on TxD and RxD after a power-on reset. This option can be used when the only mode requested is NRZ and save external pull-ups on RxD and TxD pins.

Bit 5 – unused

Bit 6 – RD_PROTECT

If set to '1,' reads to the USER area registers are no longer possible. Once this bit set to '1,' this register cannot be written to again.

Bit 7 – WR_PROTECT

If set to '1,' writes to the USER area registers are no longer possible. when the write protection option is disabled and read protection is enabled, an external write operation will force a read of the same location for verification.

Figure 9. OPTIONS Register Bit Definition

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
WR_PROTECT	RD_PROTECT	X	ForceNRZ	SetPWMTime	DisTimeOut	EnaCSync	EnaKSync

7.5 Register TX_Preamble (Addr. 0x61)

TX_Preamble determines the pause between the PREAMBLE field and the SYNC field. It must be defined according to receiver's characteristics (wakeup time, RF sensitivity). The Preamble is sent during the first frame only, with a correction step of 1ms.

7.6 Register TX_InterFrame (Addr. 0x62)

TC_InterFrame determines the pause between consecutive frames. During this time the LED is switched ON with a correction step of 1ms.

7.7 Register TX_Timeout (Addr. 0x63)

TX_Timeout defines the maximum transmission time when a key is pressed continuously. If the DisTimeOut bit in the OPTION register is set, the timeout in infinite (as long as the key is pressed).

7.8 Register LowBattCntr (Addr. 0x64)

LowBattCntr defines the number of low battery consecutive samples, minus one, before entering the *'Low Battery'* state. The counter is reset every time the battery voltage is above the low battery threshold (defined in LowBattLev Register). (Refer to the Low Battery Detect's electrical specification.)

7.9 Register Baud_ADJ (Addr. 0x65)

The BAUD_ADJ register contains the auto-adjusted baud rate value. This value is automatically written after a connection with an external programmer; therefore re-writing this register is not recommended.

7.10 Register ACETX_STATE (Addr. 0x66)

ACETX_STATE represents the transmitter's actual state. It contains the value 0x6D if no DES parameters are stored in the USER area (blank from factory). Once the DES information is transferred into the user area, the external programmer must take care to write the value 0xE2 into this location.

If during a normal operation the DES fix blocks (0x40 - 0x4C and 0x71 - 0x7C) are invalid, the transmitter will write 0x6D in ACETX_STATE while waiting for an external programmer connection.

7.11 Register LowBattLev (Addr. 0x67)

LowBattLev determines the voltage threshold where the battery in use is considered low. The value is chosen to match 3.0V lithium battery characteristics in order to guarantee as many writing operations as defined in register **LowBattCntr** before entering the *Disable State*. (Refer to the Low Battery Detect's electrical specification.)

7.12 Register EEWriteLev (Addr. 0x68)

EEWriteLev determines the lowest voltage level that data EEPROM writes can occur. When the battery voltage is above this limit, a write operation into the data EEPROM is possible, otherwise the writes are skipped. (Refer to the Low Battery Detect's electrical specification.)

7.13 Register LowBattLED (Addr. 0x69)

LowBattLED determines the duration of the LED flashes when the ACE1202T is in the Low Battery State (the correction step is 1ms). During this state, the LED will flash only once in a continuous series of frames.

7.14 Register MaxLBattAct (Addr. 0x6A)

Once ACE1202T is in the Low Battery State, MaxLBattAct detemines the number of new transmissions, minus one, before entering the *Disabled State* (no transmission) while waiting for the battery to be replaced. (Refer to the Low Battery Detect's electrical specification.)

7.15 Register PWM_Time (Addr. 0x6B)

When bit *SetPWMTime* in the **OPTIONS** register is set, **PWM_Time** determines the PWM clock timing used to send the frames. The formula to obtain the PWM clock is $10^6 / (256 + PWM\_Time)$ *in Hertz.* (See Section 8.0)

7.16 Factory Data1 to 3 (0x6D to 0X6F)

These unused locations could be programmed to hold User Factory information such as production date to track lot and testing information.

7.17 Software Revision (0x6F)

Contains the EEPROM data version (0 to 0xF) and can be read through an external programmer by asserting an Inquire command (0x55). Only bits 0 to 3 are used, always keep the remaining bits to '0.'

7.18 NumPreamble (0x70)

NumPreamble determines the number of PWM coded zeros sent in the PREAMBLE field. This allows for the adaptation of the ACE1202R wakeup time when the Receiver Switched Mode[9] supply is used.

[9] See Section 10.0 of the ACE1202R datasheet at www.fairchildsemi.com for details.

8.0 PWM Mode

The Pulse Width Modulation (PWM) Mode works in those applications where the tolerance of the coded signal must be large, such as in RF transmission. The bit coding is defined as 1/3 or 2/3 duty to distinguish between a coded '0' and a coded '1' respectively (see Figure 10).

If the Set PWMTime bit in the OPTIONS register is '0,' each coded bit is created in three phases for a total of 1.5ms (PWM clock = 2kHz). If it is set to '1,' the PWM clock is 10^6 / (256 + PWM_Time).

The ACE1202T, after a power-on reset, samples the K3/RxD and TxD lines. If one or both lines are low the device enters the PWM mode. The device then loads the DES counters from the USER area into working memory. If both DES counters are invalid, the device stops waiting for external programming connection. The address 0x66 will then be loaded with the value 0x6D to inform the external programmer (or ACE1202R) that the transmitter is not programmed. (The same process is applied to the DES KEY fix parameter.)

When valid DES KEY and COUNTER are found in the USER area, the ACE1202T will start the normal PWM operation waiting for a key depression to send the appropriate frame. As long as the electronic keys are not pressed, the ACE1202T will remain in HALT mode.

After power-on reset, it is also possible to send synchronization frames if bits *EnaKSync* and *EnaCSync* in the OPTIONS register are both set to '0.' This allows the ACE1202R to receive and store the needed DES parameter in order to decode incoming NORMAL frames. The ACE1202T can send only a series of synchronization frames by depressing K3 to send the DES KEY message (DataField = 0x23) or K4 to send the DES COUNTER message (DataField = 0x12). A new transmission, using the same key, will send NORMAL frames encoding the key depressed information in the Data field.

To send a new SYNC frame it is necessary to remove the battery, assuring that the internal capacitors are discharged, to issue a new power-on reset to the ACE1202T.

Once the key is pressed, the ACE1202T will exit from HALT mode, increment the DES COUNTER, and send the NORMAL frames.

The preamble is the first field sent and is a series of PWM coded zeros. The number of preamble bits is defined in the NumPreamble register (0x70). After the ACE1202T transmits the preamble, a pause (no carrier) is followed. The length of the pause is defined by the TX_Preamble register. The preamble is sent only during the first frame.

The transmission frame start with 8-bit SyncField used by the receiver to recognize the arrival of a new frame in order to synchronize the bit shift in to the receiving buffer.

The next field sent is the Fixed code used to identify a unique transmitter. The Fixed code is 24-bits long transmitted from MSB to LSB. If the frame is NORMAL, SYNC KEY, SYNC COUNTER, and if ACE1202T is in the *Low Battery* State, the Fixed code is followed by the Data field which contains the stored key(s) depression information.

Depending on the information sent in the Data field, the rest of the frame assumes the following meaning:

If Data field = NORMAL Frame
- 32-bit of DES Code (from MSB to LSB)
- 16-bit DES COUNTER lower part (from MSB to LSB)
- 8-bit Parity Field (byte-wise exclusive of all previous fields excluding PREAMBLE)

If Data field = SYNC KEY Frame
- 48-bit of DES KEY (from MSB to LSB)
- 8-bit Parity Field (byte-wise exclusive of all previous fields excluding PREAMBLE)

If Data field = SYNC COUNTER Frame
- 48-bit of DES COUNTER (from MSB to LSB)
- 8-bit Parity Field (byte-wise exclusive of all previous fields excluding PREAMBLE)

After sending a complete frame there will be a pause, determined by the TX_InterFrame register, where the LED will be activated. At the end of the pause the key(s) are sampled again. If no key is depressed, the ACE1202T will return to HALT mode; otherwise, the frame will be repeated until the keys are released or a transmission timeout is reached (defined by the TX_Timeout register). If the *DisTimeOut* is set, the transmission of the same frame will be repeated until all keys are released.

Figure 10. PWM Encoding Bits

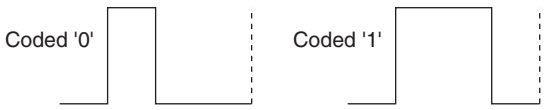
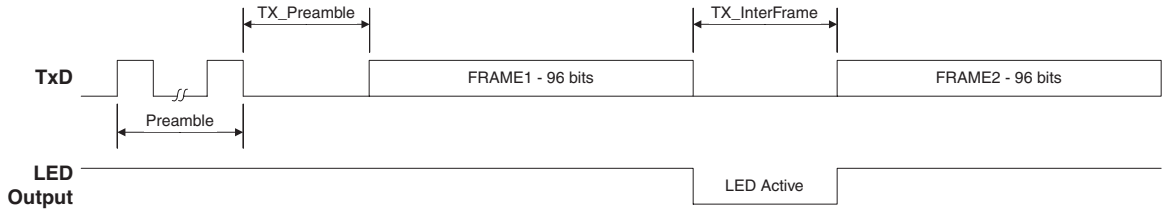


Figure 11. Frames Transmission and Preamble



Note: The number of pulses in the Preamble is defined in NumPreamble (0x70) register.

9.0 Battery Management

Each time a key is pressed, the ACE1202T will sample the Low Battery Detect (LBD) comparator output where the threshold level is defined in the LowBattLev register. If the battery voltage is lower than the selected threshold level, the LowBattCntr register is decremented. When it reaches zero, the Low Battery State is asserted. If the voltage is found above the threshold level, the LowBattCntr is set to the initial counting value regardless of the number of low-battery samples found.

Once in the Low Battery State, the following operation will be executed:

1. The LED will be activated only during the first frame. The duration is determined in the LowBattLED register.
2. The Data field lower nibble is set to '1111.'
3. A new threshold will be applied on LBD comparator to detect for a battery replacement. This threshold is fixed and corresponds to 2.8 - 2.9V.
4. The MaxLBattAct register is decremented.
5. The DES COUNTER is no longer updated in the data EEPROM only RAM.

On a new key activation, the battery voltage will be compared with the new threshold. If the battery is replaced and the level is above the new threshold, the ACE1202T will automatically reset and resume its normal operation. However, a new key must be pressed to clear the low battery condition.

If the battery is still low, the MaxLBattAct is decremented. When it is one, the ACE1202T will enter in a Disabled State where no further transmission is possible. Once in the Disabled State, the only process working is the battery replacement check. If a new battery is put in place, the process restarts at the second key activation.

When the ACE1202T battery is replaced, it is possible that a Power-on Reset will happen and the DES COUNTER copied to RAM is lost. To prevent this situation, at every Power-on Reset, the value of the DES COUNTER loaded from USER Area is added with the value defined in MaxLBattAct plus 16 since the DES counter is updated in EEPROM every 16 cycles to minimize the EEPROM writing operation.

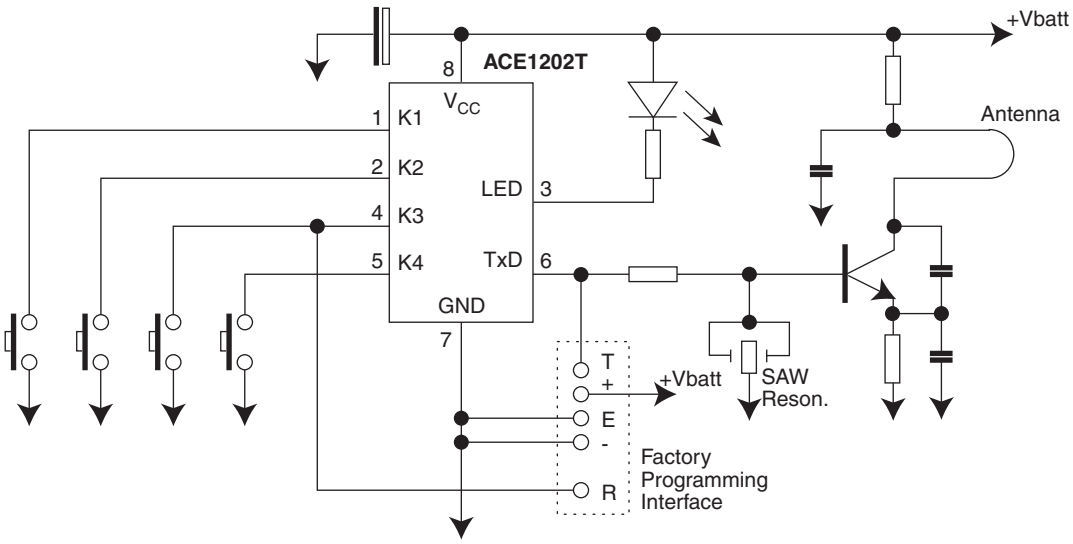
10.0 Typical RF application circuit:

Figure 12 shows the ACE1202T used in a RF transmitter with four buttons. The message is sent with CW modulation of a carrier frequency generated by the RF output stage with a SAW resonator.

The SAW resonator must be chosen in accordance with the local frequency allocation (433.92MHz for Europe, 315MHz for North America).

The transmitter uses the programming interface if the User Area is loaded after the PCB assembly or if the DES information is programmed into the ACE1202T with a wire connection not through the SYNC frame. The signal E is used by the ACE1202R to activate the NRZ mode and can be omitted in the other case (User Area programming only).

Figure 12. RF Transmitter schematic with Programming Interface



11.0 NRZ MODE (Bidirectional)

The NRZ mode is suited for wired operating applications, such as software protection, where the transmitter unit (ACE1202T) can be connected through a dedicated connector to the receiver (ACE1202R).

To enable the NRZ mode, pins 4 and 6 must be high for at least 200ms following a Power-on Reset.

Upon connection, the transmitter senses a polling message coming from the ACE1202R TxD line on pin 4 (K3/RxD). The polling message contains two bytes. The transmitter uses the first byte (0x55) of the polling message to auto-calibrate its internal baud-rate. The second byte is a request from the receiver for the transmitter's STATUS information. Once the transmitter is calibrated, the STATUS information is sent.

The status value can be:

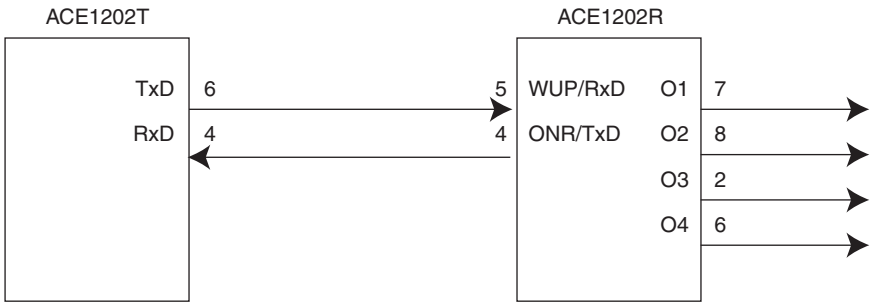
PROGRAMMED (Internal codes stored in ACE1202T)
BLANKED (Not yet coupled with ACE1202R)

If ACE1202R is connected to a BLANKED transmitter, it will automatically send a frame containing the Fixed Code, DES KEY, and DES Counter. In order to send the DES information, the bit DESPar in the OPTIONS register must be set to '1.' The ACE1202T will store this information in its user area and will reply to the ACE1202R with a new status message informing the receiver of the change to PROGRAMMED mode. Once this information is received, the ACE1202R will periodically transmit a STATUS request message (0x55) to the transmitter. (The timing is defined in register RXAWAKE with a 50ms step size.)

The ACE1202T will use the STATUS request message to adjust the internal baud rate and answer with its internal status. At this point, the ACE1202T responds with PROGRAMMED. The ACE1202R will then send the DES coded message [DES_FRAME] corresponding to the actual value of the DES Counter. The ACE1202T will compare the information received with its internal DES code. If a match is found, the next DES code (obtained by incrementing the internal DES Counter) will be sent back to ACE1202R for validation. If there is no match with the DES code sent from the ACE1202R, the same code will be sent back.

Once a validation cycle has completed, the value received in the Data field (bit7 to 5) is put into the ACE1202R output ports (O1 to O4).

Figure 13. NRZ Connection



12.0 Connection messages

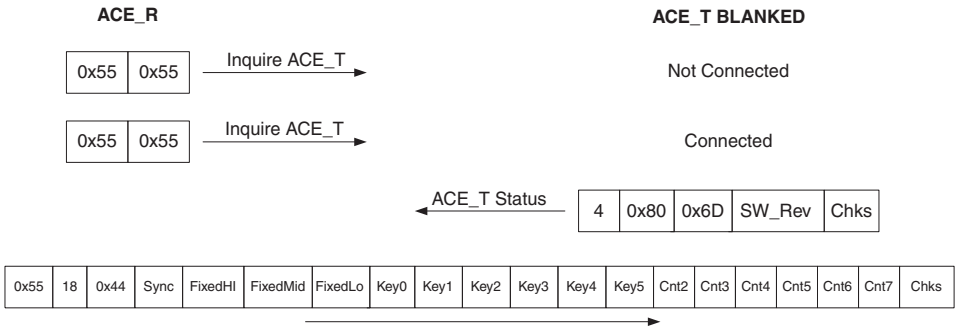
Figure 14 shows the communication protocol between the ACE1202T and the ACE1202R. The ACE1202R continuously sends an Inquire message (0x55) to the ACE1202T until the transmitter answer with its STATUS information. When a BLANKED ACE1202T is connected, the ACE1202R provides the DES Information needed to perform the DES algorithm[10]. The ACE1202T will store the DES KEY and COUNTER and change its state to PROGRAMMED.

[10] Bit DESPar in the OPTIONS register must be set to '1.' (Refer to ACE1202R datasheet for details.)

When the next Inquire message is received by the ACE1202T, it will inform the ACE1202R that it is in the PROGRAMMED state. The ACE1202R will then send the next DES code for validation by ACE1202T. If the DES Code is acknowledge, the ACE1202T will reply with the next DES Code (DES COUNTER is incremented by one) for validation by ACE1202R. After the ACE1202R DES Code is validated, the DES COUNTER is updated. Otherwise, the old value is maintained and the Data field contents will be placed on the outputs (O1-O4.) The Data field is loaded with the contents of the DataCode register (0x6C) defined in the ACE1202T USER Area.

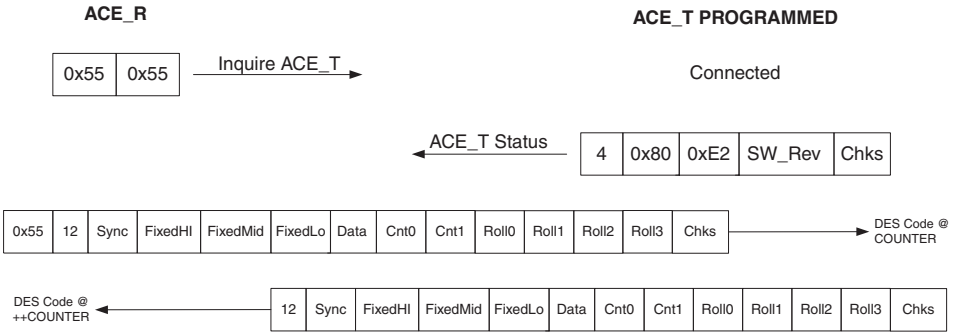
Figure 14. ACE1202T (ACE_T) with ACE1202R (ACE_R) connection

a) Communicating with a BLANKED ACE_T



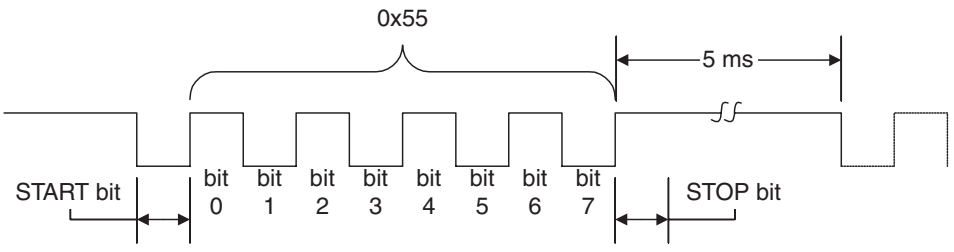
ACE_T will store the DES information changing the state to PROGRAMMED

b) Communicating with a PROGRAMMED ACE_T



Cycle is repeated sending another Inquire TX command

c) Serial data protocol



Note: All the bytes transmitted or received must be spaced at least 5ms apart.

13.0 Application Circuits

13.1 2-Wire Connection[11]

The circuit in Figure 15, shows how to implement a simple 2-wire connection between the ACE1202T and the ACE1202R.

The line 'A' carries power supply and data information that is roughly one-volt modulation over the established DC voltage level. The power is delivered from the receiver unit while the transmitter acts as a passive key. If needed, the supply source can be inverted (the ACE1202T is the source and the ACE1202R is the passive element).

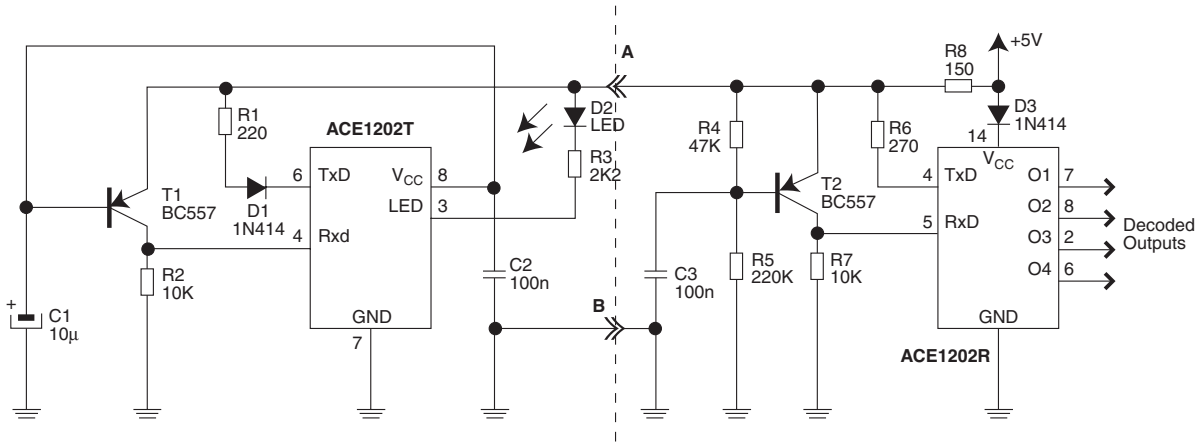
Capacitor C1 delivers current to ACE1202T during the message modulation, on both ACE1202T and ACE1202R, and it is the key element to demodulate information sent.

After connection, C1 is charged from R8 in a time faster than 50ms (this time required for the internal Power-on Reset circuit to operate correctly). After connection, both circuits (ACE1202T and ACE1202R) detect a NRZ connection mode reading '1' on respective RxD and TxD lines. At this moment ACE1202R starts to interrogate ACE1202T with message 0x55 until it receives a status response from ACE1202T. The process continues as indicated in Section 11.0.

The proposed circuit does not provide electrical protection in case the boards are connected to a non-compatible soure or extreme electrical noise.

The LED informs the user about the correct DES algorithm acknowledge and DES parameter stored. The use of this LED is optional.

Figure 15. ACE1202T/ACE1202R 2-wire connection

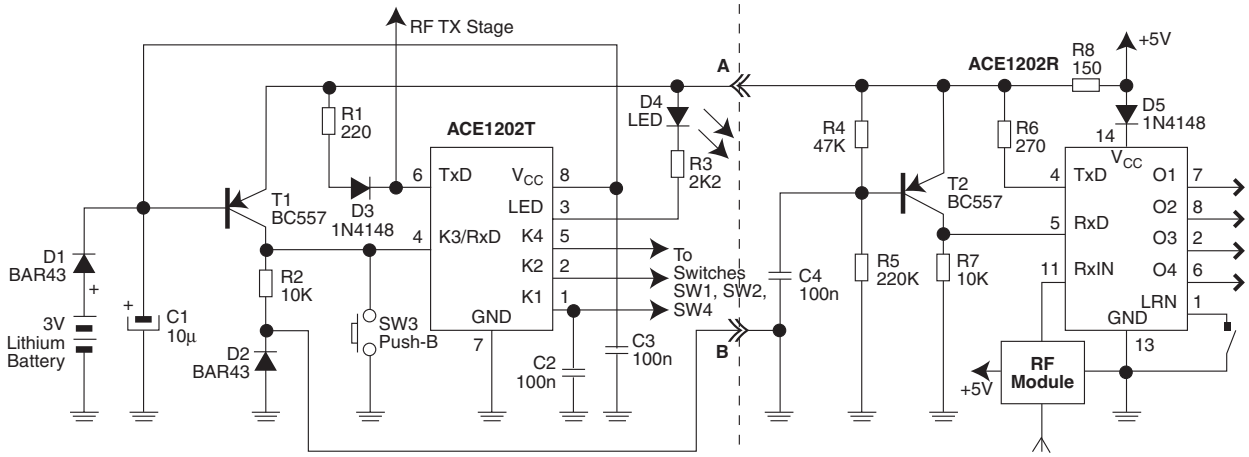


[11]Component values and schematic not tested in a real application.

13.2 RF RKE system with active/passive transmitter

Using the same 2-wire interface described in Section 13.1, it is possible to build a RKE system that allows the ACE1202T to send information in PWM mode using the RF link or act as a passive key if connected through the 2-wire connection in NRZ mode. The passive functionality could be employed as emergency enable/disable of the system or to program DES information into the ACE1202T user area. In this case, the secret information is not sent through the RF channel.To enable this possibility, pin 1 (LRN) of the ACE1202R must be connected to GND. The system can work with or without a battery on the transmitter battery-holder.

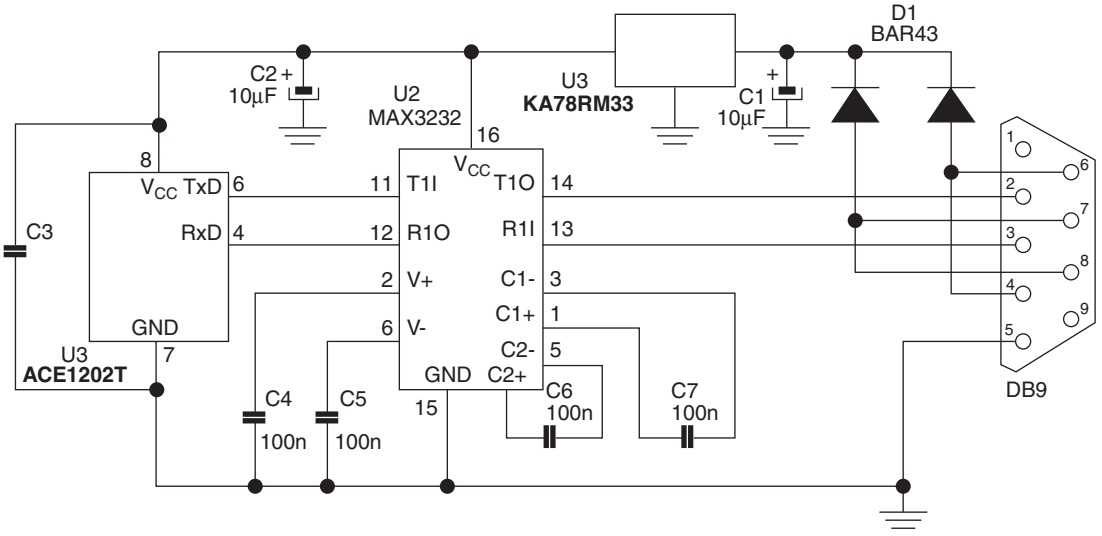
Figure 16. RKE System with 2-wire interface



13.3 Dongle Key (Coded Entry Protect)

The ACE1202 low power consumption makes it possible to realize a dongle key connected to a PC serial port. The power supply is taken from the RS232 handshake lines (CTS-RTS and DSR-DTR) not used in the communication protocol between the ACE1202T and the PC software. The PC software acts as an ACE1202R unit, described in Section 11.0, programming and verifying the DES code exchanged from the two systems. This system can be used in software protection for user validation or access control.

Figure 17. Dongle Key

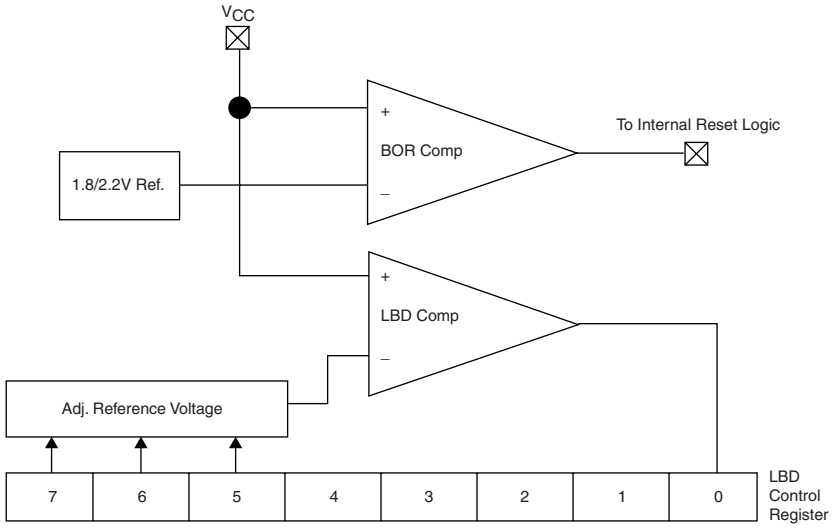


14.0 Brown-Out Reset

The Brown-Out Reset (BOR) function is a standard feature of the ACE1202 Product Family used to hold the device in reset when V_{CC} drops below a fixed threshold. (See BOR Electrical Characteristics for the threshold voltage.) While in reset, the device is held in its initial condition until V_{CC} rises above the threshold voltage, when an internal reset sequence is started. After the reset sequence, the core fetches the first instruction and starts normal operation.

The BOR should be used in situations when V_{CC} rises and falls slowly and in situations when V_{CC} does not fall to zero before rising back to its operating range. The BOR can be thought of as a supplemental function to the Power-On Reset when V_{CC} does not fall below ~1.5V. The Power-On Reset circuit works best when V_{CC} starts from zero and rises sharply. So in applications where V_{CC} is not constant the BOR will provide added device stability.

Figure 18. BOR/LBD Block Diagram

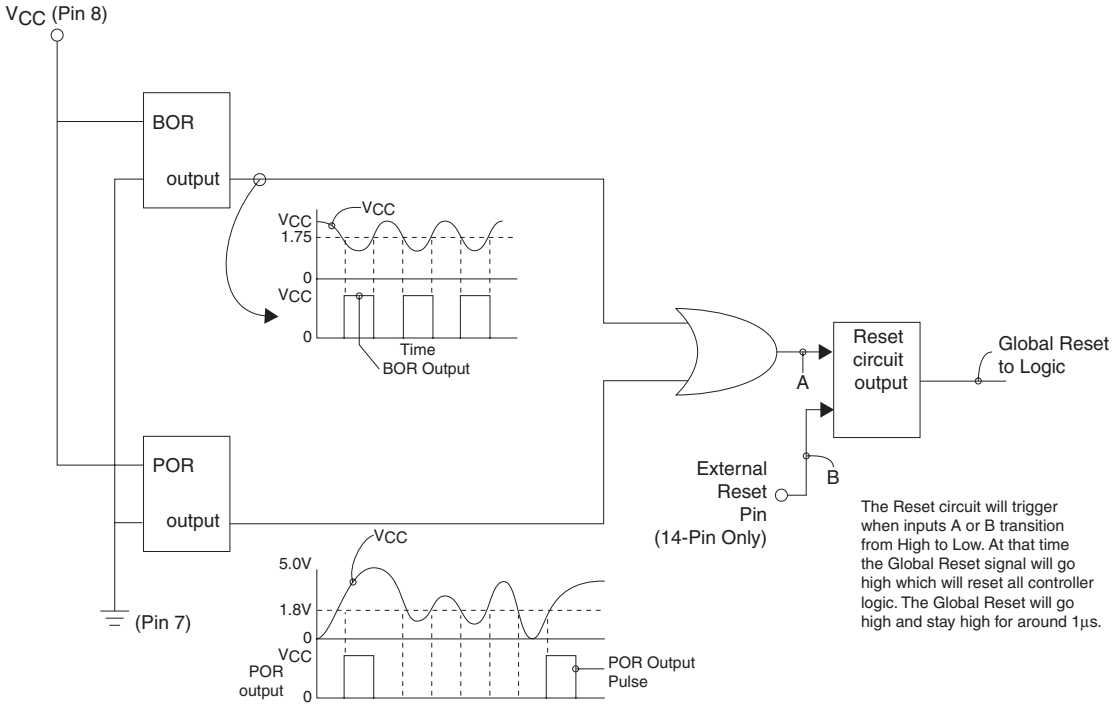


15.0 Power-on Reset

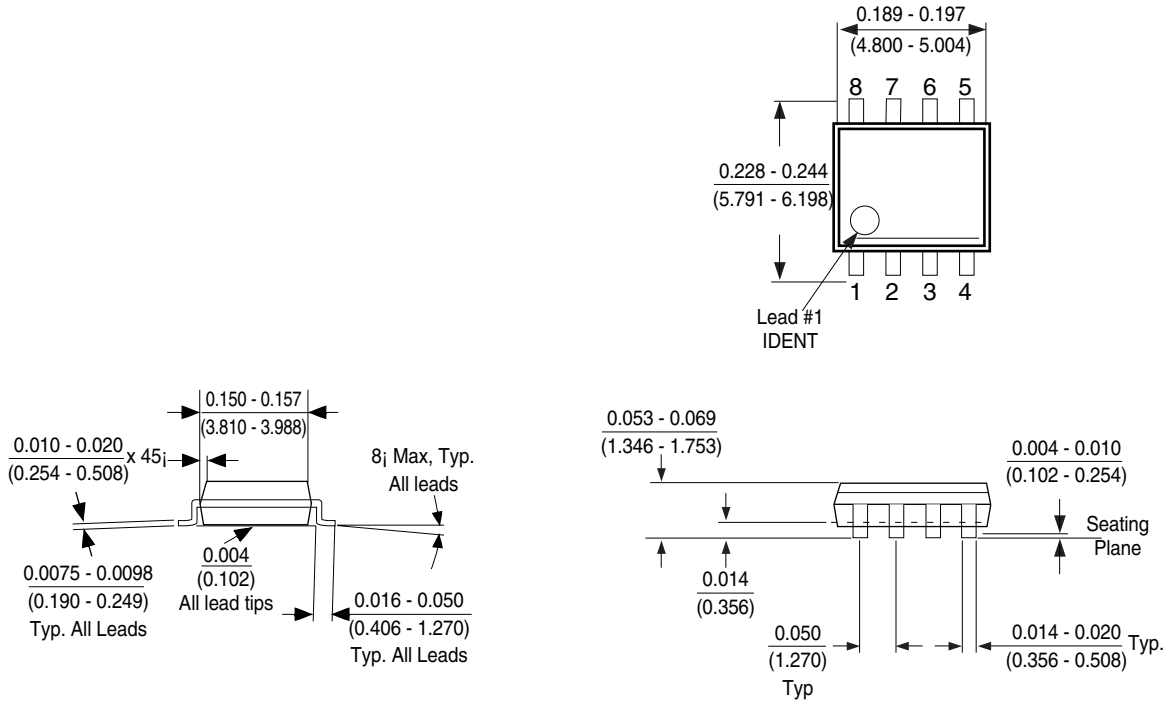
The Power-On Reset (POR) circuit is guaranteed to work if the rate of rise of V_{CC} is no slower than 10ms/1volt. The POR circuit was designed to respond to fast low-to-high transitions between 0V and V_{CC}. The circuit will not work if V_{CC} does not drop to 0V before the next power-up sequence. In applications where 1) the V_{CC} rise is slower than 10ms/1 volt or 2) V_{CC} does not drop to 0V before the next power-up sequence, the external reset option should be used.

The external reset provides a way to properly reset the ACE1202R if POR cannot be used in the application. The external reset pin contains an internal pull-up resistor. Therefore, to reset the device, the RESET pin should be held low for at least 2ms so that the internal clock has enough time to stabilize.

Figure 19. BOR and POR Circuit Relationship Diagram



Physical Dimensions inches (millimeters) unless otherwise noted



Molded Small Outline Package (M8)
Order Number ACE1202TEM8
Package Number M08A

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