REVISIONS			
LTR	DESCRIPTION	DATE (YR-MO-DA)	APPROVED
A	Updated boilerplate. Make corrections to Table I and waveforms. Add case outline "Y". Editorial changes throughout.	94-09-06	M. A. Frye
B	Updated boilerplate. Added device types 04-06. - glg	98-11-05	Raymond Monnin

THE ORIGINAL FIRST PAGE OF THIS DRAWING HAS BEEN REPLACED.

REV																				
SHEET																				
REV	B	B	B	B	B	B	B	B	B	B	B	B	B	B	B	B	B	B	B	
SHEET	15	16	17	18	19	20	21	22	23	24	25	26	27	28	29	30	31	32	33	

REV STATUS OF SHEETS	REV	B	B	B	B	B	B	B	B	B	B	B	B	B	B	B
	SHEET	1	2	3	4	5	6	7	8	9	10	11	12	13	14	

PMIC N/A

STANDARD MICROCIRCUIT DRAWING

THIS DRAWING IS AVAILABLE FOR USE BY ALL DEPARTMENTS AND AGENCIES OF THE DEPARTMENT OF DEFENSE

AMSC N/A

PREPARED BY
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DRAWING APPROVAL DATE
93-10-27

REVISION LEVEL
B

DEFENSE SUPPLY CENTER COLUMBUS
COLUMBUS, OHIO 43216-5000

MICROCIRCUIT, MEMORY, DIGITAL, CMOS,
64K X 4 DRAM, MONOLITHIC SILICON

SIZE	CAGE CODE	
A	67268	**5962-92132**

SHEET 1 OF 33

DSCC FORM 2233
APR 97

5962-E535-98

DISTRIBUTION STATEMENT A. Approved for public release; distribution is unlimited.

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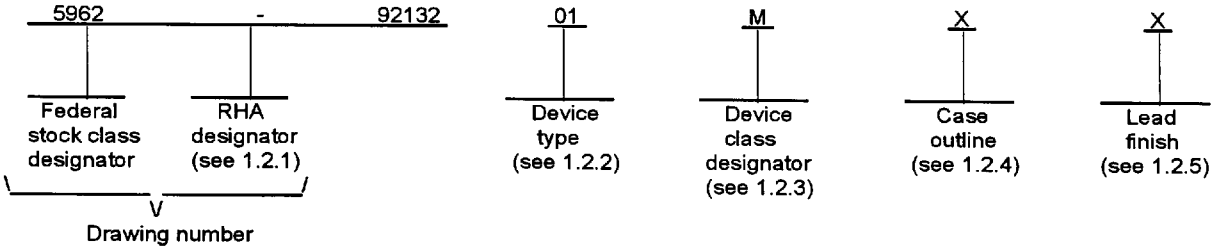
1. SCOPE

1.1 Scope. This drawing documents two product assurance class levels consisting of high reliability (device classes Q and M) and space application (device class V). A choice of case outlines and lead finishes are available and are reflected in the Part or Identifying Number (PIN). When available, a choice of Radiation Hardness Assurance (RHA) levels are reflected in the PIN.

1.2 PIN. The PIN shall be as shown in the following example:



1.2.1 RHA designator. Device classes Q and V RHA marked devices meet the MIL-PRF-38535 specified RHA levels and are marked with the appropriate RHA designator. Device class M RHA marked devices meet the MIL-PRF-38535, appendix A specified RHA levels and are marked with the appropriate RHA designator. A dash (-) indicates a non-RHA device.

1.2.2 Device type(s). The device type(s) shall identify the circuit function as follows:

Device type	Generic number 1/	Circuit function	Access time	Refresh
01,04	4C4067	64K x 4 bit DRAM	100 ns	256 cycles (4 ms)
02,05	4C4067	64K x 4 bit DRAM	120 ns	256 cycles (4 ms)
03,06	4C4067	64K x 4 bit DRAM	150 ns	256 cycles (4 ms)

1.2.3 Device class designator. The device class designator shall be a single letter identifying the product assurance level as follows:

Device class	Device requirements documentation
M	Vendor self-certification to the requirements for non-JAN class B microcircuits in accordance with MIL-PRF-38535, appendix A
Q or V	Certification and qualification to MIL-PRF-38535

1.2.4 Case outline(s). The case outline(s) shall be as designated in MIL-STD-1835 and as follows:

Outline letter	Descriptive designator	Terminals	Package style
V	GDIP1-T18	18	Dual-in-line
X	See figure 1	18	Leadless chip carrier
Y	See figure 1	18	Leadless chip carrier

1.2.5 Lead finish. The lead finish is as specified in MIL-PRF-38535 for device classes Q and V or MIL-PRF-38535, appendix A for device class M.

1/ Generic numbers are listed on the Standard Microcircuit Drawing Source Approval Bulletin at the end of this document and will also be listed in MIL-HDBK-103 (see 6.6.2 herein).

1.3 Absolute maximum ratings. 2/

Supply voltage range on any pin	-1.5 V dc to 7.0 V dc
Short circuit output current	50 mA
Maximum power dissipation (P_D)	1.0 W
Storage temperature range	-65°C to +150°C
Lead temperature (soldering, 10 seconds)	+300°C
Thermal resistance, junction-to-case (θ_{JC}):	
Case V	See MIL-STD-1835
Case X and Y	50°C/W
Junction temperature (T_J)	+150°C

1.4 Recommended operating conditions.

Supply voltage range (V_{CC})	+4.5 V dc to +5.5 V dc
Power supply and signal reference (V_{SS})	0.0 V dc
High level input voltage range (V_{IH})	2.4 V dc minimum to 6.5 V dc maximum
Low level input voltage range (V_{IL})	-1.0 V dc minimum to 0.8 V dc maximum
Case operating temperature range (T_C)	-55°C to +125°C
Refresh cycle time	4.0 ms

1.5 Digital logic testing for device classes Q and V.

Fault coverage measurement of manufacturing logic tests (MIL-STD-883, test method 5012)	3/ percent

2. APPLICABLE DOCUMENTS

2.1 Government specification, standards, and handbooks. The following specification, standards, and handbooks form a part of this drawing to the extent specified herein. Unless otherwise specified, the issues of these documents are those listed in the issue of the Department of Defense Index of Specifications and Standards (DoDISS) and supplement thereto, cited in the solicitation.

SPECIFICATION

DEPARTMENT OF DEFENSE

MIL-PRF-38535 - Integrated Circuits, Manufacturing, General Specification for.

STANDARDS

DEPARTMENT OF DEFENSE

MIL-STD-883 - Test Method Standard Microcircuits.
MIL-STD-973 - Configuration Management.
MIL-STD-1835 - Interface Standard for Microcircuit Case Outlines.

HANDBOOKS

DEPARTMENT OF DEFENSE

MIL-HDBK-103 - List of Standard Microcircuit Drawings (SMD's).
MIL-HDBK-780 - Standard Microcircuit Drawings

(Copies of the specification, standards, bulletin, and handbook required by manufacturers in connection with specific acquisition functions should be obtained from the contracting activity or as directed by the contracting activity.)

2/ Stresses above the absolute maximum rating may cause permanent damage to the device. Extended operation at the maximum levels may degrade performance and affect reliability.
3/ Values will be added when they become available.

2.2 Non-Government publications. The following document(s) form a part of this document to the extent specified herein. Unless otherwise specified, the issues of the documents which are DoD adopted are those listed in the issue of the DODISS cited in the solicitation. Unless otherwise specified, the issues of documents not listed in the DODISS are the issues of the documents cited in the solicitation.

AMERICAN SOCIETY FOR TESTING AND MATERIALS (ASTM)

ASTM Standard F1192M-95 - Standard Guide for the Measurement of Single Event Phenomena from Heavy Ion Irradiation of Semiconductor Devices.

(Applications for copies of ASTM publications should be addressed to the American Society for Testing and Materials, 1916 Race Street, Philadelphia, PA 19103).

ELECTRONICS INDUSTRIES ASSOCIATION (EIA)

JEDEC Standard No. 17 - A Standardized Test Procedure for the Characterization of Latch-up in CMOS Integrated Circuits.

(Applications for copies should be addressed to the Electronics Industries Association, 2500 Wilson Boulevard, Arlington, VA 22201.)

(Non-Government standards and other publications are normally available from the organizations that prepare or distribute the documents. These documents also may be available in or through libraries or other informational services.)

2.3 Order of precedence. In the event of a conflict between the text of this drawing and the references cited herein, the text of this drawing shall take precedence. Nothing in this document, however, supersedes applicable laws and regulations unless a specific exemption has been obtained.

3. REQUIREMENTS

3.1 Item requirements. The individual item requirements for device classes Q and V shall be in accordance with MIL-PRF-38535 and as specified herein or as modified in the device manufacturer's Quality Management (QM) plan. The modification in the QM plan shall not affect the form, fit, or function as described herein. The individual item requirements for device class M shall be in accordance with MIL-PRF-38535, appendix A for non-JAN class level B devices and as specified herein.

3.2 Design, construction, and physical dimensions. The design, construction, and physical dimensions shall be as specified in MIL-PRF-38535 and herein for device classes Q and V or MIL-PRF-38535, appendix A and herein for device class M.

3.2.1 Case outline(s). The case outline(s) shall be in accordance with 1.2.4 herein and figure 1.

3.2.2 Terminal connections. The terminal connections shall be as specified on figure 2.

3.2.3 Truth table(s). The truth table(s) shall be as specified on figure 3.

3.2.5 Functional tests. Various functional tests used to test this device are contained in the appendix. If the test patterns cannot be implemented due to test equipment limitations, alternate test patterns to accomplish the same results shall be allowed. For device class M, alternate test patterns shall be maintained under document revision level control by the manufacturer and shall be made available to the preparing or acquiring activity upon request. For device classes Q and V alternate test patterns shall be under the control of the device manufacturer's Technology Review Board (TRB) in accordance with MIL-PRF-38535 and shall be made available to the preparing or acquiring activity upon request.

3.3 Electrical performance characteristics and postirradiation parameter limits. Unless otherwise specified herein, the electrical performance characteristics and postirradiation parameter limits are as specified in table I and shall apply over the full case operating temperature range.

3.4 Electrical test requirements. The electrical test requirements shall be the subgroups specified in table IIA. The electrical tests for each subgroup are defined in table I.

3.5 Marking. The part shall be marked with the PIN listed in 1.2 herein. In addition, the manufacturer's PIN may also be marked as listed in MIL-HDBK-103. For packages where marking of the entire SMD PIN number is not feasible due to space limitations, the manufacturer has the option of not marking the "5962-" on the device. For RHA product using this option, the RHA designator shall still be marked. Marking for device classes Q and V shall be in accordance with MIL-PRF-38535. Marking for device class M shall be in accordance with MIL-PRF-38535, appendix A.

3.5.1 Certification/compliance mark. The certification mark for device classes Q and V shall be a "QML" or "Q" as required in MIL-PRF-38535. The compliance mark for device class M shall be a "C" as required in MIL-PRF-38535, appendix A.

3.6 Certificate of compliance. For device classes Q and V, a certificate of compliance shall be required from a QML-38535 listed manufacturer in order to supply to the requirements of this drawing (see 6.6.1 herein). For device class M, a certificate of compliance shall be required from a manufacturer in order to be listed as an approved source of supply in MIL-HDBK-103 (see 6.6.2 herein). The certificate of compliance submitted to DSCC-VA prior to listing as an approved source of supply for this drawing shall affirm that the manufacturer's product meets, for device classes Q and V, the requirements of MIL-PRF-38535 and herein or for device class M, the requirements of MIL-PRF-38535, appendix A and herein.

3.7 Certificate of conformance. A certificate of conformance as required for device classes Q and V in MIL-PRF-38535 or for device class M in MIL-PRF-38535, appendix A shall be provided with each lot of microcircuits delivered to this drawing.

3.8 Notification of change for device class M. For device class M, notification to DSCC-VA of change of product (see 6.2 herein) involving devices acquired to this drawing is required for any change as defined in MIL-STD-973.

3.9 Verification and review for device class M. For device class M, DSCC, DSCC's agent, and the acquiring activity retain the option to review the manufacturer's facility and applicable required documentation. Offshore documentation shall be made available onshore at the option of the reviewer.

3.10 Microcircuit group assignment for device class M. Device class M devices covered by this drawing shall be in microcircuit group number 41 (see MIL-PRF-38535, appendix A).

4. QUALITY ASSURANCE PROVISIONS

4.1 Sampling and inspection. For device classes Q and V, sampling and inspection procedures shall be in accordance with MIL-PRF-38535 or as modified in the device manufacturer's Quality Management (QM) plan. The modification in the QM plan shall not affect the form, fit, or function as described herein. For device class M, sampling and inspection procedures shall be in accordance with MIL-PRF-38535, appendix A.

4.2 Screening. For device classes Q and V, screening shall be in accordance with MIL-PRF-38535, and shall be conducted on all devices prior to qualification and technology conformance inspection. For device class M, screening shall be in accordance with method 5004 of MIL-STD-883, and shall be conducted on all devices prior to quality conformance inspection.

4.2.1 Additional criteria for device class M.

a. Delete the sequence specified as initial (preburn-in) electrical parameters through interim (postburn-in) electrical parameters of method 5004 and substitute lines 1 through 6 of table IIA herein.

b. The test circuit shall be maintained by the manufacturer under document revision level control and shall be made available to the preparing or acquiring activity upon request. The test circuit shall specify the inputs, outputs, biases, and power dissipation, as applicable, in accordance with the intent specified in test method 1015.

(1) Dynamic burn-in (method 1015 of MIL-STD-883, test condition D; for circuit, see 4.2.1b herein).

c. Interim and final electrical parameters shall be as specified in table IIA herein.

TABLE I. Electrical performance characteristics.

Test	Symbol	Conditions 1/ 2/ 3/ 4/ $-55°C \le T_C \le +125°C$ $4.5\ V \le V_{CC} \le 5.5\ V$ unless otherwise specified	Group A subgroups	Device type	Limits		Unit
					Min	Max	
High level output voltage 5/	V_{OH}	$V_{IL} = 0.8\ V$, $I_{OH} = -5\ mA$, $V_{IH} = 2.4\ V$	1,2,3	All	2.4		V
Low level output voltage 5/	V_{OL}	$V_{IL} = 0.8\ V$, $I_{OL} = 5\ mA$, $V_{IH} = 2.4\ V$	1,2,3	All		0.4	
High level input leakage current	I_{IH}	$V_{CC} = 5.5\ V$, $V_I = 6.5\ V$	1,2,3	All		10	µA
Low level input leakage current	I_{IL}	$V_{CC} = 5.5\ V$, $V_I = 0.0\ V$	1,2,3	All		-10	
High level output leakage current	I_{OH}	$V_{CC} = 5.5\ V$, $V_O = 6.5\ V$	1,2,3	All		10	
Low level output leakage current	I_{OL}	$V_{CC} = 5.5\ V$, $V_O = 0.0\ V$	1,2,3	All		-10	
Average operating current during READ 6/ or WRITE cycle	I_{CC1}	T_C = minimum cycle	1,2,3	01-03 04-06		60 70	mA
Average page-mode current 6/	I_{CC2}	$\overline{RAS}$ low, $\overline{CAS}$ cycling, $T_C(P)$ = minimum cycle	1,2,3	01-03 04-06		55 65	
Standby current	I_{CC3}	after 1 memory cycle RAS and CAS high	1,2,3	All		8	
Average refresh current (RAS only 6/ REFRESH)	I_{CC4}	T_C = minimim cycle, CAS high, RAS cycling	1,2,3	01-03 04-06		60 70	
Standby current ($\overline{CAS}$ before RAS refresh) 7/	I_{CC5}	T_C = minimum cycle, $\overline{RAS}$ and $\overline{CAS}$ cycling	1,2,3	01-03 04-06		60 70	
Input capacitance A_O - A_7, D_{IN} 7/	C_{I1}	$T_C = +25°C$, f = 1 MHz See 4.4.1e	4	All		6	pF
Input capacitance $\overline{RAS}$, $\overline{CAS}$, WE, OE 7/	C_{I2}	$T_C = +25°C$, f = 1 MHz See 4.4.1e	4	All		8	

See footnotes at end of table.

TABLE I. Electrical performance characteristics.

Test	Symbol	Conditions 1/ 2/ 3/ 4/ $-55°C \le T_C \le +125°C$, $4.5\ V \le V_{CC} \le 5.5\ V$ unless otherwise specified	Group A subgroups	Device type	Limits		Unit
					Min	Max	
Output capacitance D_{OUT} 7/	C_O	T_C = +25°C, f = 1 MHz See 4.4.1e	4	All		8	pF
Functional test		See 4.4.1c	7,8A,8B	All			
Access time from $\overline{RAS}$ 8/	$t_{a(R)}$	See figures 4 and 5	9,10,11	01,04		100	ns
				02,05		120	
				03,06		150	
Access time from $\overline{CAS}$ 9/	$t_{a(C)}$		9,10,11	01,04		50	
				02,05		60	
				03,06		75	
Output disable time after CAS high 10/	$t_{dis(CH)}$		9,10,11	All		40	
Page-mode cycle time 11/	$t_{c(P)}$		9,10,11	01,04	90		
				02,05	100		
				03,06	120		
Read cycle time	$t_{c(rd)}$		9,10,11	01,04	195		
				02,05	220		
				03,06	250		
Write cycle time	$t_{c(W)}$		9,10,11	01,04	195		
				02,05	220		
				03,06	250		
Read-write/read-modify-write cycle time 11/	$t_{c(rdW)}$		9,10,11	01,04	250		
				02,05	290		
				03,06	315		
Pulse duration, $\overline{CAS}$ high (page mode)	$t_{w(CH)P}$		9,10,11	01,02, 04,05	30		
				03,06	35		
Pulse duration, $\overline{CAS}$ low	$t_{w(CL)}$		9,10,11	01,04	50	10000	
				02,05	60	10000	
				03,06	75	10000	
Pulse duration, $\overline{RAS}$ high (precharge time) 12/ (page mode)	$t_{w(RH)P}$		9,10,11	01,02, 04,05	80		
				03,06	90		
Pulse duration, $\overline{RAS}$ high (precharge time) (non-page mode)	$t_{w(RH)}$		9,10,11	01,02, 04,05	80		
				03,06	90		
Pulse duration, $\overline{RAS}$ low	$t_{w(RL)}$		9,10,11	01,04	100	10000	
				02,05	120	10000	
				03,06	150	10000	

See footnotes at end of table.

TABLE I. Electrical performance characteristics.

Test	Symbol	Conditions 1/ 2/ 3/ 4/ $-55°C \le T_C \le +125°C$ $4.5\ V \le V_{CC} \le 5.5\ V$ unless otherwise specified	Group A subgroups	Device type	Limits		Unit
					Min	Max	
Write pulse duration	$t_{w(W)}$	See figures 4 and 5	9,10,11	01,04	35		ns
				02,05	40		
				03,06	45		
Column address setup time 11/	$t_{su(CA)}$		9,10,11	All	0		
Row address setup time 11/	$t_{su(RA)}$		9,10,11	All	0		
Data setup time 11/ 13/	$t_{su(D)}$		9,10,11	All	0		
Read command setup time 11/	$t_{su(rd)}$		9,10,11	All	0		
Early write command setup time before CAS low 14/	tsu(WCL)		9,10,11	All	0		
Write command setup time before CAS high	$t_{su(WCH)}$		9,10,11	01,04	35		
				02,05	40		
				03,06	45		
Write command setup time before RAS high	$t_{su(WRH)}$		9,10,11	01,04	35		
				02,05	40		
				03,06	45		
Setup time, $\overline{WE}$ high before RAS low (CAS before RAS refresh) 9/	$t_{su(WRP)}$		9,10,11	04-06	10		
Hold time, $\overline{WE}$ high from RAS low (CAS before RAS refresh) 9/	$t_{h(WRH)}$		9,10,11	04-06	10		
Column address hold time after CAS low	$t_{h(CLCA)}$		9,10,11	01,04	20		
				02,03, 05,06	30		
Row address hold time	$t_{h(RA)}$		9,10,11	01,04	15		
				02,03, 05,06	20		
Column address hold time after RAS low	$t_{h(RLCA)}$ $t_{su(RLCA)}$		9,10,11	01,04	70		
				02,05	80		
				03,06	100		

See footnotes at end of table.

TABLE I. Electrical performance characteristics.

Test	Symbol	Conditions 1/ 2/ 3/ 4/ $-55°C \le T_C \le +125°C$ $4.5\ V \le V_{CC} \le 5.5\ V$ unless otherwise specified	Group A subgroups	Device type	Limits		Unit
					Min	Max	
Data hold time after $\overline{CAS}$ low 13/	$t_{h(CLD)}$	See figures 4 and 5	9,10,11	01,02, 04,05	35		ns
				03,06	45		
Data hold time after $\overline{RAS}$ low	$t_{h(RLD)}$		9,10,11	01,04	85		
				02,05	100		
				03,06	120		
$\overline{RAS}$ before $\overline{CAS}$ precharge 11/	t_{RHCL}		9,10,11	All	0		
Data hold time after $\overline{WE}$ low 13/	$t_{h(WLD)}$		9,10,11	01,02, 04,05	35		
				03,06	45		
Read command hold time after $\overline{CAS}$ high 11/	$t_{h(CHrd)}$		9,10,11	All	0		
Read command hold time after $\overline{RAS}$ high	$t_{h(RHrd)}$		9,10,11	All	10		
Write command hold time after $\overline{CAS}$ low	$t_{h(CLW)}$		9,10,11	01,04	35		
				02,05	40		
				03,06	45		
Write command hold time after $\overline{RAS}$ low	$t_{h(RLW)}$		9,10,11	01,04	85		
				02,05	100		
				03,06	120		
Delay time, $\overline{RAS}$ low to $\overline{CAS}$ high	t_{RLCH}		9,10,11	01,04	110		
				02,05	120		
				03,06	150		
Delay time, $\overline{CAS}$ high to $\overline{RAS}$ low	t_{CHRL}		9,10,11	All	5		
Delay time, $\overline{CAS}$ low to $\overline{RAS}$ high	t_{CLRH}		9,10,11	01,04	50		
				02,05	60		
				03,06	75		
Delay time, $\overline{RAS}$ low to $\overline{CAS}$ high ($\overline{CAS}$ before $\overline{RAS}$ refresh only)	t_{RLCHR}		9,10,11	01,04	20		
				02,05	25		
				03,06	30		
Delay time, $\overline{CAS}$ low to $\overline{RAS}$ low ($\overline{CAS}$ before $\overline{RAS}$ refresh only) 15/	t_{CLRL}		9,10,11	All	10		

See footnotes at end of table.

TABLE I. Electrical performance characteristics.

Test	Symbol	Conditions 1/ 2/ 3/ 4/ $-55°C \le T_C \le +125°C$, $4.5\ V \le V_{CC} \le 5.5\ V$ unless otherwise specified	Group A subgroups	Device type	Limits		Unit
					Min	Max	
Delay time, $\overline{CAS}$ low to $\overline{WE}$ low (read-modify-write cycle only) 14/ 16/	t_{CLWL}	See figures 4 and 5	9,10,11	01,04	30		ns
				02,05	50		
				03,06	60		
Delay time, $\overline{RAS}$ low to $\overline{CAS}$ low	t_{RLCL}		9,10,11	01,04	25	50	
				02,05	30	60	
				03,06	30	75	
Delay time, $\overline{RAS}$ low to $\overline{WE}$ low (read-modify-write cycle only) 14/ 16/	t_{RLWL}		9,10,11	01,04	80		
				02,05	110		
				03,06	135		
Refresh time interval 17/ 18/	t_{rf}		9,10,11	All		4.0	ms
Transition time (rise and fall)	t_t		9,10,11	1,2,3	3	100	ns
				4,5,6		50	
Output disable time after $\overline{OE}$ high	$t_{dis(GH)}$		9,10,11	01,04		35	
				02,03, 05,06		40	
Output enable time after $\overline{OE}$ low 19/	$t_{en(GL)}$		9,10,11	01,02, 04,05		25	
				03,06		30	

1/ An initial pause of 100 µs is required after power-up followed by any 8 RAS $\overline{ONLY}$ REFRESH or CBR REFRESH cycles only before proper device operation is assured.
2/ AC characteristics assume transition time (t_T) = 5 ns. Input levels are from GND to 3.0 V. Input and output timing reference levels are 1.5 V.
3/ V_{IL} (max) and V_{IH} (min) are reference levels for measuring timing of input signals. Transition times are measured between V_{IL} and V_{IH}.
4/ In addition to meeting the transition rate specification, all input signals must make the transition between V_{IL} and V_{IH} (or V_{IH} and V_{IL}) in a monotonic manner.
5/ V_{SS} is common for all voltages.
6/ Specified values are obtained with the output load equal to 2 TTL loads and 100 pF to V_{SS}.
7/ Capacitance measured with a Boonton meter or equivalent or effective capacitance calculated from the equation $C=I\Delta t/\Delta V$ with ΔV equal to 3 volts and V_{CC} equal to 5.0 V. Capacitance shall be measured only for the initial qualification and after process or design changes which may effect terminal capacitance.
8/ Assumes that $t_{RLCL} <$ (max). If t_{RCD} is greater than the maximum recommended value shown in this table, $t_{a(R)}$ will increase by the amount that t_{RLCL} exceeds the value shown.
9/ Assumes that $t_{RLCL} \ge t_{RLCL}$ (max).
10/ $t_{dis(CH)}$ (max) defines the time at which the output achieves the open circuit condition and is not referenced to V_{OH} or V_{OL}.
11/ Some parameters are conditionally guaranteed that are specified to aid device application. They are not necessarily directly verified by a specific test, however, the vendor uses device characterizations and design specifications to insure all device parameters are within specified performance limits.
12/ If CAS is low at the falling edge of RAS, D_{OUT} will be maintained from the previous cycle. To initiate a new cycle and clear the data out buffer CAS must be pulsed high for $t_{c(P)}$. Footnote 20/ applies to determine valid data out.

TABLE I. Electrical performance characteristics - continued.

13/ These parameters are referenced to $\overline{CAS}$ leading edge in early WRITE cycles and to $\overline{WE}$ leading edge in late WRITE or READ-MODIFY-WRITE cycles.

14/ $t_{su(WCL)}$, t_{CLWL} and t_{RLWL} are restrictive operating parameters in READ-WRITE and READ-MODIFY-WRITE cycles only. If $t_{su(WCL)} \geq t_{su(WCL)}$ (min) the cycle is an EARLY WRITE cycle and the data output will remain open circuit throughout the entire cycle. If $t_{CLWL} \geq t_{CLWL}$ (min) and $t_{RLWL} \geq t_{RLWL}$ (min) the cycle is a READ-WRITE and the data output will contain data read from the selected cell. If neither of the above conditions are met the conditions of the data out (at access time and until CAS goes back to V_{IH}) is indeterminate.

15/ Enables on-chip refresh and address counters.

16/ During a READ-WRITE or READ-MODIFY-WRITE cycle the minimum specifications for t_{RWD} and t_{CWD} must be modified by adding 40 ns to each specification due to $\overline{OE}$ delay.

17/ A 256-cycle distributed refresh consists of an address location refresh cycle being performed within 15.625 µs so that all 256 $\overline{RAS}$ address combinations are executed within 4 ms (regardless of sequence). Distributed refresh is recommended.

18/ A 256-cycle burst refresh consists of refreshing, as rapidly as minimum cycle time allows, all 256 combinations of $\overline{RAS}$ addresses (regardless of sequence). This refresh mode must be executed within 4 ms.

19/ If OE is taken low then high (V_{IH}) D_{OUT} goes open. If OE is tied permanently low a READ-WRITE or READ-MODIFY-WRITE operation requires a separate READ and WRITE cycle.

20/ If $\overline{CAS} = V_{IH}$ or $\overline{OE} = V_{IH}$ data output is high impedance. If $\overline{CAS} = V_{IL}$ and $\overline{OE} = V_{IL}$ data output may contain data from the last valid READ cycle.

Case X

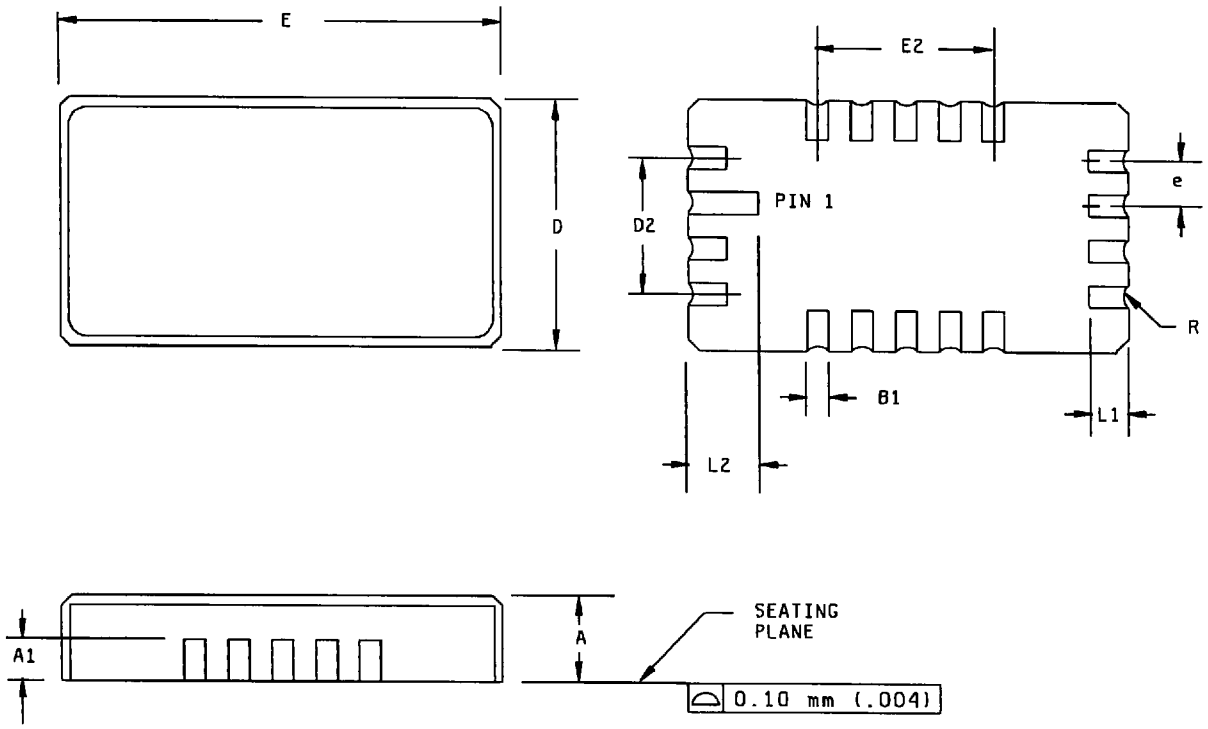


FIGURE 1. Case outline.

STANDARD MICROCIRCUIT DRAWING DEFENSE SUPPLY CENTER COLUMBUS COLUMBUS, OHIO 42316-5000	SIZE **A**		**5962-92132**
		REVISION LEVEL B	SHEET **12**

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Symbol	Dimensions shown in			
	Millimeters		Inches	
	Min	Max	Min	Max
A	1.40	1.91	.055	.075
A_1	0.89	1.14	.035	.045
B_1	0.56	0.71	.022	.028
D	7.11	7.49	.280	.295
D_2	3.81 REF		.150 REF	
E	12.32	12.83	.485	.505
E_2	5.08 REF		.200 REF	
e	1.27 BSC		.050 BSC	
L_1	1.14	1.40	.045	.055
L_2	1.91	2.31	.075	.091
N	18		18	
R	0.10 R	0.36 R	.004 R	.014 R
ND	4		4	
NE	5		5	

Note: The U.S. government preferred system of measurement is the metric SI system. However, this item was originally designed using inch-pound units of measurement. In the event of conflict between the metric and inch-pound units, the inch-pound units shall take precedence.

FIGURE 1. Case outline - Continued.

Case Y

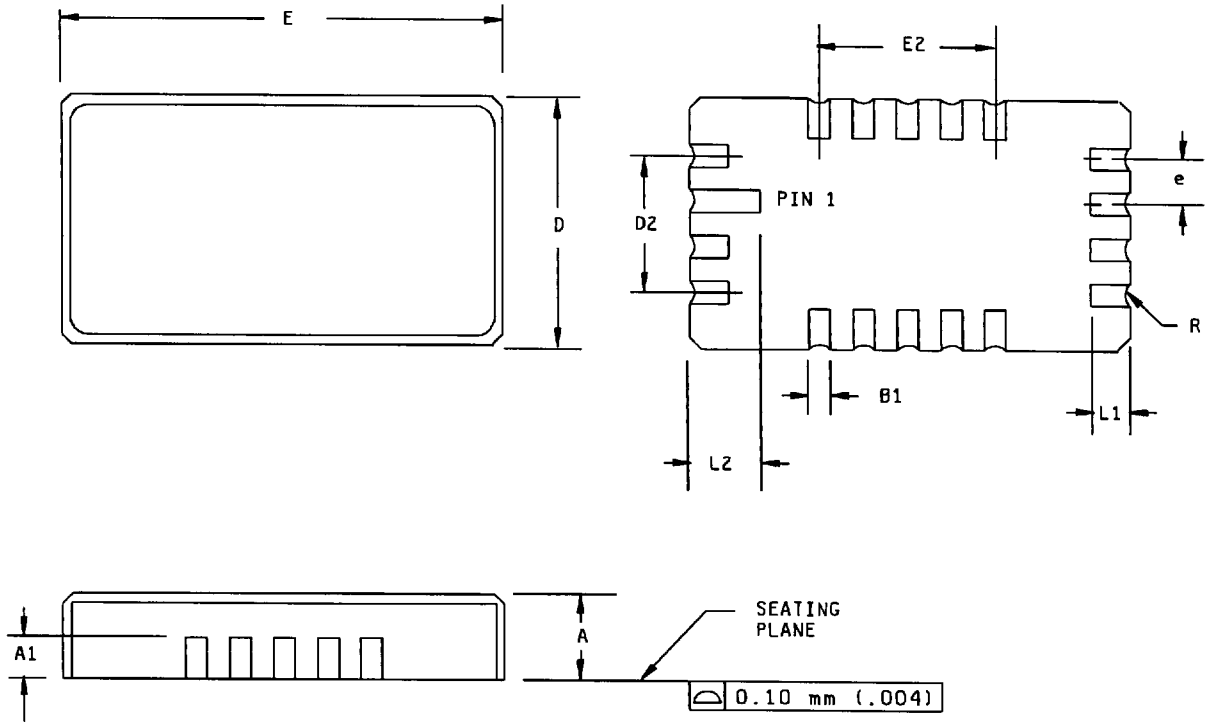

FIGURE 1. Case outline.

STANDARD MICROCIRCUIT DRAWING DEFENSE SUPPLY CENTER COLUMBUS COLUMBUS, OHIO 42316-5000	SIZE **A**		**5962-92132**
		REVISION LEVEL B	SHEET **14**

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APR 97

9004708 0039975 565

Symbol	Dimensions shown in			
	Millimeters		Inches	
	Min	Max	Min	Max
A	1.47	1.83	.058	.072
A_1	1.14	1.40	.045	.055
B_1	0.15	0.56	.006	.022
D	7.11	7.37	.280	.290
D_2	3.81 REF		.150 REF	
E	11.28	11.58	.444	.456
E_2	5.08 REF		.200 REF	
e	1.27 BSC		.050 BSC	
L_1	1.14	1.40	.045	.055
L_2	1.96	2.36	.077	.093
N	18		18	
R	0.10 R	0.36 R	.004 R	.014 R
ND	4		4	
NE	5		5	

Note: The U.S. government preferred system of measurement is the metric SI system. However, this item was originally designed using inch-pound units of measurement. In the event of conflict between the metric and inch-pound units, the inch-pound units shall take precedence.

FIGURE 1. Case outline - Continued.

Device types	ALL
Case outlines	V,X,Y
Terminal number	Terminal symbol
1	$\overline{OE}$
2	I/O_1
3	I/O_2
4	$\overline{WE}$
5	$\overline{RAS}$
6	A_6
7	A_5
8	A_4
9	V_{CC}
10	A_7
11	A_3
12	A_2
13	A_1
14	A_0
15	I/O_3
16	$\overline{CAS}$
17	I/O_4
18	V_{SS}

Figure 2. Terminal connections.

Operation	Inputs						Input/Output
	$\overline{RAS}$	$\overline{CAS}$	$\overline{WE}$	$\overline{OE}$	Row address	Column address	
Standby	H	H	H	H	X	X	High-Z
Read	L	L	L	X	Row	Col	Data out
Write (early write)	L	L	L	X	Row	Col	Data in
Read-write	L	L	H→L→H	L→H	Row	Col	Data out, Data in
Page-mode read	L	H→L→H	H	L	Row	Col	Data out, Data out
Page-mode write	L	H→L→H	L	X	Row	Col	Data in, Data in
Page-mode read-write	L	H→L→H	H→L→H	L→H	Row	Col	Data out, Data in
$\overline{RAS}$-only refresh	L	H	X	H	Row	N/A	High-Z
Hidden refresh	L→H→L	L	H	L	Row	Col	Data out
$\overline{CAS}$ before $\overline{RAS}$ refresh	H→L	L	H	X	X	X	High-Z

X = Don't care

FIGURE 3. Truth table.

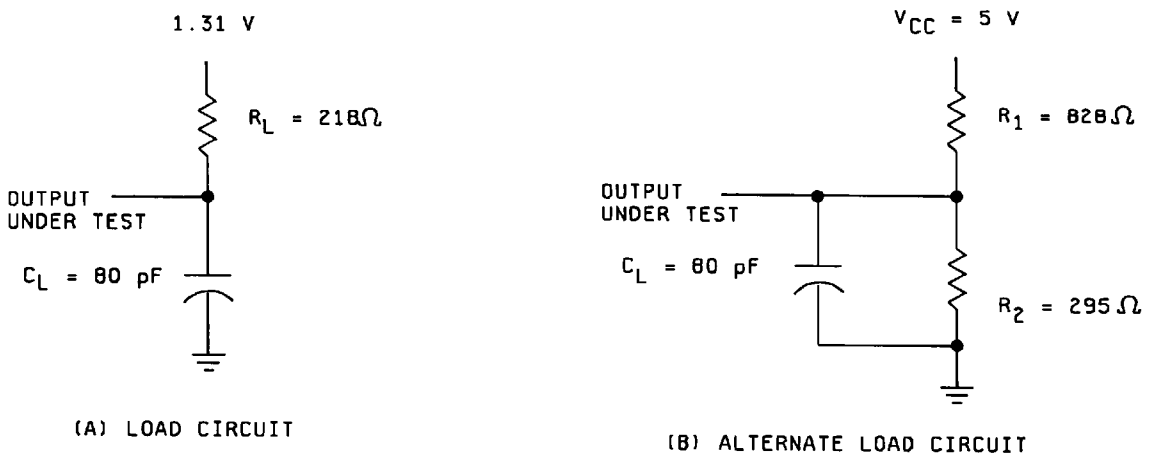

FIGURE 4. Load circuit.

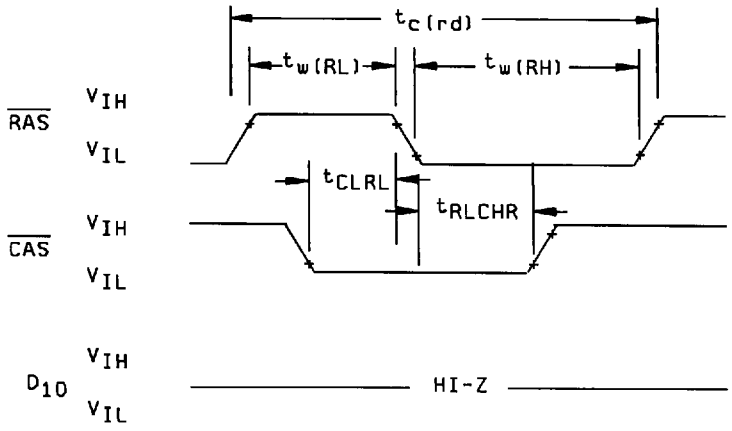

FIGURE 5. Switching waveforms.

Read cycle

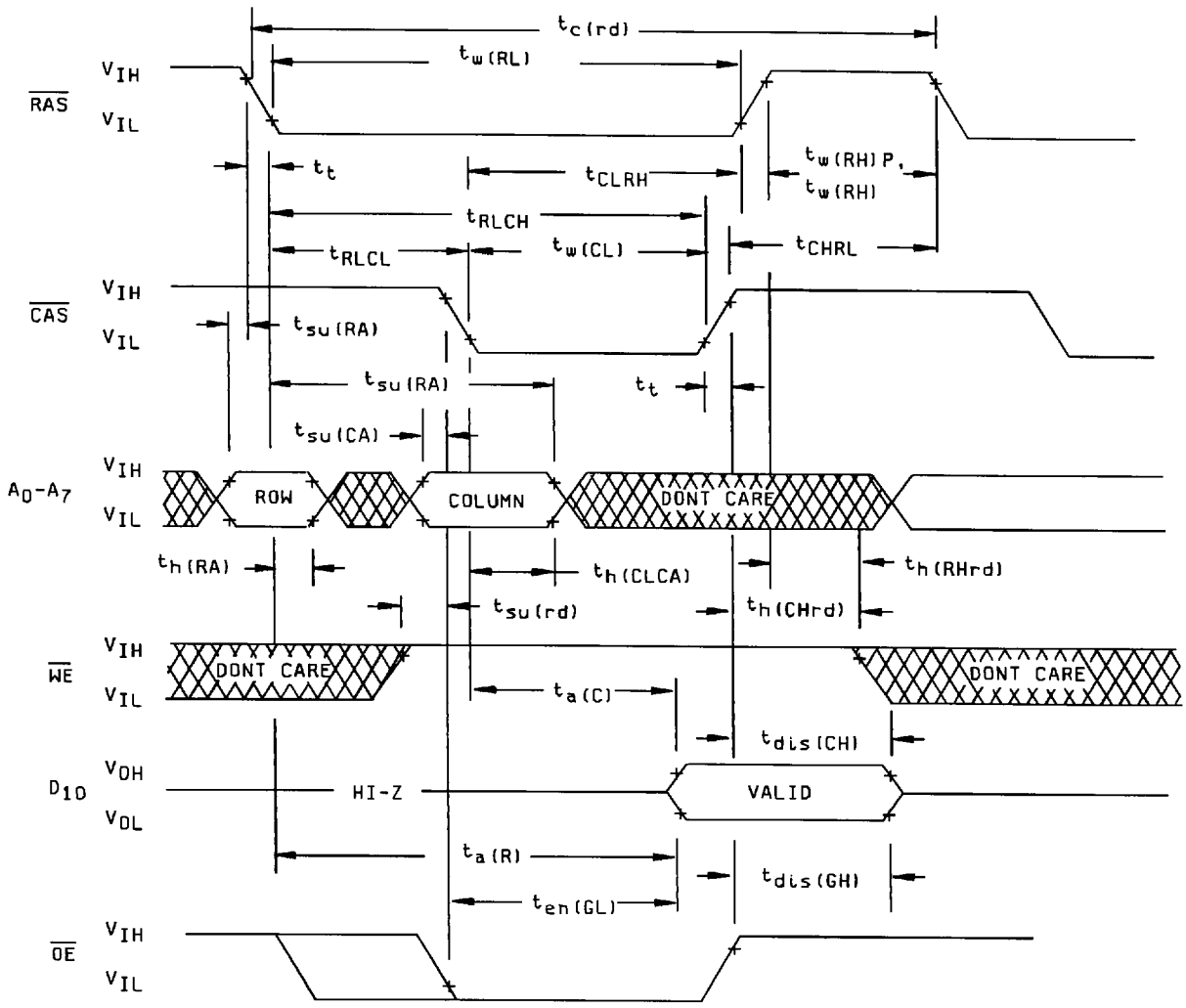

FIGURE 5. Switching waveforms - continued.

Early write cycle

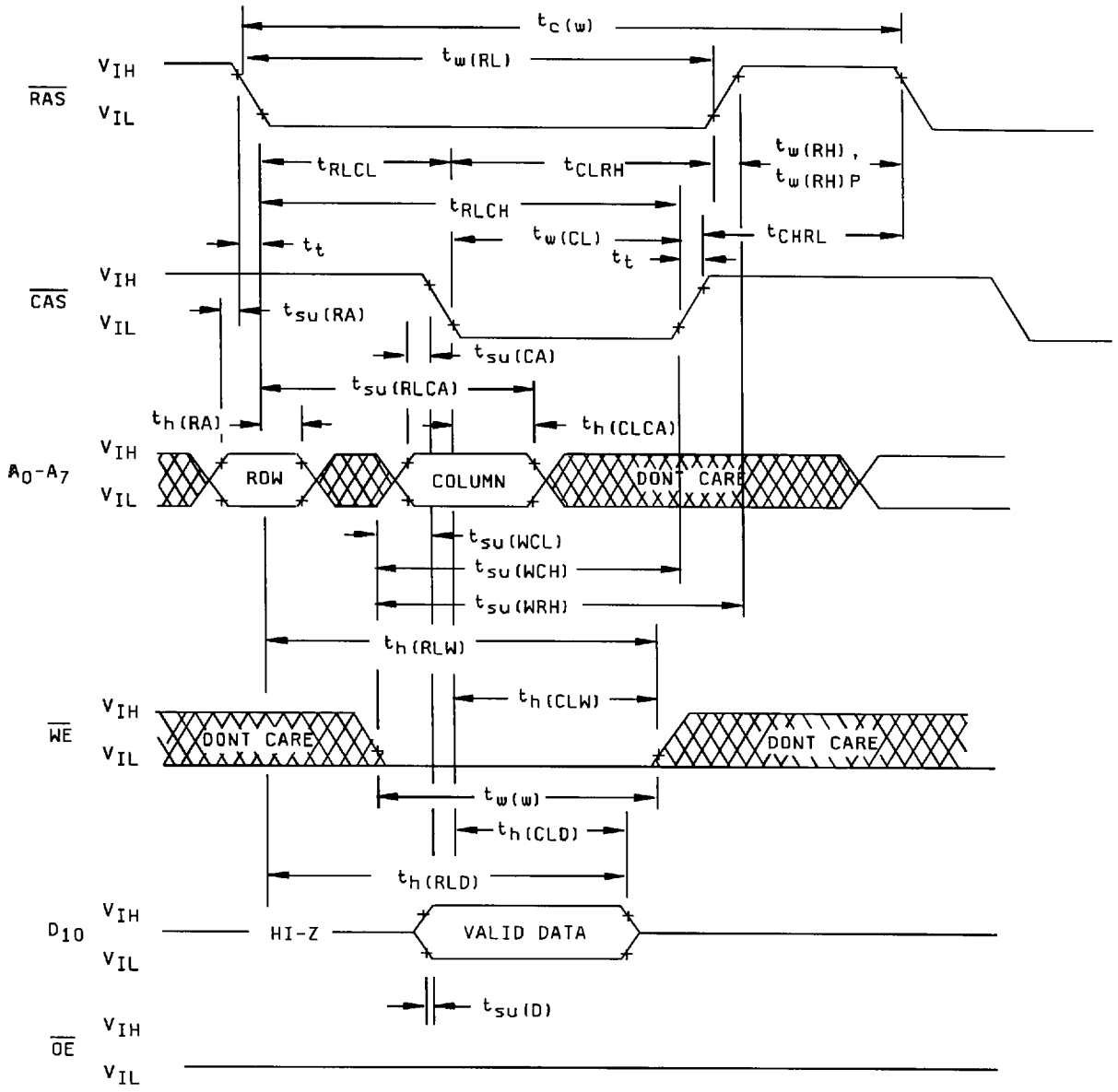

FIGURE 5. Switching waveforms - continued.

Read-write/read-modify-write cycle

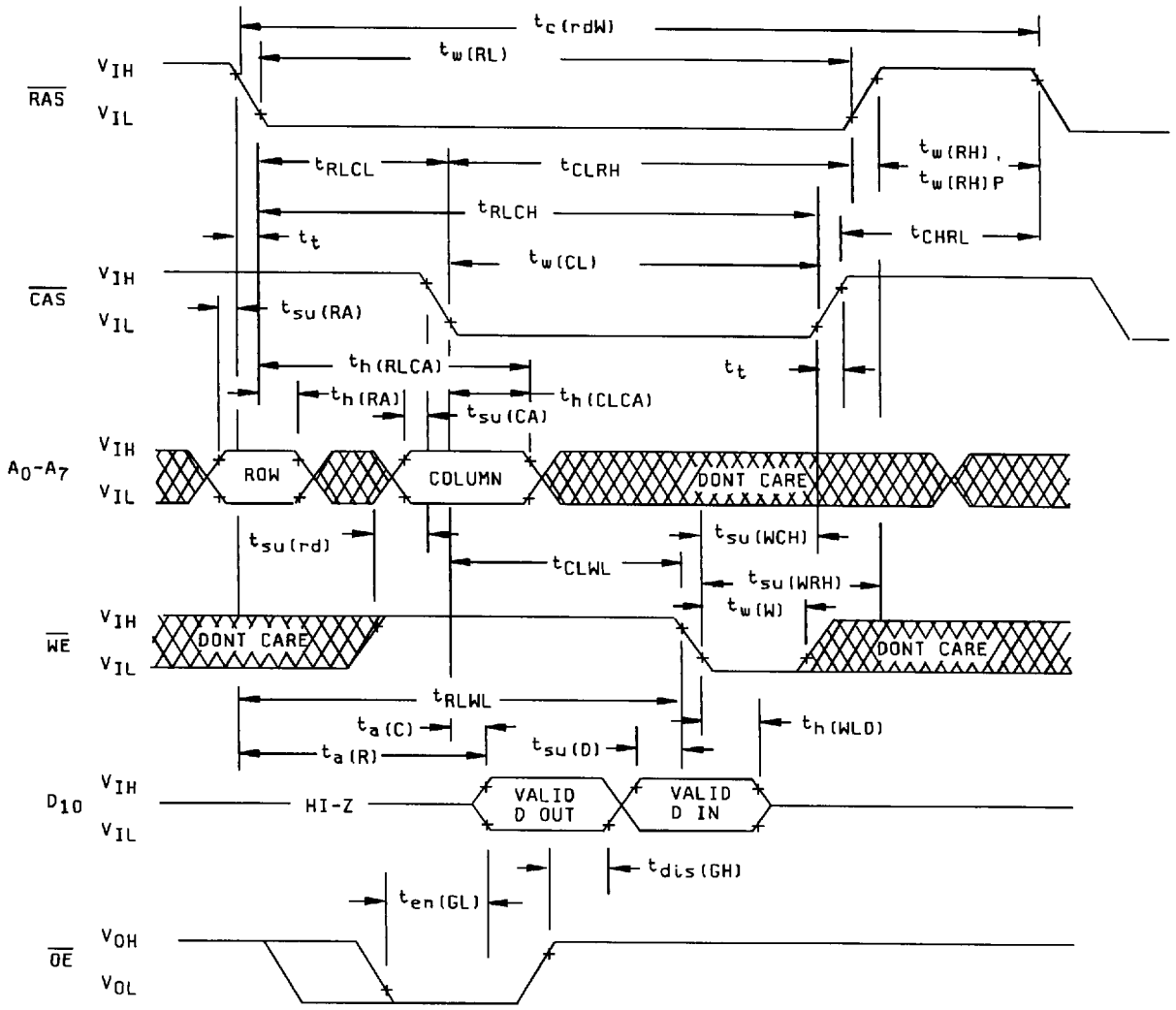

FIGURE 5. Switching waveforms - continued.

Page-mode read cycle

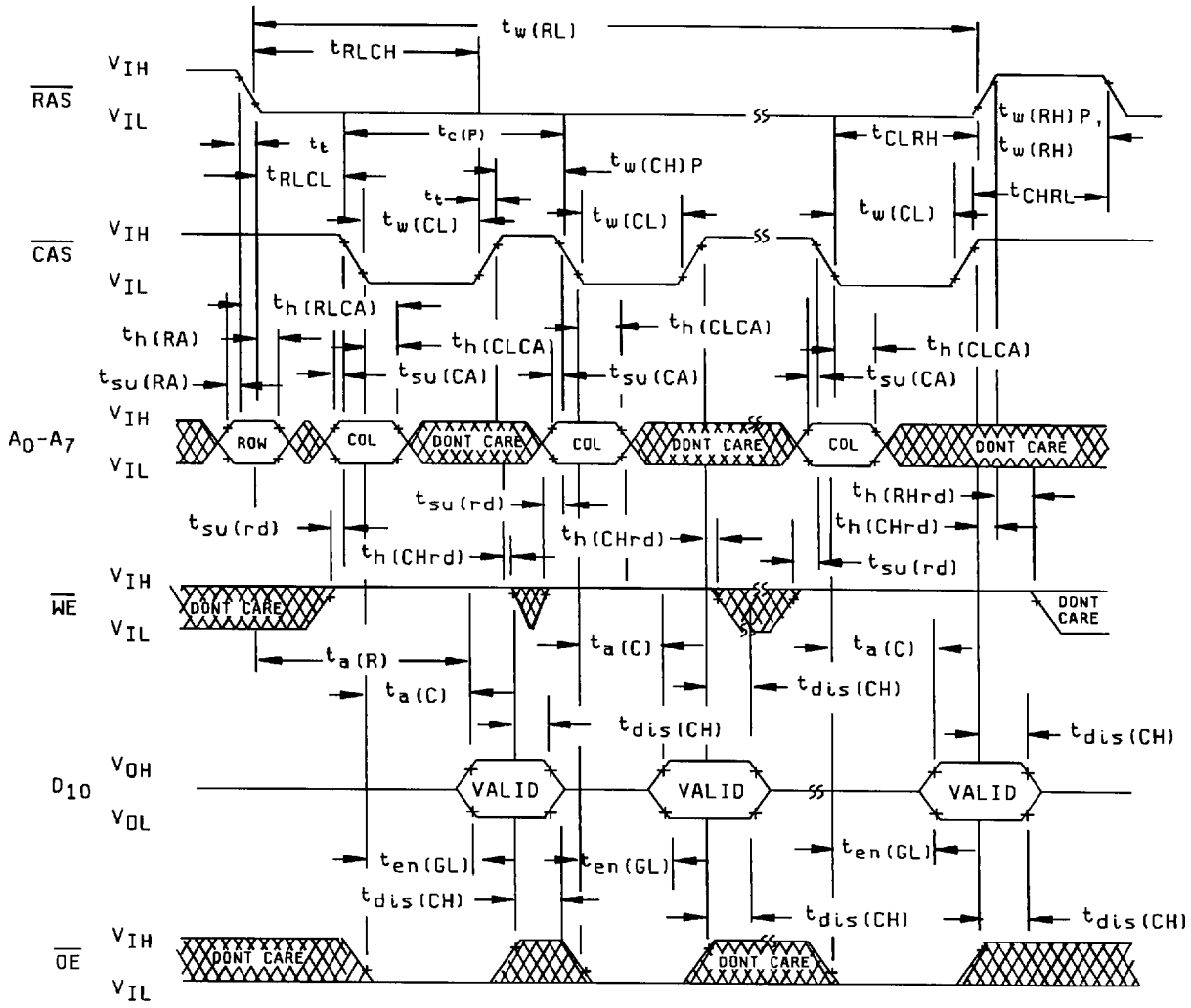

FIGURE 5. Switching waveforms - continued.

Page-mode early write cycle

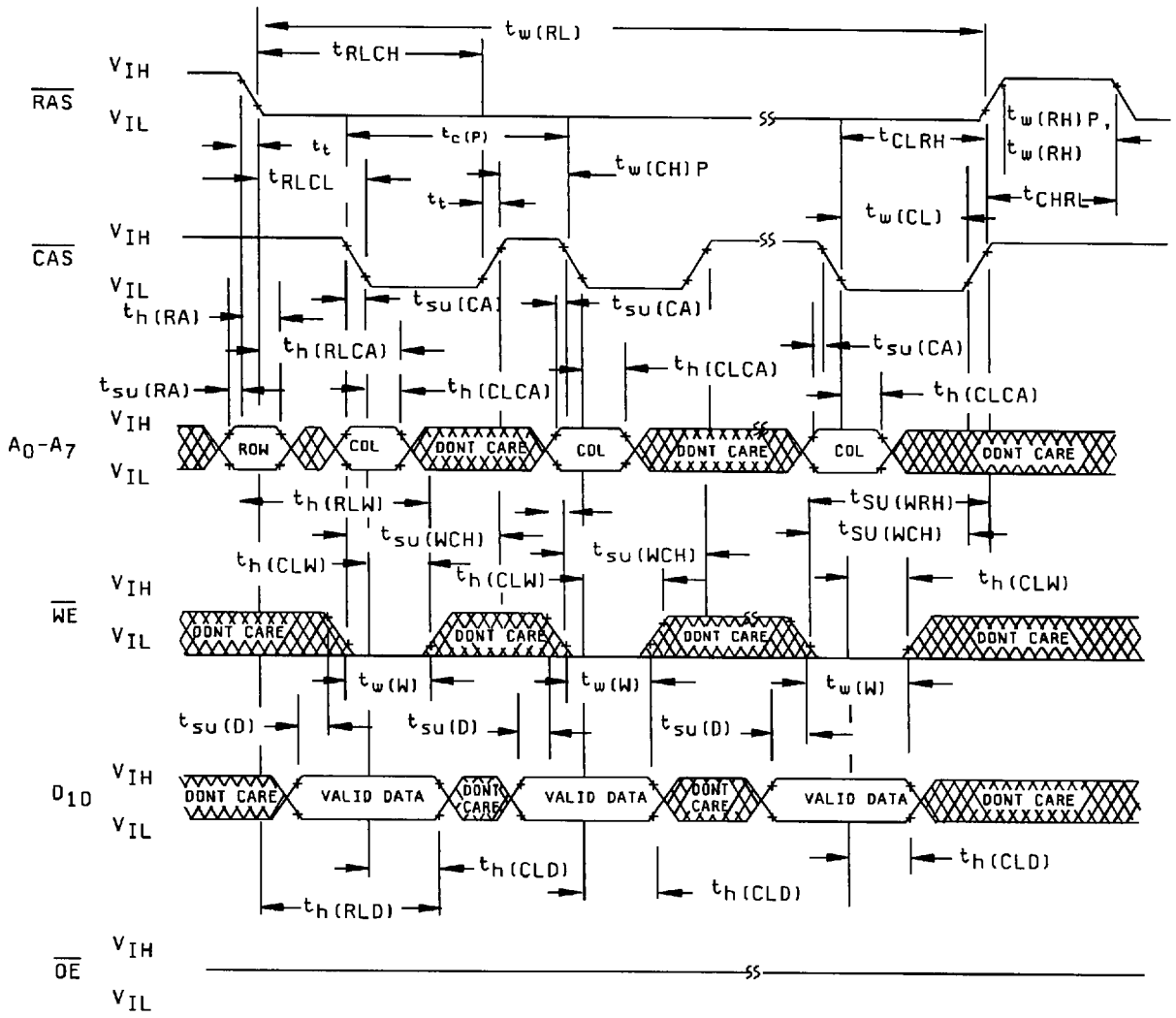

FIGURE 5. Switching waveforms - continued.

STANDARD MICROCIRCUIT DRAWING DEFENSE SUPPLY CENTER COLUMBUS COLUMBUS, OHIO 42316-5000	SIZE A		5962-92132
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Page-mode read-modify-write cycle

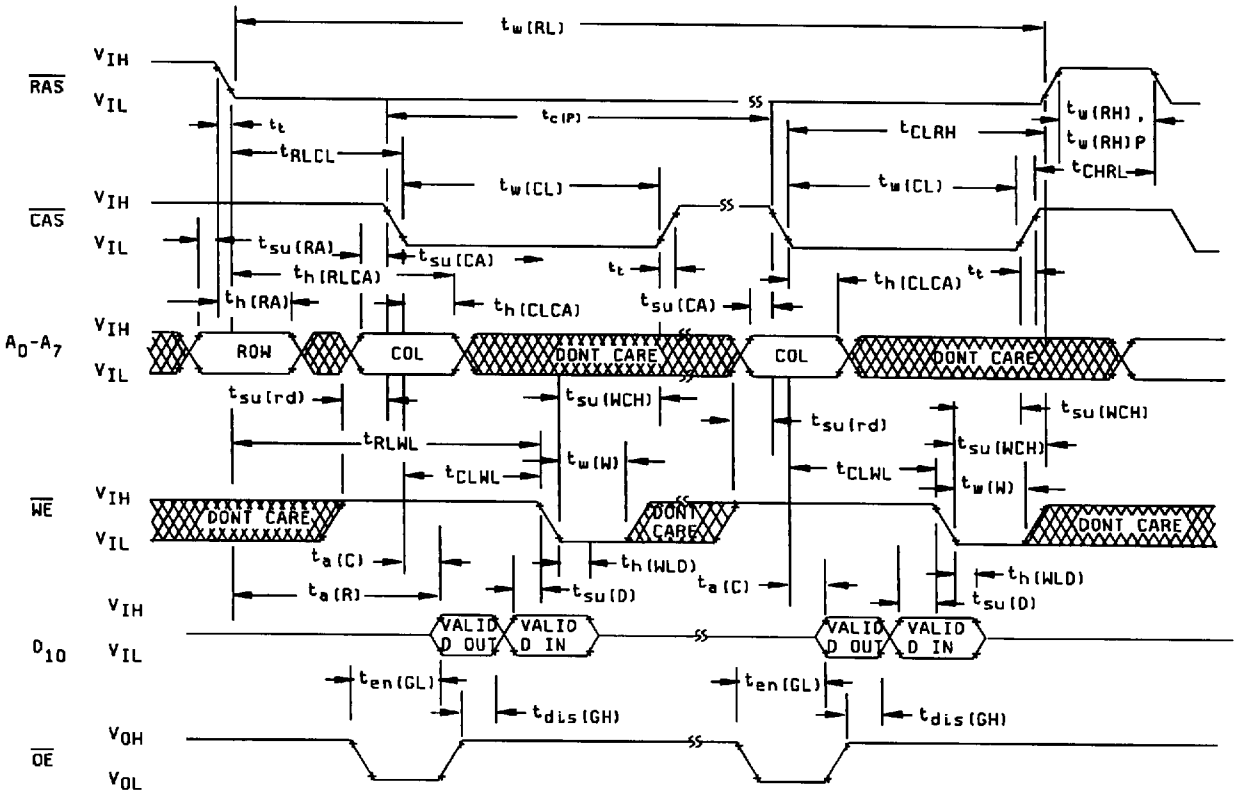


FIGURE 5. Switching waveforms - continued.

$\overline{RAS}$-only refresh cycle

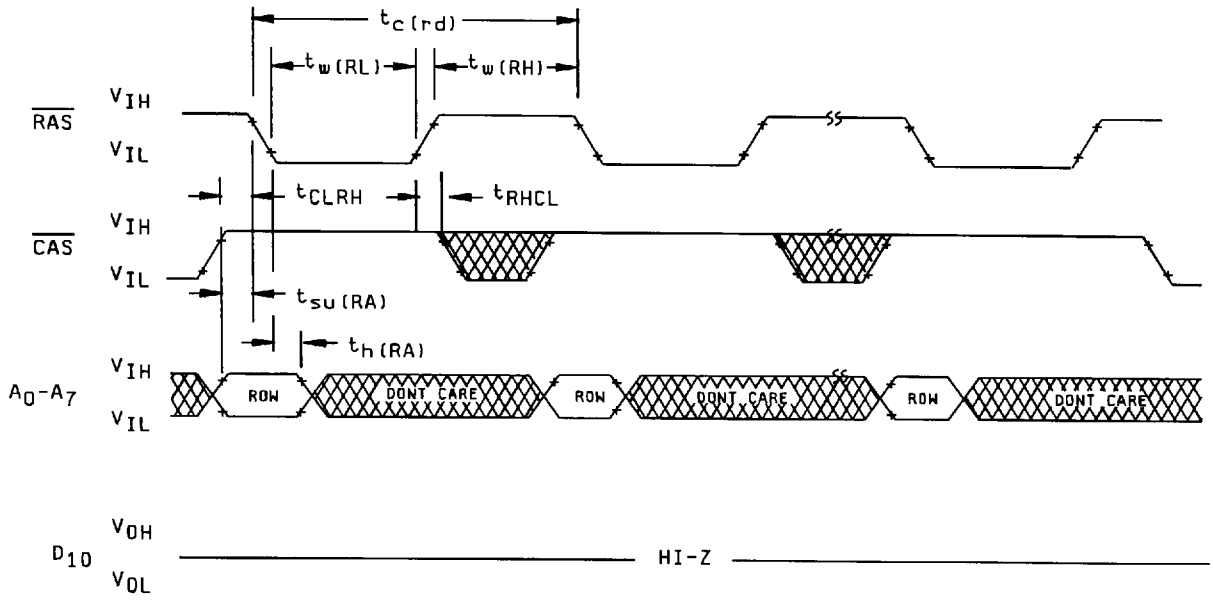
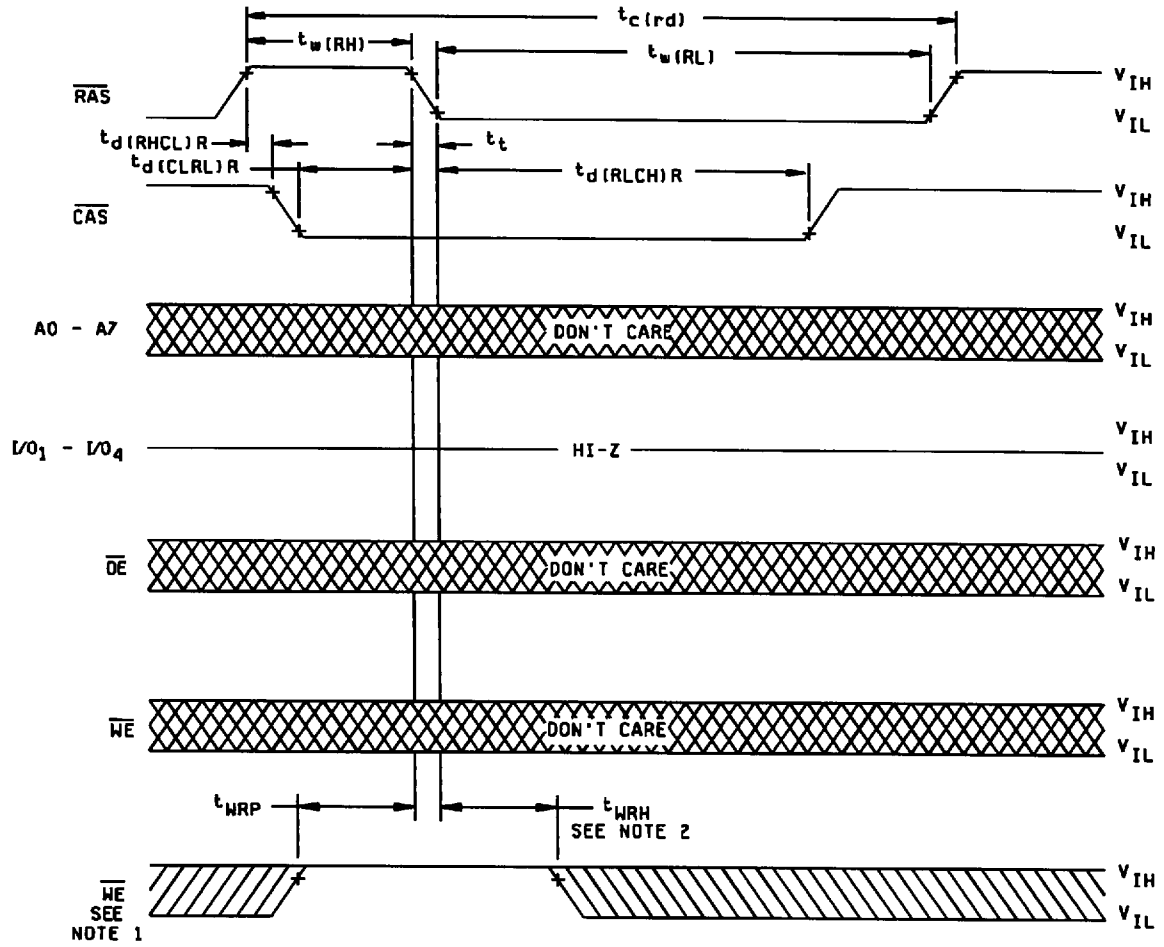


FIGURE 5. Switching waveforms - continued.

Automatic ($\overline{CAS}$-before-$\overline{RAS}$) refresh cycle timing



NOTES:
1. This specific $\overline{WE}$ waveform is only applicable to device types 04 -06.
2. $\overline{WE}$ must be high for $\overline{RAS}$ low transition to insure proper operation.

FIGURE 5. Timing wave diagrams - Continued.

Hidden refresh cycle

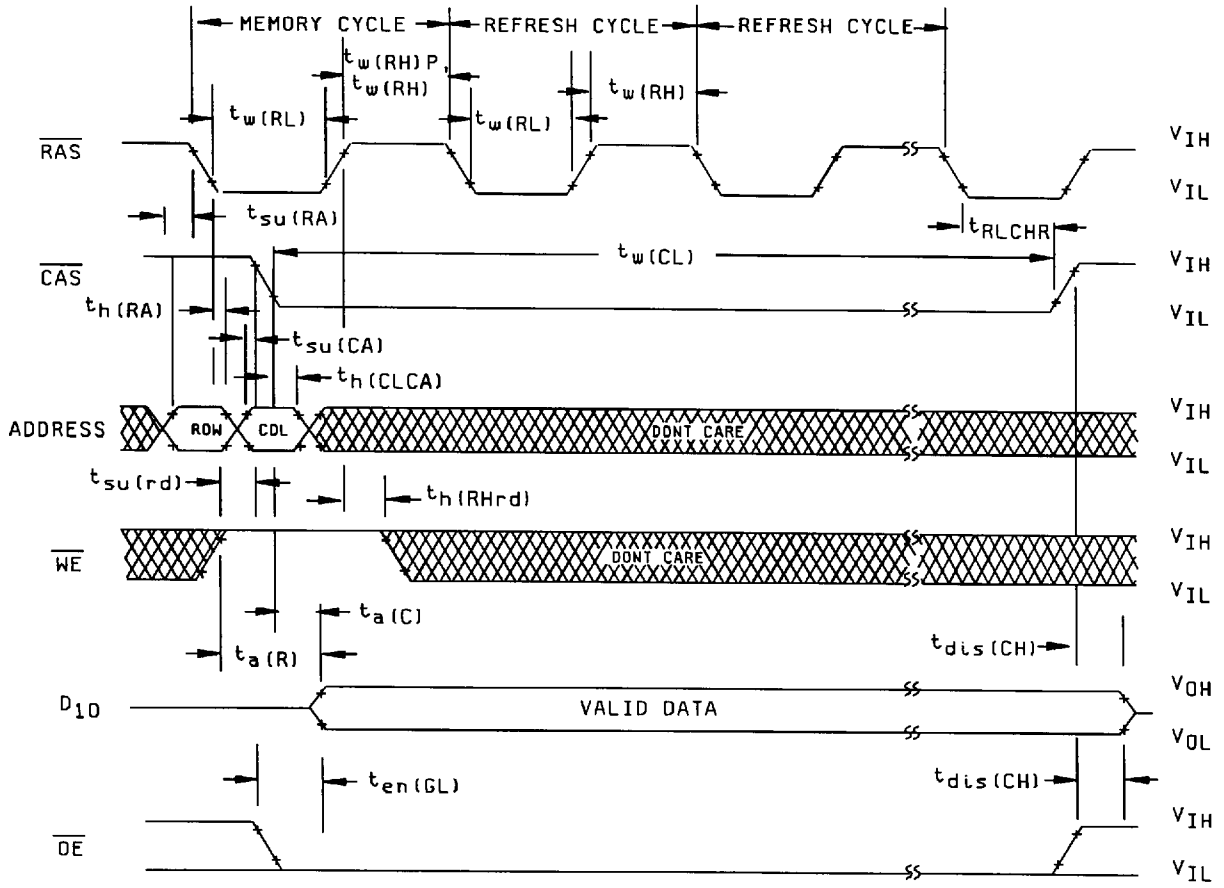


FIGURE 5. Switching waveforms - continued.

4.2.2 Additional criteria for device classes Q and V.

a. The burn-in test duration, test condition and test temperature, or approved alternatives shall be as specified in the device manufacturer's QM plan in accordance with MIL-PRF-38535. The burn-in test circuit shall be maintained under document revision level control of the device manufacturer's Technology Review Board (TRB) in accordance with MIL-PRF-38535 and shall be made available to the acquiring or preparing activity upon request. The test circuit shall specify the inputs, outputs, biases, and power dissipation, as applicable, in accordance with the intent specified in test method 1015 of MIL-STD-883.

b. Interim and final electrical test parameters shall be as specified in table IIA herein.

c. Additional screening for device class V beyond the requirements of device class Q shall be as specified in MIL-PRF-38535, appendix B.

4.3 Qualification inspection for device classes Q and V. Qualification inspection for device classes Q and V shall be in accordance with MIL-PRF-38535. Inspections to be performed shall be those specified in MIL-PRF-38535 and herein for groups A, B, C, D, and E inspections (see 4.4.1 through 4.4.4).

4.4 Conformance inspection. Technology conformance inspection for classes Q and V shall be in accordance with MIL-PRF-38535 including groups A, B, C, D, and E inspections and as specified herein except where option 2 of MIL-PRF-38535 permits alternate in-line control testing. Quality conformance inspection for device class M shall be in accordance with MIL-PRF-38535, appendix A and as specified herein. Inspections to be performed for device class M shall be those specified in method 5005 of MIL-STD-883 and herein for groups A, B, C, D, and E inspections (see 4.4.1 through 4.4.4).

4.4.1 Group A inspection.

a. Tests shall be as specified in table IIA herein.

b. Subgroups 5 and 6 of table I of method 5005 of MIL-STD-883 shall be omitted.

c. For device class M, subgroups 7 and 8 tests shall be sufficient to verify the truth table. For device classes Q and V, subgroups 7 and 8 shall include verifying the functionality of the device; these tests shall have been fault graded in accordance with MIL-STD-883, test method 5012 (see 1.5 herein).

d. O/V (latch-up) tests shall be measured only for initial qualification and after any design or process changes which may affect the performance of the device. For device class M, procedures and circuits shall be maintained under document revision level control by the manufacturer and shall be made available to the preparing activity or acquiring activity upon request. For device classes Q and V, the procedures and circuits shall be under the control of the device manufacturer's TRB in accordance with MIL-PRF-38535 and shall be made available to the preparing activity or acquiring activity upon request. Testing shall be on all pins, on five devices with zero failures. Latch-up test shall be considered destructive. Information contained in JEDEC Standard number 17 may be used for reference.

e. Subgroup 4 (C_{IN} and C_{OUT} measurements) shall be measured only for initial qualification and after any process or design changes which may affect input or output capacitance. Capacitance shall be measured between the designated terminal and GND at a frequency of 1 MHz. Sample size is 15 devices with no failures, and all input and output terminals tested.

4.4.2 Group C inspection. The group C inspection end-point electrical parameters shall be as specified in table IIA herein.

4.4.2.1 Additional criteria for device class M.

a. Steady-state life test conditions, method 1005 of MIL-STD-883:

(1) Test condition D. The test circuit shall be maintained by the manufacturer under document revision level control and shall be made available to the preparing or acquiring activity upon request. The test circuit shall specify the inputs, outputs, biases, and power dissipation, as applicable, in accordance with the intent specified in test method 1005.

(2) T_A = +125°C, minimum.

(3) Test duration: 1,000 hours, except as specified in method 1005 of MIL-STD-883.

TABLE IIA. Electrical test requirements. 1/ 2/ 3/ 4/ 5/ 6/ 7/

Line no.	Test requirements	Subgroups (in accordance with MIL-STD-883, method 5005, table I)	Subgroups (in accordance with MIL-PRF-38535, table III)	
		Device class M	Device class Q	Device class V
1	Interim electrical parameters (see 4.2)		1,7,9	1,7,9
2	Static burn-in I and II (method 1015)	Not required	Not required	Required
3	Same as line 1			1*,7* Δ
4	Dynamic burn-in (method 1015)	Required	Required	Required
5	Same as line 1			1*,7* Δ
6	Final electrical parameters	1*,2,3,7*, 8A,8B,9,10, 11	1*,2,3,7*, 8A,8B,9,10, 11	1*,2,3,7*, 8A,8B,9, 10,11
7	Group A test requirements	1,2,3,4**,7, 8A,8B,9,10, 11	1,2,3,4**,7, 8A,8B,9,10, 11	1,2,3,4**,7, 8A,8B,9,10, 11
8	Group C end-point electrical parameters	2,3,7, 8A,8B	1,2,3,7, 8A,8B Δ	1,2,3,7, 8A,8B,9, 10,11 Δ
9	Group D end-point electrical parameters	2,3, 8A,8B	2,3, 8A,8B	2,3, 8A,8B
10	Group E end-point electrical parameters	1,7,9	1,7,9	1,7,9

1/ Blank spaces indicate tests are not applicable.
2/ Any or all subgroups may be combined when using high-speed testers.
3/ Subgroups 7 and 8 functional tests shall verify the truth table.
4/ * indicates PDA applies to subgroup 1 and 7.
5/ ** see 4.4.1e.
6/ Δ indicates delta limit (see table IIB) shall be required where specified, and the delta values shall be computed with reference to the previous interim electrical parameters (see line 1).
7/ See 4.4.1d.

TABLE IIB. Delta limits at +25°C.

Parameter 1/	Device types
	All
I_{CC3} standby	±10% of specified value in table I.
I_{IH}, I_{IL}, I_{OL}, I_{OH}	±10% of specified value in table I.

1/ The above parameter shall be recorded before and after the required burn-in and life tests to determine the delta.

4.4.2.2 Additional criteria for device classes Q and V. The steady-state life test duration, test condition and test temperature, or approved alternatives shall be as specified in the device manufacturer's QM plan in accordance with MIL-PRF-38535. The test circuit shall be maintained under document revision level control by the device manufacturer's TRB in accordance with MIL-PRF-38535 and shall be made available to the acquiring or preparing activity upon request. The test circuit shall specify the inputs, outputs, biases, and power dissipation, as applicable, in accordance with the intent specified in test method 1005 of MIL-STD-883.

4.4.3 Group D inspection. The group D inspection end-point electrical parameters shall be as specified in table IIA herein.

4.4.4 Group E inspection. Group E inspection is required only for parts intended to be marked as radiation hardness assured (see 3.5 herein). RHA levels for device classes M, Q and V shall be as specified in MIL-PRF-38535. End-point electrical parameters shall be as specified in table IIA herein.

a. End-point electrical parameters shall be as specified in table IIA herein.

b. For device class M, the devices shall be subjected to radiation hardness assured tests as specified in MIL-PRF-38535, appendix A, for the RHA level being tested. For device classes Q and V, the devices or test vehicle shall be subjected to radiation hardness assured tests as specified in MIL-PRF-38535 for the RHA level being tested. All device classes must meet the postirradiation end-point electrical parameter limits as defined in table I at T_A = +25°C ±5°C, after exposure, to the subgroups specified in table IIA herein.

c. When specified in the purchase order or contract, a copy of the RHA delta limits shall be supplied.

4.5 Delta measurements for device class V. Delta measurements, as specified in table IIA, shall be made and recorded before and after the required burn-in screens and steady-state life tests to determine delta compliance. The electrical parameters to be measured, with associated delta limits are listed in table IIB. The device manufacturer may, at his option, either perform delta measurements or within 24 hours after life test perform final electrical parameter tests, subgroups 1, 7, 9.

5. PACKAGING

5.1 Packaging requirements. The requirements for packaging shall be in accordance with MIL-PRF-38535 for device classes Q and V or MIL-PRF-38535, appendix A for device class M.

6. NOTES

6.1 Intended use. Microcircuits conforming to this drawing are intended for use for government microcircuit applications (original equipment), design applications, and logistics purposes.

6.1.1 Replaceability. Microcircuits covered by this drawing will replace the same generic device covered by a contractor-prepared specification or drawing.

6.1.2 Substitutability. Device class Q devices will replace device class M devices.

6.2 Configuration control of SMD's. All proposed changes to existing SMD's will be coordinated with the users of record for the individual documents. This coordination will be accomplished in accordance with MIL-STD-973 using DD Form 1692, Engineering Change Proposal (Short Form).

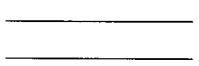
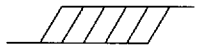
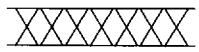
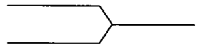
6.3 Record of users. Military and industrial users shall inform Defense Supply Center Columbus when a system application requires configuration control and which SMD's are applicable to that system. DSCC will maintain a record of users and this list will be used for coordination and distribution of changes to the drawings. Users of drawings covering microelectronics devices (FSC 5962) should contact DSCC-VA, telephone (614) 692-0525.

6.4 Comments. Comments on this drawing should be directed to DSCC-VA, Columbus, Ohio 43216-5000, or telephone (614) 692-0674.

6.5 Abbreviations, symbols, and definitions. The abbreviations, symbols, and definitions used herein are defined in MIL-PRF-38535 and MIL-STD-1331, and as follows.

C_{IN} ..... Input terminal capacitance.
C_{OUT} ..... Output and bidirectional output terminal capacitance.
GND ..... Ground zero voltage potential.
I_{CC} ..... Supply current.
I_I ..... Input current.
I_O ..... Output current.
T_C ..... Case temperature.
V_{CC} ..... Positive supply voltage.

6.5.1 Waveforms.

Waveform symbol	Input	Output
	MUST BE VALID	WILL BE VALID
	CHANGE FROM H TO L	WILL CHANGE FROM H TO L
	CHANGE FROM L TO H	WILL CHANGE FROM L TO H
	DON'T CARE ANY CHANGE PERMITTED	CHANGING STATE UNKNOWN
		HIGH IMPEDANCE

6.6 Sources of supply.

6.6.1 Sources of supply for device classes Q and V. Sources of supply for device classes Q and V are listed in QML-38535. The vendors listed in QML-38535 have submitted a certificate of compliance (see 3.6 herein) to DSCC-VA and have agreed to this drawing.

6.6.2 Approved sources of supply for device class M. Approved sources of supply for class M are listed in MIL-HDBK-103. The vendors listed in MIL-HDBK-103 have agreed to this drawing and a certificate of compliance (see 3.6 herein) has been submitted to and accepted by DSCC-VA.

APPENDIX

FUNCTIONAL ALGORITHMS 1/

10. SCOPE

10.1 Scope. Functional algorithms are test patterns which define the exact sequence of events used to verify proper operation of a random access memory (RAM). Each algorithm serves a specific purpose for the testing of the device. It is understood that all manufacturers do not have the same test equipment; therefore, it becomes the responsibility of each manufacturer to guarantee that the test patterns described herein are followed as closely as possible, or equivalent patterns be used that serve the same purpose. Each manufacturer should demonstrate that this condition will be met. Algorithms shall be applied to the device in a topologically pure fashion. This appendix is a mandatory part of the specification. The information contained herein is intended for compliance.

20. APPLICABLE DOCUMENTS. This section is not applicable to this appendix.

30. ALGORITHMS

30.1 Algorithm A (pattern 1).

30.1.1 Output high impedance (t_{OFF}). This pattern verifies the output buffer switches to high impedance (three-state) within the specified t_{OFF} after the rise of $\overline{CAS}$. It is performed in the following manner:

Step 1: Perform 8 pump cycles.
Step 2: Load address location with data.
Step 3: Raise $\overline{CAS}$ and read address location and guarantee $V_{OL} < V_{OUT} < V_{OH}$ after t_{OFF} delay.

30.2 Algorithm B (pattern 2).

30.2.1 V_{CC} slew. This pattern indicates sense amplifier margin by slewing the supply voltage between memory writing and reading. It is performed in the following manner:

Step 1: Perform 8 pump cycles.
Step 2: Load memory with background data with V_{CC} at 5.0 V.
Step 3: Change V_{CC} to 5.5 V.
Step 4: Read memory with background data.
Step 5: Load memory with background data complement.
Step 6: Change V_{CC} to 4.5 V.
Step 7: Read memory with background data complement.

30.3 Algorithm C (pattern 3).

30.3.1 March data. This pattern tests for address uniqueness and multiple selection. It is performed in the following manner:

Step 1: Perform 8 pump cycles.
Step 2: Load memory with background data.
Step 3: Read location 0.
Step 4: Write data complement in location 0.
Step 5: Repeat steps 3 and 4 for all other locations in the memory (sequentially).
Step 6: Read data complement in maximum address location.
Step 7: Write data in maximum address location.
Step 8: Repeat steps 6 and 7 for all other locations in the memory from maximum to minimum address.
Step 9: Read data in maximum address location.
Step 10: Write data complement in maximum address location.
Step 11: Repeat steps 6 and 7 for all other locations in the memory from maximum to minimum address.
Step 12: Read memory with data complement.

1/ For device types 04 - 06 only, a 1MEG x 4 die is used and bonded out to produce a 64K x 4 array. Therefore, it is not possible to apply a true topologically pure algorithm. For details regarding testing to verify proper device operation in lieu of functional algorithms, contact the supplying vendor.

30.4 Algorithm D (pattern 4).

30.4.1 Refresh test (cell retention) +125°C only. This test is used to check the retention time of the memory cells. It is performed in the following manner:

Step 1: Perform 8 pump cycles.
Step 2: Load memory with background data.
Step 3: Pause t_{REF} (stop all clocks).
Step 4: Read memory with background data.
Step 5: Repeat steps 2 through 4 with data complement.

30.5 Algorithm E (pattern 5).

30.5.1 Read-modify-write (RMW). This pattern verifies the Read-modify-write mode for the memory. It is performed in the following manner:

Step 1: Perform 8 pump cycles.
Step 2: Load memory with background data.
Step 3: Read memory with data and load with data complement using RMW cycle.
Step 4: Repeat step 3 for all address locations.
Step 5: Repeat steps 2 and 3 using data complement.

30.6 Algorithm F (pattern 6).

30.6.1 Page mode. This pattern verifies the Page mode for the memory. It is performed in the following manner:

Step 1: Perform 8 pump cycles.
Step 2: Load first page of memory with background data using Page mode cycle.
Step 3: Read first page of memory with data and load with data complement using Page mode cycle.
Step 4: Read first page of memory with data complement and load with data using Page mode cycle.
Step 5: Repeat steps 2 through 4 for remaining memory locations.

30.7 Algorithm G (pattern 7).

30.7.1 $\overline{\text{CAS}}$-before-$\overline{\text{RAS}}$ refresh test. This test is used to verify the functionality of the $\overline{\text{CAS}}$ before $\overline{\text{RAS}}$ mode of cell refreshing. It is done at +125°C only and is performed in the following manner:

Step 1: Perform 8 pump cycles.
Step 2: Load memory with background data.
Step 3: Perform 1024 CAS-before-RAS cycles while attempting to modify data.
Step 4: Read memory with background data.

30.8 Algorithm H (pattern 8).

30.8.1 $\overline{\text{RAS}}$-only refresh test. This test is used to verify the functionality of the $\overline{\text{RAS}}$-only mode of cell refreshing. It is done at +125°C only and is performed in the following manner:

Step 1: Perform 8 pump cycles.
Step 2: Load memory with background data.
Step 3: Perform 1024 RAS-only cycles while attempting to modify data.
Step 4: Repeat step 3 for 1 second.
Step 5: Read memory with background data.

STANDARD MICROCIRCUIT DRAWING SOURCE APPROVAL BULLETIN

DATE: 98-11-05

Approved sources of supply for SMD 5962-92132 are listed below for immediate acquisition only and shall be added to MIL-HDBK-103 and QML-38535 during the next revision. MIL-HDBK-103 and QML-38535 will be revised to include the addition or deletion of sources. The vendors listed below have agreed to this drawing and a certificate of compliance has been submitted to and accepted by DSCC-VA. This bulletin is superseded by the next dated revision of MIL-HDBK-103 and QML-38535 .

Standard microcircuit drawing PIN 1/	Vendor CAGE number	Vendor similar part number 2/
5962-9213201MVX	3/	MT4C4067C-10 883C
5962-9213201MXX	3/	MT4C4067EC-10 883C
5962-9213201MYX	3/	MT4C4067EA-10 883C
5962-9213202MVX	3/	MT4C4067C-12 883C
5962-9213202MXX	3/	MT4C4067EC-12 883C
5962-9213202MYX	3/	MT4C4067EA-12 883C
5962-9213203MVX	3/	MT4C4067C-15 883C
5962-9213203MXX	3/	MT4C4067EC-15 883C
5962-9213203MYX	3/	MT4C4067EA-15 883C
5962-9213204MVA	0EU86	MT4C4067C-10 883C
5962-9213204MXA	0EU86	MT4C4067EC-10 883C
5962-9213204MYA	0EU86	MT4C4067EA-10 883C
5962-9213205MVA	0EU86	MT4C4067C-12 883C
5962-9213205MXA	0EU86	MT4C4067EC-12 883C
5962-9213205MYA	0EU86	MT4C4067EA-12 883C
5962-9213206MVA	0EU86	MT4C4067C-15 883C
5962-9213206MXA	0EU86	MT4C4067EC-15 883C
5962-9213206MYA	0EU86	MT4C4067EA-15 883C

1/ The lead finish shown for each PIN representing a hermetic package is the most readily available from the manufacturer listed for the part. If the desired lead finish is not listed, contact the Vendor to determine its availability.

2/ Caution. Do not use this number for item acquisition. Items acquired to this number may not satisfy the performance requirements of this drawing.

3/ Although no longer available from an approved source, these devices have been replaced by device types 04 - 06 using a 1Meg x 4 die bonded out to produce a 64K x 4 array.

Vendor CAGE number	Vendor name and address
0EU86	Austin Semiconductor Inc. 8701 Cross Park Drive Austin, TX 78754-4566

The information contained herein is disseminated for convenience only and the Government assumes no liability whatsoever for any inaccuracies in this information bulletin.