Winbond Electronics Corp.

AN-CS006a

W682388 Pro-X™ CODEC Layout Guideline

1. W682388 Layout Considerations

The Winbond W682388 Pro-X™ CODEC family is an excellent solution for short loop telephony applications. Place the components carefully to insure best performance. This document outlines critical component layout issues. Use it together with the W682388 data sheet and other supporting Pro-X application notes.

The W682388 will exhibit high-quality low-noise performance with the appropriate layout design. Pins 52–61 are sensitive current input pins that are susceptible to induced noise. Keep traces between these pins and their respective components (C7, C8, C10, C11, R13–16, and R18–27) to a minimum length. Do not route any digital traces near these sensitive traces.

Place the line compensation capacitors, C5, C8, C9, and C12, near their respective TIP and RING output pins. Place a 0.1 µF ceramic decoupling capacitor as close as possible to each VDD and VBAT power supply input pin. These are Pin 49 (VDD1), Pin 64 (VDD2), Pin 41 (VDD3), Pin 8 (VDD4), Pin 27 (VDD5) and Pin 26 (VDDL). Replace the 0.1 µF capacitors at VDD1 and VDD2 with 10 µF ceramic capacitors for additional noise performance. Refer to the Figure 3 for an example of this layout.

There are two external Tip and Ring capacitors for each channel. They are connected to CT1 (Pin 39), CR1 (Pin 38), CT2 (Pin 10), and CR2 (Pin 11). The capacitor is a 10 µF ceramic (low leakage) capacitor. It is connected to 3.3V. Route the capacitors directly to the appropriate VDD pin. For example, the CT1 and CR1 capacitors connect directly to their respective pins. Their shared 3.3V connection is routed directly to VDD1 before connecting to the main 3.3V supply. The situation is the same for CT2 and CR2, which must terminate at VDD2.

The AFE transistors QR3/QT3 (SOT-223) and QR1/QT1 (SOT-89) should have exposed copper pads to help reduce the thermal resistance of these components. The amount of copper used for the heat sink in combination with the surface area of the PCB will improve the heat dissipation of the transistor package.

One way to increase the copper area when board space is limited is to connect the pad used for the heat sink by using multiple layers. A top and bottom side can be used with multiple vias connecting them together. The optimal copper area to heat sink a SOT-223 is 1 sq inch. This approach is similar to heat sinking used for the QFN package. (Refer to Section 4 on QFN grounding)

Place the resistors for IREF (Pin 13) and the transconductance amplifiers (Pins 3,5,44 and 46) as close as possible to the part to minimize the trace length. These resistors are R29, R30 and R31.

If more than two layers are used for the overall board circuit, separate analog and digital trace layers may enhance performance. Digital signals are best applied to a dedicated layer. The ideal approach is to separate digital layers from analog layers by a power/ground plane.

Idle Channel Noise (ICN) performance can be further improved by splitting the 3.3V power plane. This way the front end power (VDD1 – VDD4) and ground (GND1 – GND4 & VSSP) will be isolated from the main 3.3V and Ground planes by using ferrite beads.

2. DC-TO-DC Converter Layout

The W682388 DC-to-DC converter circuit uses pulse width modulation to generate the desired voltages. Lay out this circuit carefully to minimize the contributed noise from the high switching currents. The DC-to-DC converter has specific areas to optimize to minimize this noise effect. The critical areas are described below:

Loop 1 in Figure 1 is the secondary fly-back current path that generates the negative VBAT potential. Place the components in this area in a tight loop. Cover the open areas in between with as much copper as possible.

Loop 2 in Figure 1 is the primary input current loop for the DC-to-DC converter from the unregulated power supply. Place the capacitors in this area near the sense resistor to maximize results.

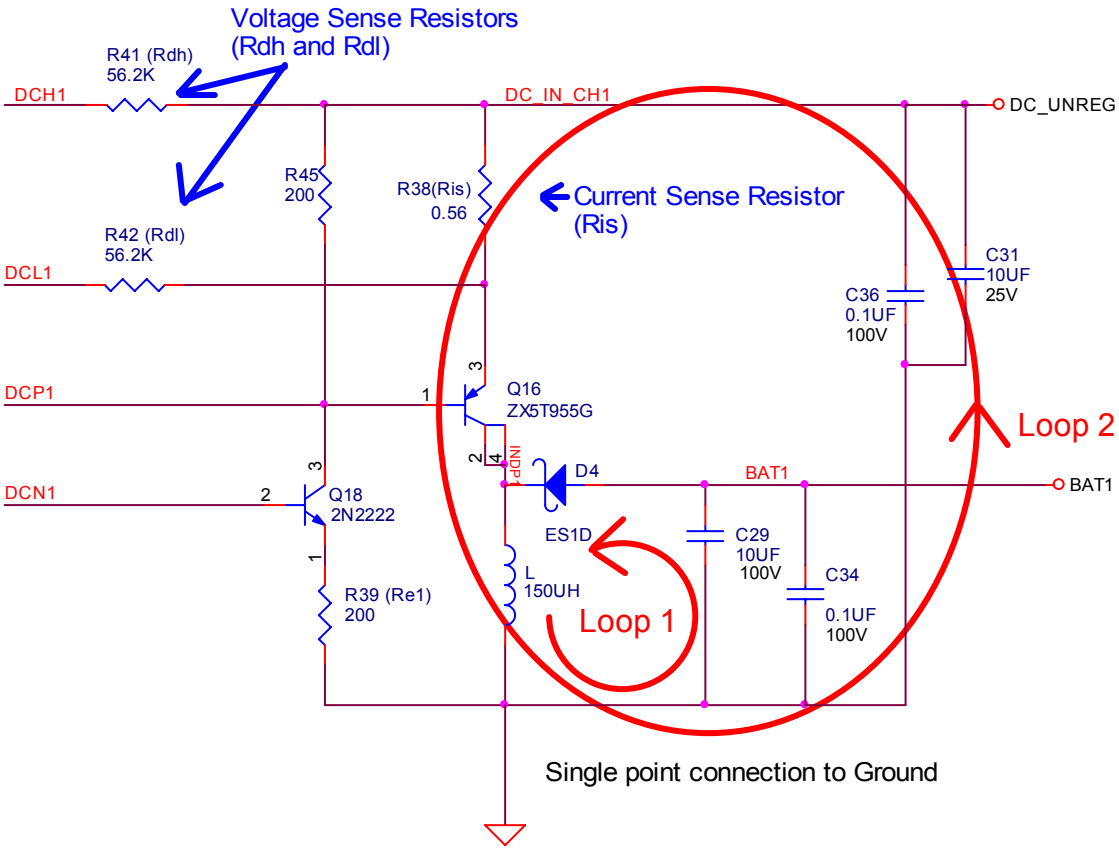

Figure 1. DC-to-DC Converter Circuit

DC-to-DC converter layout recommendations:

1) The perimeters of loops (1) & (2) must be as short as possible.
2) The high current paths must use large trace widths: typically WVDC>WVBAT>5 mm [200 mils.]
3) The Ground connection should be extended with multiple vias (3) in the case of inner layer or bottom layer ground plane (WVIAS<10 mm.)
4) Even a small ground plane is better than no ground plane at all.
5) Node N must have a very small area (low capacitance to ground.)
6) CVDC and CVBAT should be low ESR (or add a parallel ceramic capacitor to an electrolytic capacitor.)
7) Lay out the diode, the transistor and the inductor as tightly as possible, preferably in a 15 mm by 15 mm square. It is most important that the layout of the diode, the capacitors and the inductor be as tight as possible. The inductor can be used as a heat sink for the switching transistor by merging and increasing the copper planes.

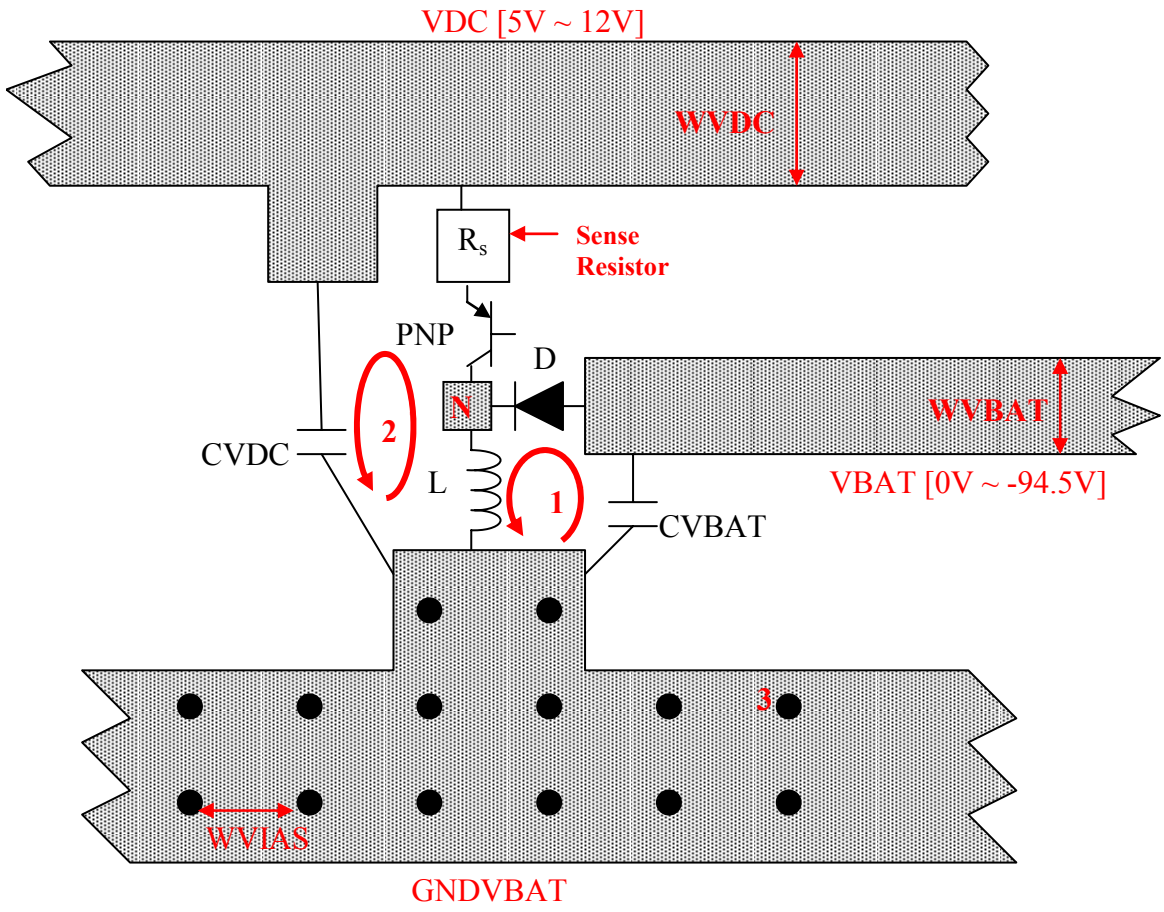

Figure 2. DC-to-DC switch cell layout

3. Layout Example

The following layout example uses the W682388_RB1 Daughter Board.

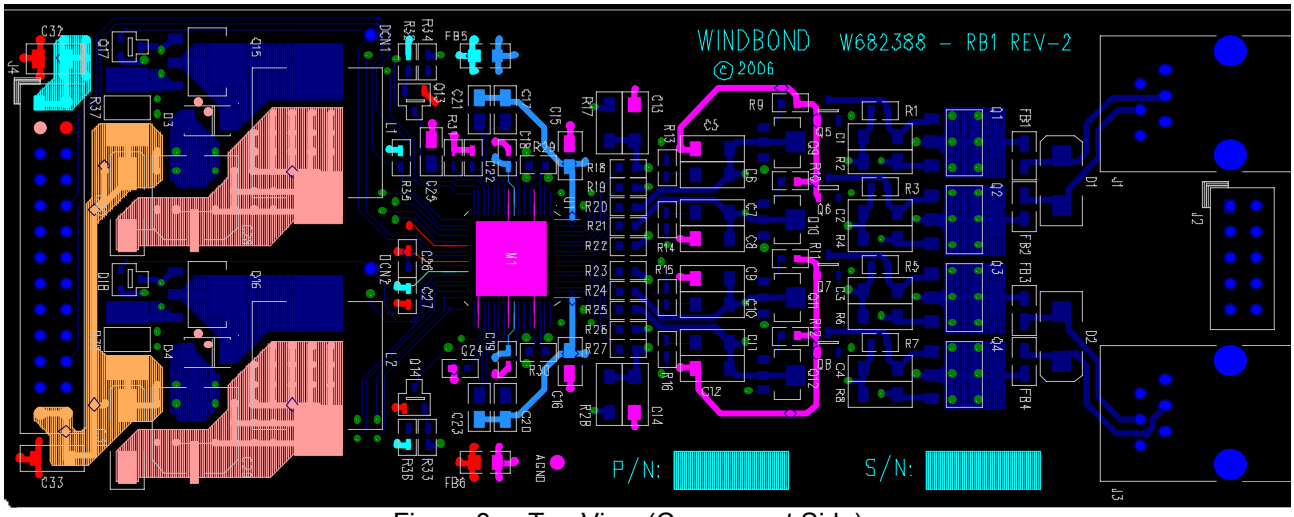

Figure 3a. Top View (Component Side)

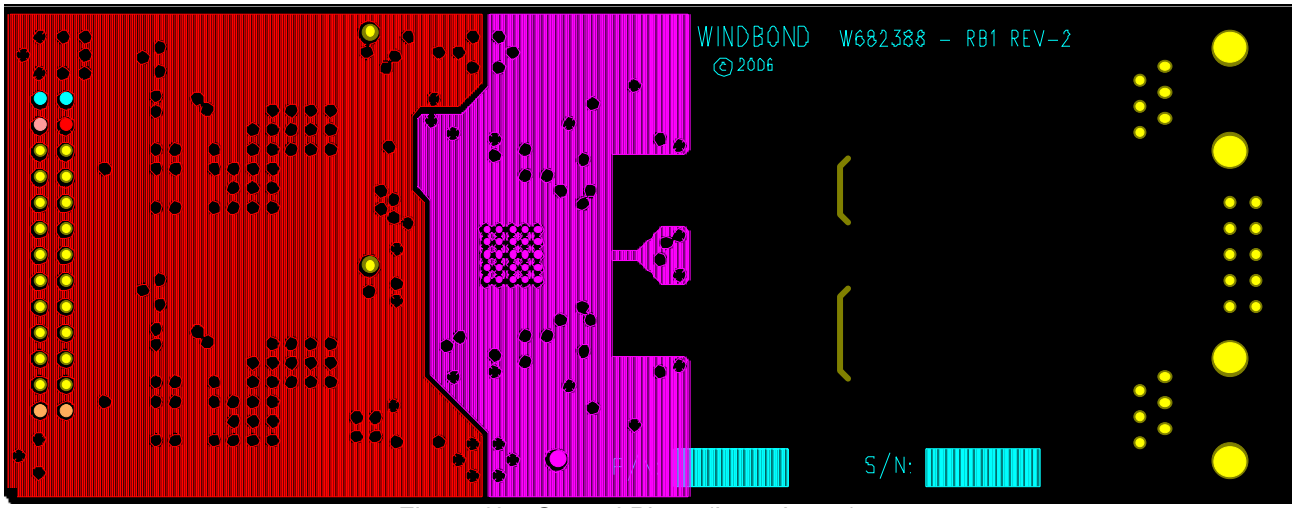

Figure 3b. Ground Plane (Inner Layer)

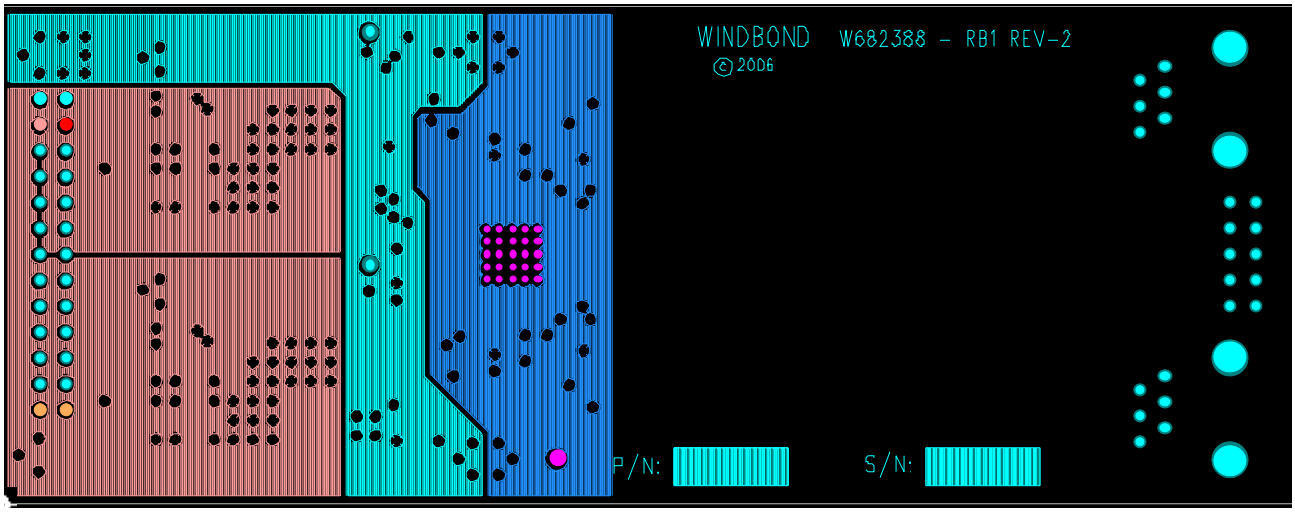

Figure 3c. Power Plane (Inner Layer))

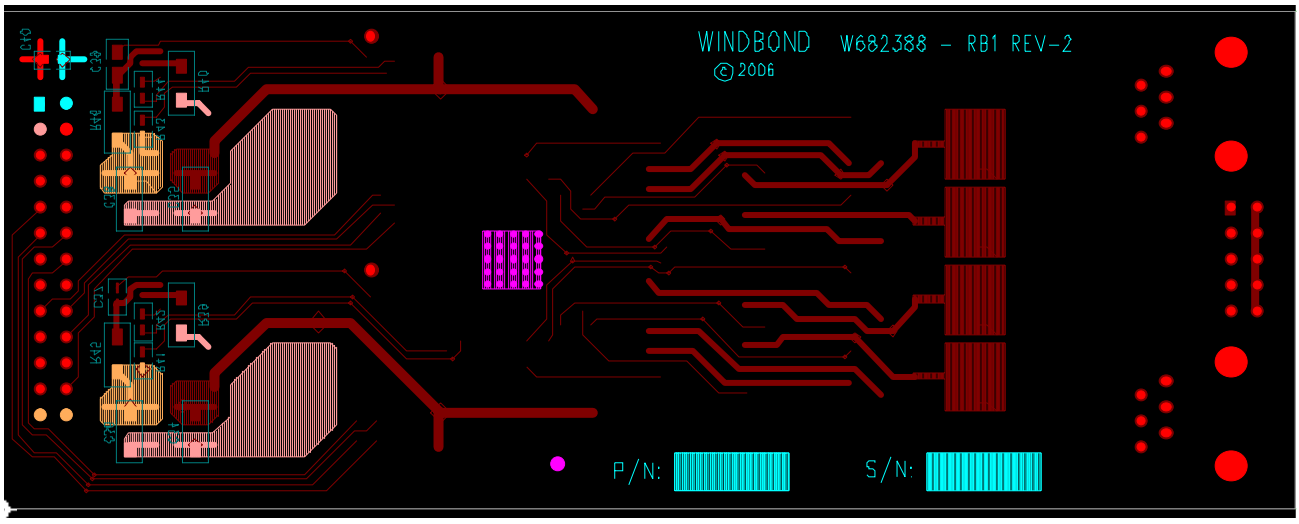

Figure 3d. Bottom View (Solder Side)

4. QFN Package Grounding

The W682388 QFN package uses an exposed pad to dissipate thermal energy. For best thermal performance of the package, solder the exposed pads to multiple ground planes. A top side, bottom side, and one inner ground plane must be used. There must be multiple vias connecting them together. Twenty-five vias should be used in a 5x5 grid under the W682388. The size of the vias used for the W682388 EPad should be at least 10 mils. (Refer to Figures 4, 5, and 6.)

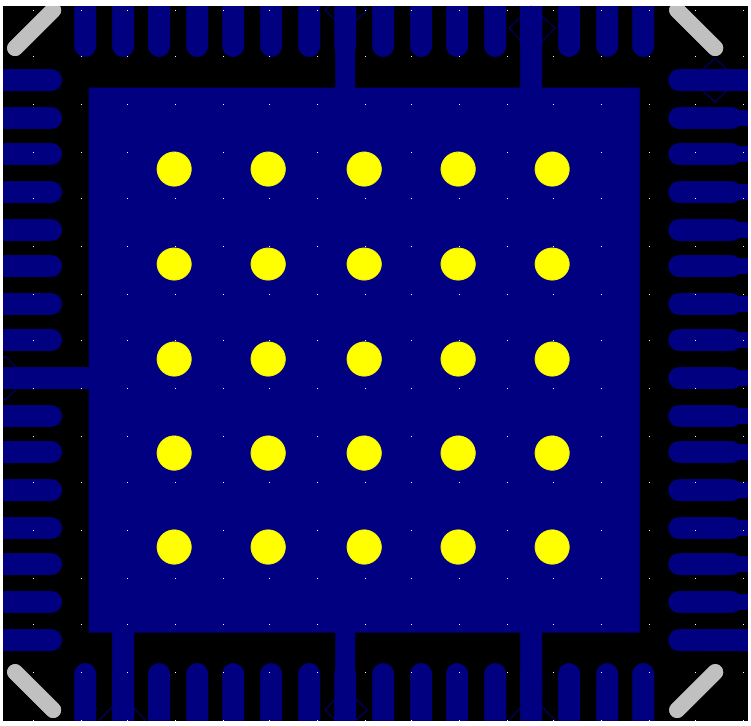

Figure 4. EPad Top Layer (Component Side)

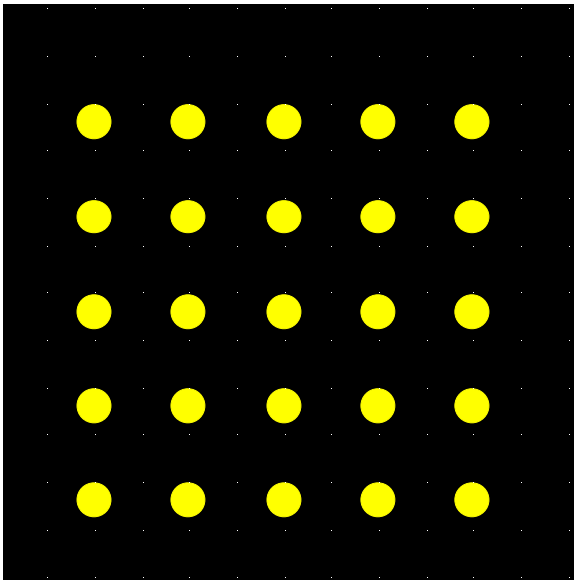

Figure 5. EPad Ground (Inner Layer)

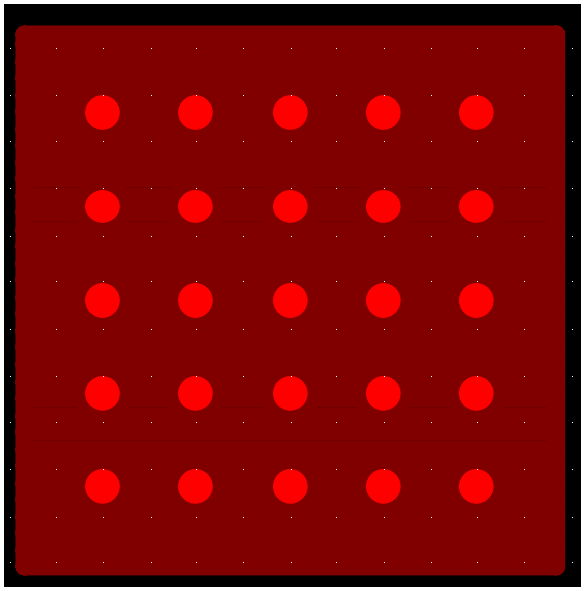

Figure 6. EPad Bottom Layer (Solder Side)

5. Layout Check List

Perform the following steps to have high quality, low-noise performance:

1. Copy the W682388 evaluation board/example layout as closely as possible.
2. Place the DC-TO-DC converter near pins 17-32 of the W682388 device as on the evaluation board.
3. Put no power/ground planes under the protection circuitry in the front end.
4. Isolate the Analog front end power (VDD1, VDD2, VDD3, VDD4) and ground (GND1, GND2, GND3, GND4, VSSP) by connecting them to the main 3.3v / GND planes using ferrite beads.
5. Route analog traces away from digital traces. Stay away from pins 17 and 32 of W682388.
6. VDD capacitors should be placed close to the power and ground pins. Connect all power and ground connections between the power pins and the bypass capacitors together with short traces.
7. Use separate GND and digital trace layers if the board has four or more layers, ideally separated by a power/GND plane.
8. Place the sense resistors (R18, R19, R20, R21, R22, R23, R24, R25, R26, R27), the IREF resistor (R31) and transconductance resistors (R29 & 30) as close to the pins as possible. Have no digital traces in path.
9. Width of high current traces (i.e. DC-to-DC converter, etc.), should be at least 50 mils.
10. Width of the Tip and Ring traces must be as wide as possible.
11. Keep the components and traces related to the DC-to-DC converter isolated. Avoid running a trace away from these components and traces.
12. Each DC-TO-DC converter must have a separate ground trace leading back to the supply as shown in Figure 1.
13. Minimize the surface area formed by the current sense resistor, Ris (R38), and the voltage sense resistors Rdh and Rdl (R41& R42). Place the voltage sense resistors close to the W682388. Route the voltage sensing trace between Ris to the pair Rdh and Rdl tightly in parallel or on top of each other on two separate layers.

Perform the following steps to optimize the analog front end:

1. Place the discrete transistors near pins 49-65 of the W682388 similar to the evaluation board.
2. Compensation capacitors should be placed as follows:
    1. C9 as close as possible to the collector of transistors QR1_C1 and QR3_C1.
    2. C12 as close as possible to the collector of transistors QT1_C1 and QT3_C1.
    3. C8 as close as possible to the collector of transistors QR1_C2 and QR3_C2.
    4. C5 as close as possible to the collector of transistors QT1_C2 and QT3_C2.

The AFE transistors QR3/QT3 (SOT-223) and QR1/QT1 (SOT-89) should have exposed copper pads to help reduce the thermal resistance of these components. The amount of copper used for the heat sink in combination with the surface area of the PCB will improve the heat dissipation of the transistor package.

One way to increase the copper area when board space is limited is to connect the pad used for the heat sink by using multiple layers. A top and bottom side can be used with multiple vias connecting them together. The optimal copper area to heat sink a SOT-223 is 1 sq inch. This approach is similar to heat sinking used for the QFN package. (Refer to Section 4 on QFN grounding)

6. VERSION HISTORY

VERSION	DATE	PAGE	DESCRIPTION
1.1	March 21, 2006		Initial revision
1.2	April 17, 2006	1,4,5,7	Modified per new layout and schematic annotation.
1.3	June 21, 2006	1,2,3,7,8	Added paragraph on AFE layout and heat sinking. Changed a few words for clarity. Corrected typos.

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