EPSON

SED1640

Dot Matrix High Duty LCD Driver

Wide Voltage Operation Products

- 80-bit Output
- 1/300 Duty Max.
- 2.7 to 5.5Vdc Logic Power Supply

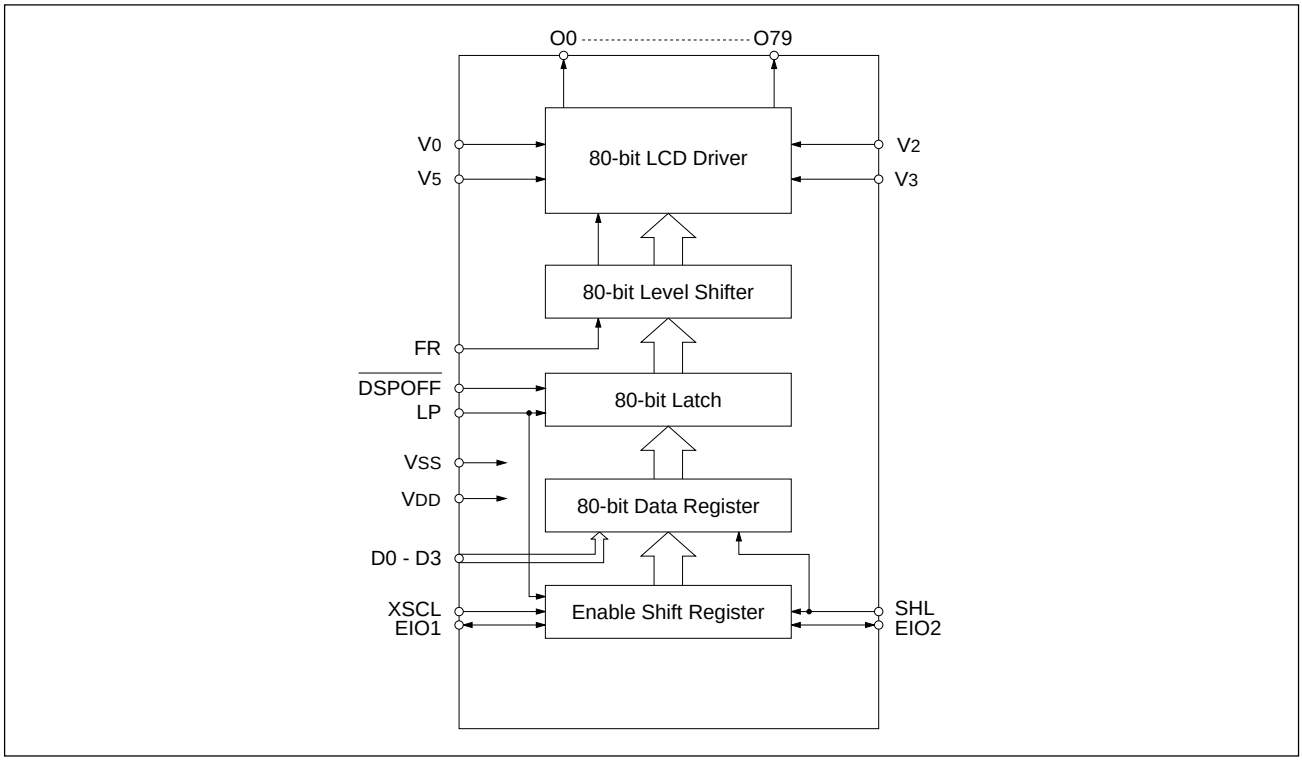
■ DESCRIPTION

The SED1640 is the 80-segment (column) output driver that is appropriate to driving of a large-capacity, dot-matrix LCD panel.
The chip has been designed to improve the LCD display quality and it provides the high-speed enable chain method useful for lower power operation. The flat chip design allows more compact LCD panel production. The logic power supply allows low-voltage operation in a wide range of applications.

■ FEATURES

- No. of LCD drive outputs 80
- Super slim chip design
- Low current consumption
- Low voltage operation ..... –2.7 Vdc Max.
- Wide range of LCD drive voltages ..... –8 to –28 Vdc
- High-speed data transmission at the low power by 4-bit bus enable chain method ..... Shift clock frequencies : 6.5 MHz (at –2.7 Vdc)
  : 7.5 MHz (at –3.0 Vdc)
- Non-bias display off function
- Available pin selection in output shift direction
- Available offset bias adjustment of LCD power supply for V_{DD} level
- Logic power supply ..... –2.7 to –5.5 Vdc
- Package ..... Die form (Au bump): SED1640D0B

■ BLOCK DIAGRAM



■ PIN DESCRIPTION

<table>
<tr><th>Terminal name</th><th>I/O</th><th>Function</th><th>No. of pins</th></tr>
<tr><td>O0 to O79</td><td>O</td><td>LCD drive segment output; the output changes at the LP falling edge.</td><td>80</td></tr>
<tr><td>D0 to D3</td><td>I</td><td>Display data input</td><td>4</td></tr>
<tr><td>XSCL</td><td>I</td><td>Shift clock input of display data (falling edge trigger)</td><td>1</td></tr>
<tr><td>LP</td><td>I</td><td>Latch pulse input of display data (falling edge trigger)</td><td>1</td></tr>
<tr><td>EIO1</td><td>I/O</td><td>Enable I/O</td><td>2</td></tr>
<tr><td>EIO2</td><td></td><td>The terminals are set to the input or output according to the SHL input signal level. The output is reset by LP input. When the 80-bit data is read, the signal automatically goes high.</td><td></td></tr>
<tr><td>SHL</td><td>I</td><td>Used for shift direction selection and I/O control input of EIO terminal.
If data sets (a, b, c, d) (e, f, g, h) ... (w, x, y, z) are entered in this sequence in terminals (D3, D2, D1, D0), the data and segment output are processed as follows:
<table>
<tr><th rowspan="2">SHL</th><th colspan="7">Output</th><th colspan="2">EIO</th></tr>
<tr><th>79</th><th>78</th><th>77</th><th></th><th>2</th><th>1</th><th>0</th><th>EIO1</th><th>EIO2</th></tr>
<tr><td>L</td><td>a</td><td>b</td><td>c</td><td>…</td><td>x</td><td>y</td><td>z</td><td>Output</td><td>Input</td></tr>
<tr><td>H</td><td>z</td><td>y</td><td>x</td><td>…</td><td>c</td><td>b</td><td>a</td><td>Input</td><td>Output</td></tr>
</table>
Note: The relationship between the data and segment output is determined regardless of the number of shift clocks.</td><td>1</td></tr>
<tr><td>FR</td><td>I</td><td>AC conversion signal input of LCD drive output</td><td>1</td></tr>
<tr><td>V_{DD}, V_{SS}</td><td>Power supply</td><td>Logic power supply V_{DD}: 0 V V_{SS}: –2.7 to –5.5 Vdc</td><td>3</td></tr>
<tr><td>V_0, V_2, V_3
V_5</td><td>Power supply</td><td>Power supply for LCD drive circuit V_{DD}: 0 V
*1</td><td>V_5: –8 to –28 Vdc
$V_{DD} \geqq V_0 \geqq V_2 \geqq 6/9\ V_5$
$3/9\ V_5 \geqq V_3 \geqq V_5$</td><td>8</td></tr>
<tr><td>$\overline{DSPOFF}$</td><td>I</td><td>Forced blank input
When the signal level is low, the output is forcibly set to V0 level.
Note: If this function is used, the SED1631 cannot be used as a pair.</td><td>1</td></tr>
</table>

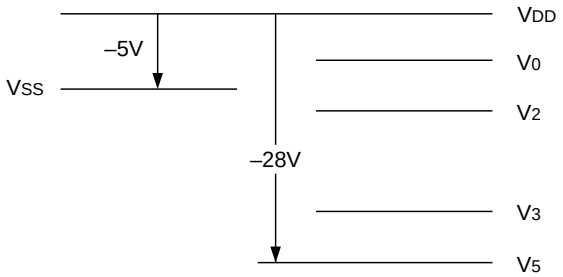
*1 A pair of V0 to V_5 must always be connected to their dedicated LCD power supplies.

Total: 107
(NC: 5)

■ ABSOLUTE MAXIMUM RATING

Rating	Symbol	Value	Unit
Power voltage (1)	V_{SS}	–7.0 to +0.3	V
Power voltage (2)	V_5	–30.0 to +0.3	V
Power voltage (3)	V_0, V_2, V_3	V_5 –0.3 to V_{DD} +0.3	V
Input voltage	V_I	V_{SS} –0.3 to V_{DD} +0.3	V
Output voltage	V_O	V_{SS} –0.3 to V_{DD} +0.3	V
EIO output current	I01	20	mA
Operating temperature	Topr	–40 to +85	˚C
Storage temperature 1	Tstg 1	–65 to +150	˚C
Storage temperature 2	Tstg 2	–55 to +100	˚C

Notes:
1. All voltages are based on V_{DD} = 0 V.
2. Storage temperature 1 defines the storage temperature of the separate chip, and storage temperature 2 defines the TAB mounted chip.
3. The V_0, V_2 and V_3 voltages must always satisfy the following:
   $V_{DD} \geqq V_0 \geqq C2 \geqq C3 \geqq V_5$



4. If the logic power supply is floating or if it exceeds V_{SS} = –2.6 Vdc when the LCD drive is powered, the LSI may be destroyed permanently. Cares must be taken especially when the system power supply is turned on or off.

■ ELECTRICAL CHARACTERISTICS

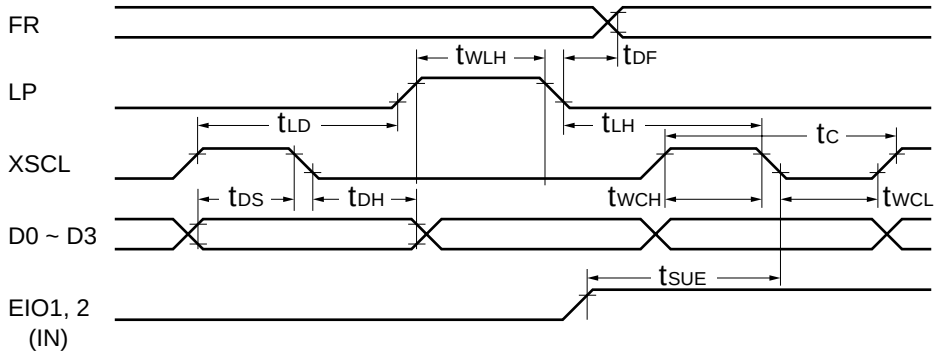
● DC chracteristics

(V_{DD} = V0 = 0 V, V_{SS} = -5.0 Vdc ±10%, Ta = -40 to +85˚C unless otherwise specified.)

Characteristic	Symbol	Condition	Pin applied	Min.	Typ.	Max.	Unit
Power voltage (1)	V_{SS}		V_{SS}	-5.5	-5.0	-2.7	V
Recommended operating voltage	V_5	V_{SS} = -2.7 to -5.5 Vdc	V_5	-28.0		-12.0	V
Operable voltage	V_5	Function	V_5			-8.0	V
Power voltage (2)	V_0	Recommended value	V_0	V_{DD} -2.5		V_{DD}	V
Power voltage (3)	V_2	Recommended value	V_2	3/9V_5			V
Power voltage (4)	V_3	Recommended value	V_3	V_5		6/9V_5	V
High-level input voltage	V_{IH}	V_{SS} = -2.7 to -5.5 Vdc	EIO1, EIO2, FR D0 to D3, XSCL SHL, LP, $\overline{DSPOFF}$	0.2V_{SS}			V
Low-level input voltage	V_{IL}					0.8V_{SS}	V
High-level output voltage	V_{OH}	V_{SS} = -2.7 to -5.5 Vdc, I_{OH} = -0.6 mA	EIO1, EIO2	V_{DD} -0.4			V
Low-level output voltage	V_{OL}	V_{SS} = -2.7 to -5.5 Vdc, I_{OL} = 0.6 mA	EIO1, EIO2			V_{SS} +0.4	V
Input leakage current	ILI	$V_{SS} \leqq V_{IN} \leqq V_{DD}$	D0 to D3, LP, FR, XSCL, SHL, $\overline{DSPOFF}$			2.0	µA
I/O leakage current	ILI/O	V_{SS} V_{IN} V_{DD}	EIO1, EIO2			5.0	µA
Static current	I_{SS}	V_5 = -28.0 to -14.0 Vdc, V_{IH} = V_{DD}, V_{IL} = V_{SS}	V_{SS}			25	µA
Output resistance	R_{SEG}	△V_{ON} = 0.5V, V_5 = -20.0 V, V_3 =13/15 • V_5, V_2 = 2/15 • V_5, V_0 =V_{DD}	O_0 to O_{79}		1.5	2.5	KΩ
Average operating current consumption (1)	I_{SS}	V_{SS} = -5.5 Vdc, V_{IH} = V_{DD}, V_{IL} = V_{SS}, f_{XSCL} = 2.69 MHz, f_{LP} = 16.8 kHz, f_{FR} = 70 Hz, Input data: Stripe display, no load	V_{SS}		0.10	0.2	mA
		V_{SS} = -3.0 Vdc ; others are the same as V_{SS} = -5 Vdc.			0.07	0.15	
Average operating current consumption (2)	I_5	V_{SS} = –5.0 Vdc, V_0 = 0.0 V, V_2 = –9.3 Vdc, V_3 = –18.6 Vdc, V_5 = –28.0 Vdc; others are the same as I_{SS}.	V_5		0.02	0.05	mA
Input terminal capacity	C_I	Freq. = 1 MHz, Ta = 25˚C, separate chip	D0 to D3, LP, FR, XSCL, SHL, $\overline{DSPOFF}$			8	pF
I/O terminal capacity	$C_{I/O}$		EIO1, EIO2			15	pF

● **AC characteristics**

Input timing characteristics



(V_{SS} = –5.0 V ±0.5, Ta = –40 to 85˚C)

Characteristic	Symbol	Condition	Min.	Max.	Unit
XSCL cycle	t_C		100		ns
XSCL high-level pulse width	t_{WCH}		30		ns
XSCL low-level pulse width	t_{WCL}		30		ns
Data setup time	t_{DS}		30		ns
Data hold time	t_{DH}		20		ns
XSCL-to-LP rise time	t_{LD}		0		ns
LP-to-XSCL fall time	t_{LH}		40		ns
LP high-level pulse width	t_{WLH}	*3	40		ns
FR delay allowance time	t_{DF}		–900	+900	ns
EIO setup time	t_{SUE}		35		ns

(V_{SS} = –4.5 V to –2.7 V, Ta = –40 to 85˚C)

Characteristic	Symbol	Condition	Min.	Max.	Unit
XSCL cycle	t_C	V_{SS} = –2.7 V *1	153		ns
		V_{SS} = –3.0 V *2	133		
XSCL high-level pulse width	t_{WCH}		50		ns
XSCL low-level pulse width	t_{WCL}		50		ns
Data setup time	t_{DS}		50		ns
Data hold time	t_{DH}		30		ns
XSCL-to-LP rise time	t_{LD}		0		ns
LP-to-XSCL fall time	t_{LH}	V_{SS} = –2.7 V	75		ns
		V_{SS} = –3.0 V	65		
LP high-level pulse width	t_{WLH}	V_{SS} = –2.7 V *3	75		ns
		V_{SS} = –3.0 V *3	65		
FR delay allowance time	t_{DF}		–900	+900	ns
EIO setup time	t_{SUE}	V_{SS} = –2.7 V	50		ns
		V_{SS} = –3.0 V	40		

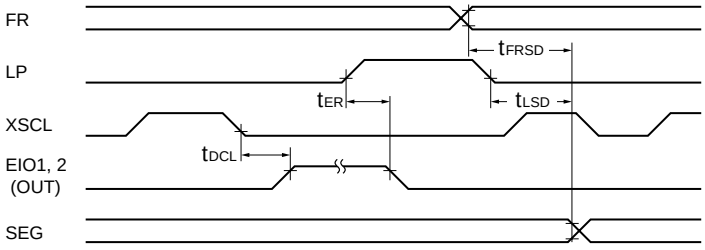
*1 Equivalent to 6.5 MHz

*2 Equivalent to 7.5 MHz

*3 "t_{WLH}" defines the time when LP is high and XSCL is low.

● **AC characteristics**

Output timing characteristics



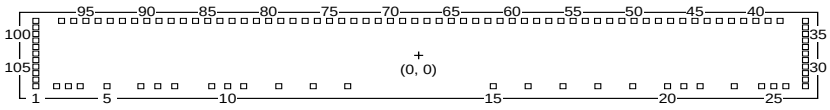
(V_{DD} = –5.0 ±0.5 V, V5 = –12.0 to –28.0 V)

Characteristic	Symbol	Condition	Min.	Max.	Unit
EIO reset time	t_{ER}	C_L = 15 pF (EIO)		90	ns
EIO output delay time	t_{DCL}			55	ns
Delay time from LP to segment output	t_{LSD}	C_L = 100 pF		200	ns
Delay time from FR to segment output	t_{FRSD}	(0 .... n)		400	ns

(V_{DD} = –4.5 to –2.7V, V5 = –12.0 to –28.0 V)

Characteristic	Symbol	Condition		Min.	Max.	Unit
EIO reset time	t_{ER}	C_L = 15 pF (EIO)			150	ns
EIO output delay time	t_{DCL}		V_{SS} = –2.7 V		95	ns
			V_{SS} = –2.7 V		85	
Delay time from LP to segment output	t_{LSD}	C_L = 100 pF			400	ns
Delay time from FR to segment output	t_{FRSD}	(0 .... n)			800	ns

■ PAD LAYOUT



Chip size: 11.59 × 1.40 mm
Pad pitch: 105 µm (Min.)
Chip thickness: 625 µm ±25 µm

(1) SED1640D$_{OB}$ Au bump specifications (reference)

Bump size A	: 106 µm × 80 µm × 4 µm	(Pad Nos. 2 to 26)
Bump size B	: 86 µm × 91 µm × 4 µm	(Pad Nos. 1, 27, 37, 98)
Bump size C	: 86 µm × 68 µm × 4 µm	(Pad Nos. 28 to 36, 99 to 107)
Bump size D	: 82 µm × 74 µm × 4 µm	(Pad Nos. 38 to 97)
Bump height A to D	: 22.5 ±5.5 µm	(Pad Nos. 1 to 107)

■ PAD COORDINATION

Pad No.	Pad name	X coordinate	Y coordinate	Pad No.	Pad name	X coordinate	Y coordinate	Pad No.	Pad name	X coordinate	Y coordinate
2	V_0	–5345	–541	38	O10	5269	553	74	O46	–1161	553
3	V_2	–5164		39	O11	5090		75	O47	–1340	
4	V_3	–4984		40	O12	4912		76	O48	–1518	
5	V_5	–4594		41	O13	4733		77	O49	–1697	
6	V_{SS}	–4091		42	O14	4554		78	O50	–1875	
7	Dummy	–3839		43	O15	4376		79	O51	–2054	
8	SHL	–3587		44	O16	4197		80	O52	–2233	
9	Dummy	–3065		45	O17	4019		81	O53	–2411	
10	Dummy	–2828		46	O18	3840		82	O54	–2590	
11	V_{DD}	–2590		47	O19	3661		83	O55	–2768	
12	$\overline{DSPOFF}$	–2086		48	O20	3483		84	O56	–2947	
13	FR	–1583		49	O21	3304		85	O57	–3126	
14	LP	–1079		50	O22	3126		86	O58	–3304	
15	XSCL	1079		51	O23	2947		87	O59	–3483	
16	D0	1583		52	O24	2768		88	O60	–3661	
17	D1	2086		53	O25	2590		89	O61	–3840	
18	D2	2590		54	O26	2411		90	O62	–4019	
19	Dummy	3065		55	O27	2233		91	O63	–4197	
20	D3	3587		56	O28	2054		92	O64	–4376	
21	Dummy	3839		57	O29	1875		93	O65	–4554	
22	V_{SS}	4091		58	O30	1697		94	O66	–4733	
23	V_5	4594		59	O31	1518		95	O67	–4912	
24	V_3	4984		60	O32	1340		96	O68	–5090	
25	V_2	5164		61	O33	1161		97	O69	–5269	
26	V_0	5345		62	O34	982		98	O70	–5644	546
27	EIO1	5644	–544	63	O35	804		99	O71		418
28	O0		–426	64	O36	625		100	O72		313
29	O1		–320	65	O37	447		101	O73		207
30	O2		–215	66	O38	268		102	O74		102
31	O3		–109	67	O39	89		103	O75		–4
32	O4		–4	68	O40	–89		104	O76		–109
33	O5		102	69	O41	–268		105	O77		–215
34	O6		207	70	O42	–447		106	O78		–320
35	O7		313	71	O43	–625		107	O79		–426
36	O8		418	72	O44	–804		1	EIO2		–544
37	O9		546	73	O45	–982					

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